iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 6 **Issue:** II **Month of publication:** February 2018

DOI:

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 6.887
Volume 6 Issue II, February 2018- Available at www.ijraset.com

Circuit Level Leakage Minimization Techniques in CMOS VLSI Circuits: Literature Review

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Abstract: ***Low power has emerged as a principal theme in today's world of electronics industries. Power dissipation has become an important consideration as performance and area for VLSI Chip design. With shrinking technology reducing power consumption and over all power management on chip are the key challenges below 100nm due to increased complexity. For many designs, optimization of power is important as timing due to the need to reduce package cost and extended battery life.***
For power management leakage current also plays an important role in low power VLSI designs. In CMOS circuits, increased sub-threshold leakage current refers static power dissipation is the result of low threshold voltage. For the most recent CMOS technologies static power dissipation i.e. leakage power dissipation has become a challenging area for VLSI chip designers. According to ITRS (International technology road-map for semiconductors), leakage power is becoming a dominant part of total power consumption. To prolong the battery life of portable devices, leakage power reduction is the primary goal. This paper describes about the various strategies, methodologies and power management techniques for low power circuits and systems. Future challenges that must be met to designs low power high performance circuits are also discussed.
Keywords: Power Dissipation, low power, process nodes, leakage current, power management.

I. INTRODUCTION

There are two main sources of power dissipation in very large-scale integration (VLSI) circuits namely the dynamic power and the static power. Dynamic power is consumed when the device is in active mode that is when the signals are changing their states from 0 to 1 or vice versa. Static power is consumed when the device is turned ON, but in standby mode and no signals are changing their values. At process nodes below 100 nm technology, power consumption due to leakage has joined switching activity as a primary power management concern. There are many techniques [1] that have been developed over the past decade to address the continuously aggressive power reduction requirements of most of the high performance. The basic techniques for low power design such as: clock gating for reducing dynamic power, multiple threshold voltage (multi-Vt) to decrease leakage current, are well-established and supported by existing tools [2].

II. SOURCES OF POWER DISSIPATION

In a circuit two components are responsible for power dissipation: dynamic power and static power. i.e

$$P_{Total}=P_{dynamic}+P_{shortcircuit}+P_{static} \quad (1)$$

Figure 1 displays the various component of total power dissipation [3].

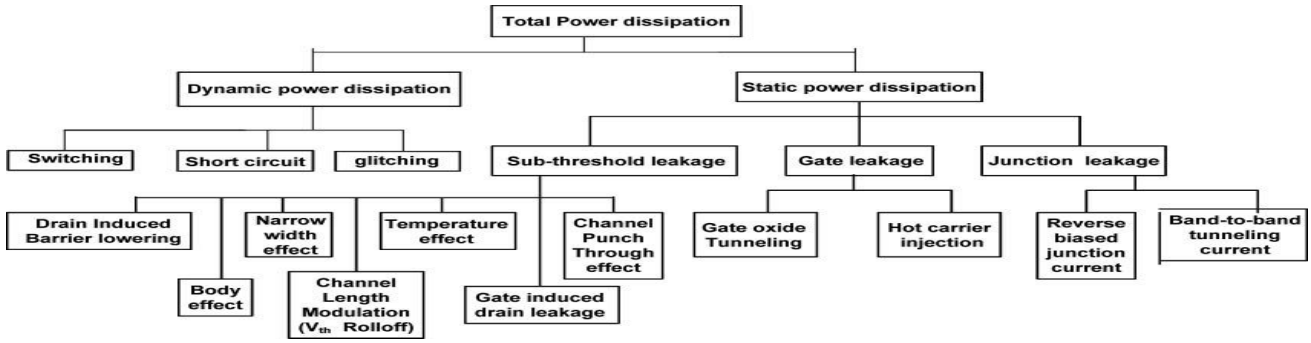

Figure 1:Types of Power Dissipation In VLSI Circuits

Out of these, dynamic power or switching power is primarily power dissipated when charging or discharging capacitors and is described below [4, 5]

A. Dynamic Power Dissipation

$P_{dynamic} = C_L Vdd^2 \alpha f$ (2)

Where CL: Load Capacitance, a function of fan-out, wire length, and transistor size, Vdd: Supply Voltage, which has been dropping with successive process nodes, α: Activity Factor, meaning how often, on average, the wires switch, f: Clock Frequency, which is increasing at each successive process node.

B. Voltage

Because of its quadratic relationship to power , voltage reduction offers the most effective means of minimizing power consumption. Without requiring any special circuits and technologies, a factor of two reduction in supply voltage yields a factor of four decreases in power consumption. Unfortunately, there is speed penalty for supply voltage reduction and delays drastically increase as Vdd approaches to the threshold voltage Vt of the device. The approach to reduce the supply voltage without loss in throughput is to modify the threshold voltage of the devices. Reducing the Vt allows the supply voltage to be scaled down without loss in speed. The limit of how low the Vt can go is set by the requirement to set adequate noise margins and control the increase in the subtreshold leakage current [6,8,10].

C. Physical Capacitance

Dynamic power consumption depends linearly on the physical capacitance being switched. So, in addition to operating at low voltages, minimizing capacitances offer another technique for minimizing power consumption. The capacitances can be kept at a minimum by using less logic, smaller devices, fewer and shorter wires[6,8,10]. As with voltage, however, we are not free to optimize capacitances independently, for example reducing device sizes reduces physical capacitance, but it also reduces the current drive of the transistor making the circuit operate more slowly.

D. Switching Activity

There are two components to switching activity : F_{clk} which determines the average periodicity of data arrivals and E(sw)which determines how many transitions each arrival will generate[14]. E(sw) is reduced by selecting proper algorithms architecture optimization, by proper choice of logic topology and by logic level optimization which results in less power[15]. The data activity E(sw) are combined with the physical capacitance C to obtained switch capacitance C_{SW}=C.E(sw),which describes the average capacitance charge during each data period1/Fclk which determines the power consumed by CMOS circuit[9].

E. Short Ciruit Power Dissipation

Short circuit power consumption is less than 15% of dynamic power consumption if rise and fall time of input(s) and output(s) are equivalent. Exploitation of appropriate circuit and device designing techniques can endeavor in bogging down the short circuit and leakage current.

$P\ Short\text{-}Circuit = k * (Vdd - 2\ Vt)2 * t * N * f$ (3)

Where k is a constant depends on Transistor size and technology, Vt is the Threshold Voltage of Transistor, t is the rise or fall time of the transistors, N is the average no. of transistors in the output stage and f is the clock frequency.

F. Static Power Dissipation

Static power dissipation takes place when the device is turned

ON with power supply but it does not perform any useful task. In other words, the device is in standby mode and no signal transition taking place. In CMOS circuits, there is no direct path from Vdd to GND and so there is no static power dissipation, but there exists various leakage current mechanisms which are responsible for static power dissipation. Few of leakage current minimization techniques are discussed here

III.SURVEY OF LEAKAGE CURRENT MINIMIZATION TECHNIQUE

A. Dual V_T and MTCMOS

This is a basic approach to reduce the leakage power. MTCMOS reduces the leakage by introducing the high threshold NMOS gating between pull down network and ground terminal, in series to low threshold voltage circuitry. As stated in [6] Dual V_T technique is a variation in MTCMOS, in which high threshold voltage can be assigned to transistors of non-critical path to reduce leakage current and low threshold voltage transistors are used in critical paths. An additional mask layer is required due to V_T (Threshold voltage) variation, thereby making fabrication process complicated. This technique suffers from latency period i.e. it need some time to get into normal operating mode after reactivation. The structure for dual V_T and MTCMOS technique is shown as:

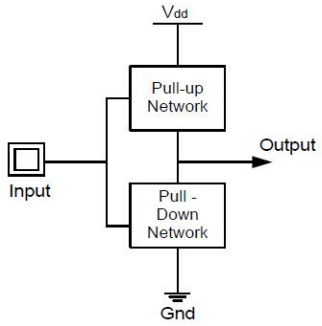

Figure 2: Dual V_T and MTCMOS Structure

B. Sleep Transistor Technique

Addition to the MTCMOS technique, high V_T sleep transistor is introduced between V_{DD} (supply voltage) and pull up network, and between pull down network and ground for high switching speed, where low V_T transistors are used in circuit [10]. Efficient power management is done by sleep control mechanism. This modified MTCMOS technique can only reduce the standby leakage power and the introduced MOSFETs results increase in area and delay. During stand-by mode both sleep transistors gets turned off, introducing large resistance in conduction path and thus, leakage current is low. Isolation between V_{DD} and ground path is necessary for leakage reduction. This technique faces a problem for data retention purpose during sleep mode. The Wakeup time and energy of the sleep technique have a significant impact on the efficiency of the circuit

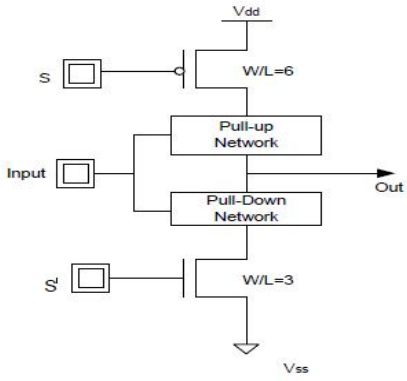

Figure 3: Sleep Transistor Approach

C. Novel Sleep Transistor Technique

The new sleepy inverter makes use of PMOS transistor as the pull down sleep transistor and NMOS transistor as the pull up sleep transistor. During active operation the sleep signal slp is held at logic 0 value and sleep bar signal slpb is held at logic 1 value. During the active period the two sleep transistors M3 and M4 are on. The node VG is at a higher potential than ground and the node VP is at a lower potential than VDD. The inverter circuit thus

sees lower potential difference across nodes VP and VG. Thus the current though the circuit reduces and power dissipation comes down. For the standby mode of operation the signal slp is made logic 1 and signal slpb is made logic 0. Transistor M3 and M4 are off and provide a very high impedance path between VDD and ground and leakage current is lowered. The power dissipation during this

standby mode of operation is the lowest.

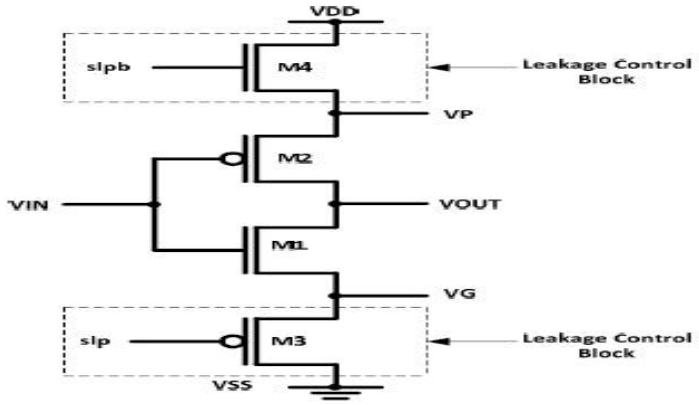

Figure 4: Novel Sleep Transistor Technique

D. State Retention with low leakage power

The novel low leak sleepy inverter though provides excellent low leakage power operation, has degraded output voltage levels during active mode of operation. The inverter output is not at good logic levels. During sleep (standby) mode of operation, the last output state is also not retained. To address these issues, a state retention transistor is connected in parallel to the sleepy transistors in the circuit of low leak sleepy inverter. The proposed state retention low leak inverter is shown in figure 8. An NMOS transistor is connected in parallel to PMOS pull down to achieve state retention; a PMOS transistor is used to maintain the last state during sleep in the pull up path in parallel to NMOS sleep transistor. During Active mode operation the sleep signal slp is maintained at logic 0 value and slpb is held at logic 1 value. These sleep signals cause both pairs of P and N transistors in the pull up and pull down path to be on. The output is at good logic levels. During sleep (standby) mode of operation sleep signals slp and slpb are held at logic 1 and 0 values respectively. Both the pairs of sleep transistors are off and hence reduced leakage current and lower power dissipation.

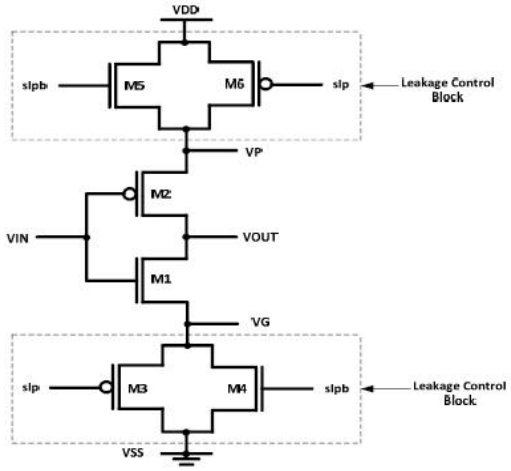

Figure 5:Novel Sleep Transistor with state retention

E. Forced Stack Technique

The authors in their work [1] have proposed new technique named as forced stack technique because of the limitations of previously introduced techniques. This technique includes duplication of an already present transistor into two half sized

transistors. There exists a reverse bias due to duplicated transistors when both the transistors are turned off, which results in sub threshold leakage current reduction. It is a state retention technique with disadvantage of increased delay and area.

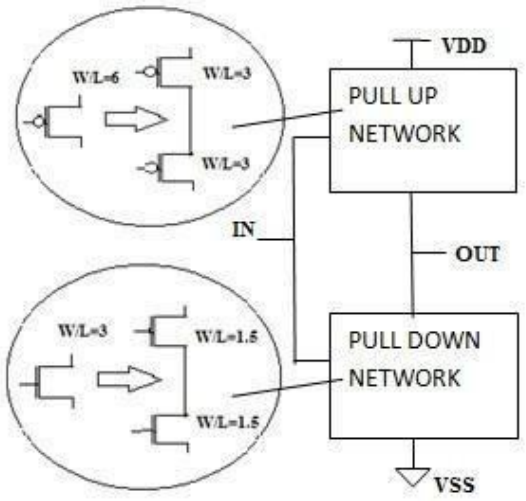

Figure 6: Forced Stack Approach

F. Zigzag Technique

To reduce the power consumption to a maximum possible extent, this technique uses one sleep transistor in each logic state either in pull-up or pull-down network according to a particular input vector. Then, we either assign a transistor to the pull-down network if the output is „1 or else assign a sleep transistor to the pull-up network if the output is „0.The zigzag technique is introduced to reduce the wake-up cost by choosing a specific state but it has a limitation of state destruction. As mentioned in [2] it may require extra circuitry to regenerate a specific input vector through some means on wake up mode.

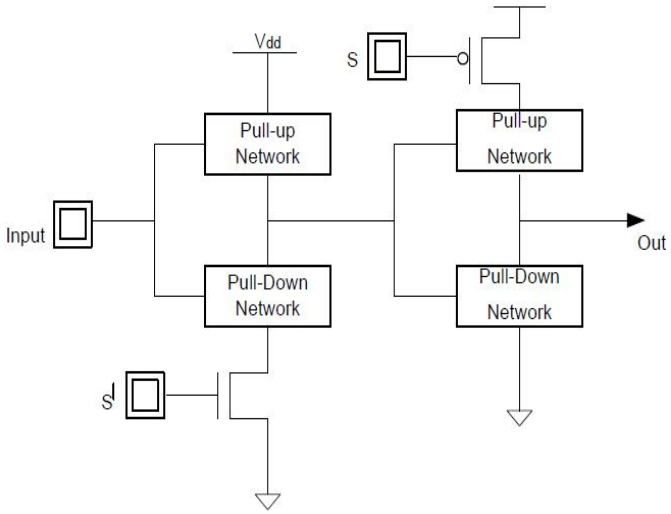

Figure 7: Zigzag Approach

G. Sleepy Stack Technique

This technique combines the features of sleepy transistor technique and forced stack technique. In this technique, the sleep transistor is added parallel to the two half sized transistors configuration is used to replace the original transistor in the circuit. During sleep mode, sleep transistors are turned off and stacked transistors suppress leakage current while saving state. Variation in the width of sleep transistor results tradeoffs in power, area and delay. Additional control and monitoring circuit is required for the sleep transistor.

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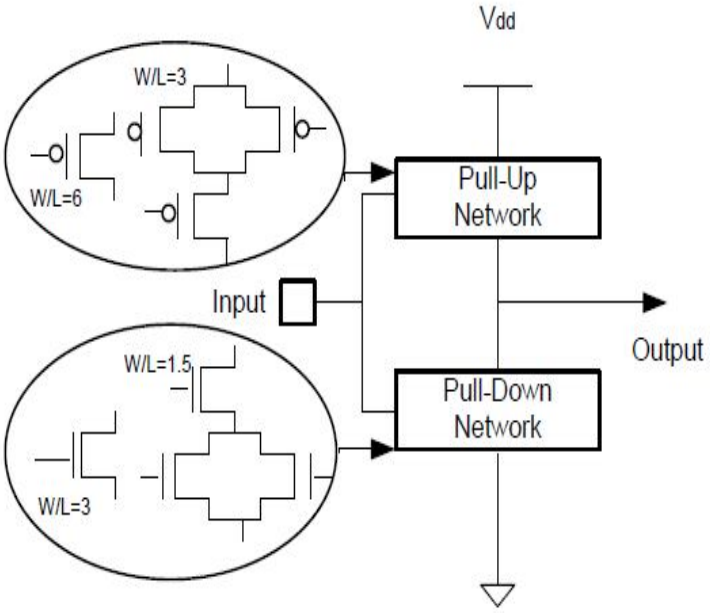


Figure 8: Sleep Stack Approach

H. Leakage Feedback Technique

transistor to the pull-down network if the output is „1" or else assign a sleep transistor to the pull-up network if the output is „0".The zigzag technique is introduced to reduce the wake-up cost by choosing a specific state but it has a limitation of state destruction. As mentioned in [2] it may require extra circuitry to regenerate a specific input vector through some means on wake up mode.

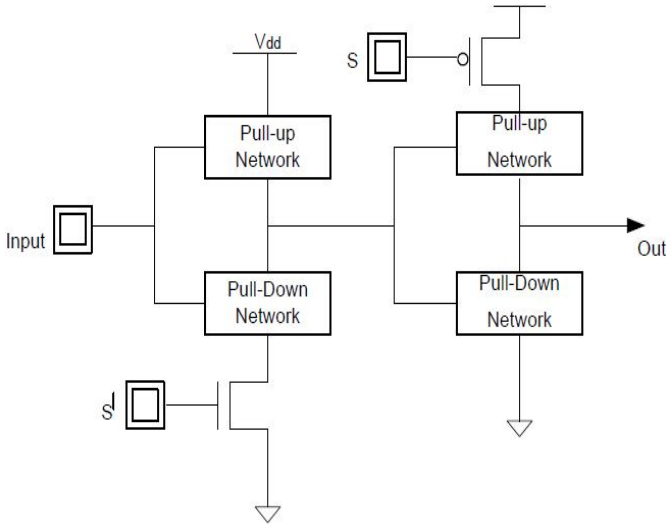


Figure 9: Zigzag Approach

I. Leakage Feedback Technique

To maintain logic during sleep mode, the leakage feedback technique uses two additional transistors and the two transistors are driven by the output of an inverter which is driven by output of the circuit implemented utilizing leakage manipulation and format conversion is GIMP, available from

feedback [3]. Performance degradation and increase in area are the limitations along with the limitation of sleep technique.

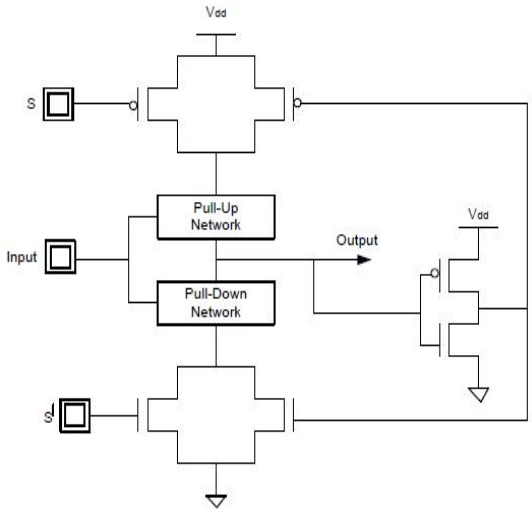
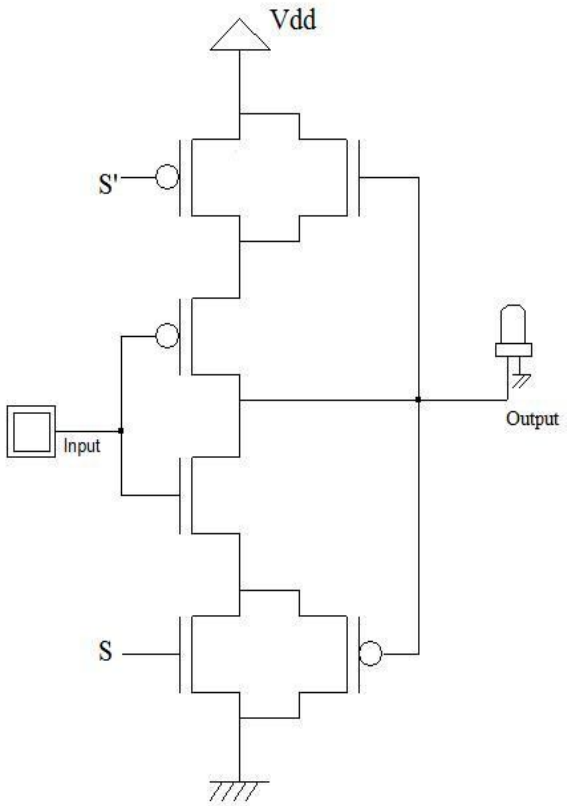


Figure 10: Leakage Feedback Approach

J. Sleepy Keeper Technique

In this technique [7] parallel connected combination of PMOS and NMOS transistor is inserted between pull up network and V_{DD} and pull down network and GND (Ground). When in sleep mode, this additional NMOS transistor is the only source of VDD to the pull-up network and additional PMOS transistor is the only source of GND to the pull down network since the sleep transistor is off. To maintain output value „1" in sleep mode, this approach uses pre-estimated output logic „1" and NMOS transistor connected to V_{DD}. Similarly to retain output logic „0" the PMOS transistor connected to GND is used in sleep mode. This technique uses extra retention transistors to maintain logic state during sleep mode.



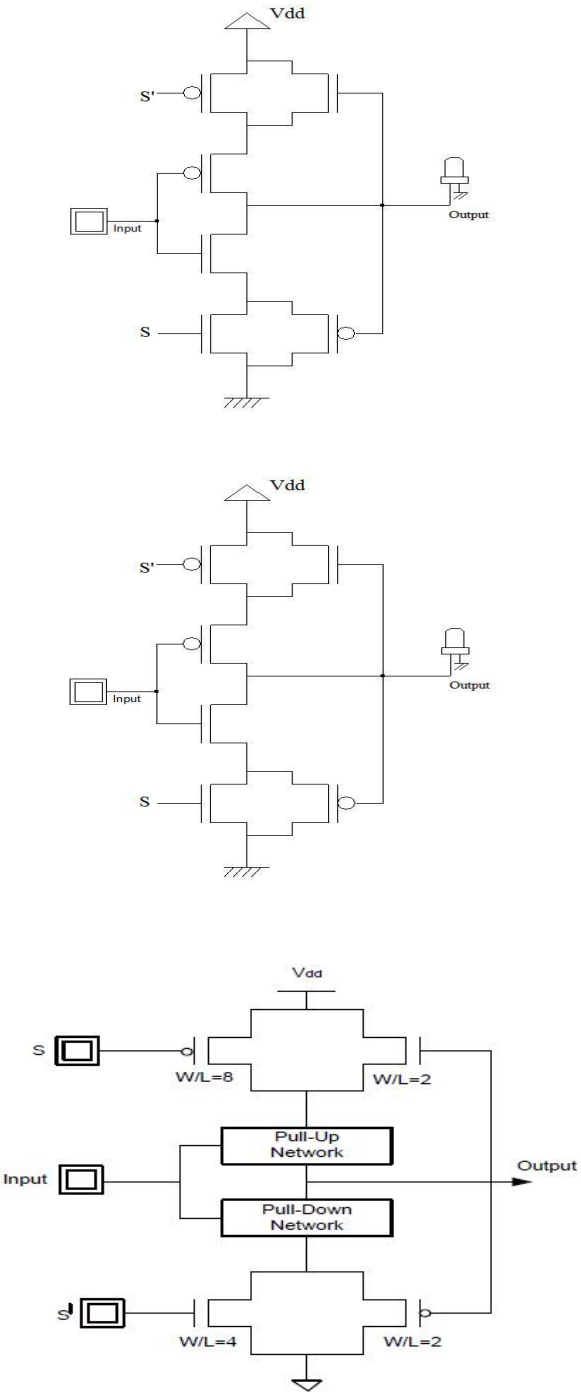


Figure 11: Sleepy Keeper Approach

K. Lector Technique

In LECTOR [8], the concept of effective stacking transistors has been introduced between the VDD and GND for the leakage power reduction. In this technique two leakage control transistors i.e. P-type and N-type are inserted between the pull up and pull down network of a circuit, in which each LCT gate is controlled by the source of other, hence termed as self-controlled stacked transistors. Since it is a self-controlled technique so no external circuit is required for controlling purpose. These LCT produces high resistance path between the V_{DD} and GND by turning more than one transistor OFF, thereby reducing the leakage current. This technique has a very low leakage but there is no provision of sleep mode of operation for state retention.

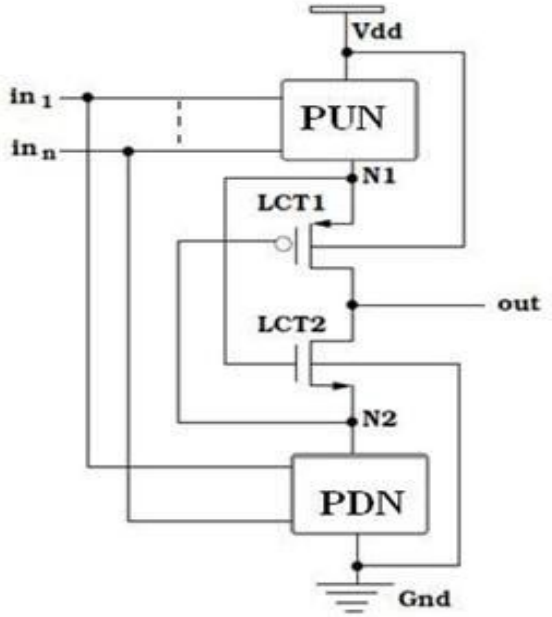


Figure 12: LECTOR Approach

L. GALEOR Technique

Introduction of stacking effect in the circuit results reduction in leakage current flowing across circuit, in GALEOR technique. In this approach, one gate leakage high V_T NMOS transistor is introduced between the output and the pull up network and another gated leakage high V_T PMOS transistor in inserted between output and the pull down network. Due to the threshold voltage loss caused by high V_T MOS transistors, this technique suffers from significant low voltage swing where low logic level appears much above than 0 and high logic level occurs much below than V_{DD}. Increase of propagation delay is result of low output voltage swing.

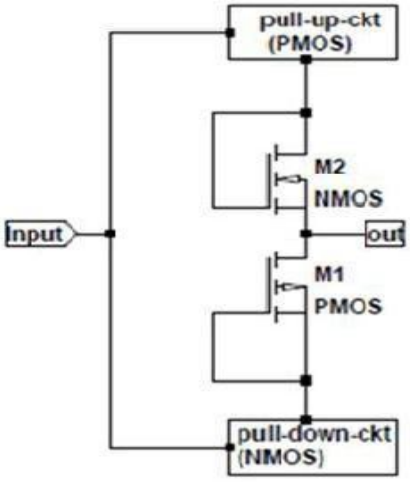


Figure 13: GALEOR Approach

J. LECTOR Stack State Retention (LSSR)

This technique combines the feature of both, LECTOR approach and the Forced Stack Technique with the additional feature of state retention in circuit. The circuit configuration includes [1], two leakage control transistors are added between the pull up and pull down network, and the stack effect is introduced to pull up and pull down network by replacing each existing transistor with two half sized transistors. It provides the limitation of area because of usage of extra transistors to preserve the circuit state during sleep mode. But this technique provides good leakage current reduction without any delay penalty.

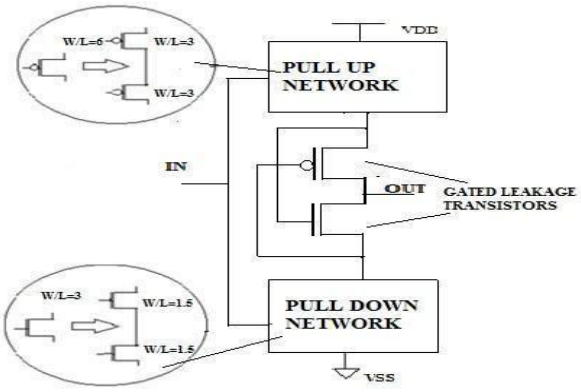


Figure 11: LECTOR Stack State Retention (LSSR) Approach

K. Zigzag Keepers Technique

This approach is proposed to reduce the leakage power consumption to a large extent along with the property of state preservation during sleep mode. Zigzag Keepers approach [9] has added the qualities of both the approaches, Zigzag approach and sleepy Keepers Technique. Here, along with the sleep transistors, two additional transistors which are driven by pre-estimated output logic are introduced in a parallel with sleep transistors which are for saving the logic state.

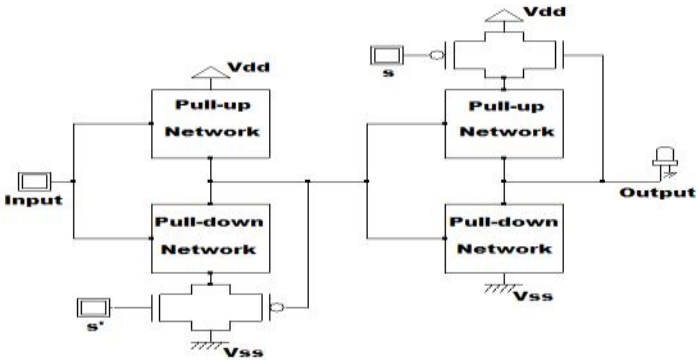


Figure 12: Zigzag Keepers Approach

IV.COMPARATIVE STUDY

In this paper, we have presented a detail review and analysis of the circuit level leakage minimization techniques for CMOS VLSI circuits in nanoscale era. We then classified all the techniques related to leakage minimization based on the fundamental concept of enhancing the threshold voltage, either by multi-V_t, transistor stacking, body biasing, or input vector control. All the techniques considered

Here share the same objective of minimizing the leakage.

We then classified all the techniques related to leakage

Minimization based on fundamental concept of enhancing the threshold voltage in circuit level.

In this paper, we have presented a detail review and analysis of the circuit level leakage minimization techniques for CMOS VLSI circuits in nanoscale era.

Sl. no publication		Techniques	Advantages	Limitation
(1)	1995	Power gating [33]	Very high leakage power saving, industry preferred technique	
(2)	1998	Forced stack [42]	Substantial leakage saving, ease of implementation, no need for controller design, single threshold transistor and easy to fabricate	Delay penalty, need for dual threshold transistors, data retention problem controller design needed

Increases circuit delay

(3)	1999	Mixed Vt Scheme [41]	More leakage reduction	This technique require extra library
(4)	2001	VTCMOS [35]	Leakage and delay advantage by tuning the threshold voltage	

Additional controller is needed to control the body bias

(5)	2001	Leakage feedback approach [38]	

Solves data retention problem and minimizes leakage
Area and delay penalty due to additional transistor

(6)	2002	Super-cut-off CMOS circuit [56]	Substantial leakage power saving, single threshold transistor and easy to fabricate	
(7)	2003	DTMOS [34]	Dynamically tuned threshold voltage for low leakage and high speed	
(8)	2003	Zigzag approach [57]	Removing the problem of floating node as in power gating approach and better leakage saving	

Complex control design and large delay penalty

RC time constant shift the body signal, higher energy consumption
Designing is complicated and delay is an issue

(9)	2004	Input vector control [49–53]		Leakage saving is based on input vectorsxtensive computational time requirement and dynamic power is not taken into consideration
(10)	2004	LECTOR [46]	Better leakage reduction, no need of additional circuitry to monitor leakage	
(11)	2004	NC SRAM cell [61]	Leakage current reduction by DIBL effect and raising the source voltage	

Signal quality problem
This technique also have the problem of delay degradation

(12)	2004	Dual Threshold [36]	Leakage saving and speed advantage	Doubles the library size and increased design efforts
(13)	2005	Sleepy stack [43]	Lesser delay penalty compared to the forced stacking	

Lower leakage saving with respect to forced stacking, increase in transistor count

(14)	2005	Control point insertion [44]	Average leakage reduction	Dynamic power and area is a penalty
(15)	2006	Sleepy keeper approach [39]	Solving data retention problem	Control signals are needed for sleep transistors and having area penalty
(16)	2008	GALEOR [47]	Better leakage saving with no external control	Signal quality is poor than lector technique
(17)	2009	PP SRAM cell [62]	Leakage reduction is more than NC SRAM, performance is also better	

At the cost of additional circuitry

(18)	2010	Drain gating [48]	Better leakage saving and logic levels are good	External controller is needed
(19)	2010	Dual stack [40]	Better leakage saving	Delay and area penalty due to additional helper transistors
(20)	2012	Bootstrapped circuit [54]	Active leakage current reduction	Additional circuit is needed to control the leakage
(21)	2012	Clamping diode SRAM cell [59]	More leakage saving by clamping the source voltage to high value	

This technique have delay degradation

(22)	2012	Bootstrapped repeater circuit [63]	

This technique reduce the leakage current, delay and noise
dditional circuit is controlling the leakage current

(23)	2012	Schmitt trigger logic [65]	This technique reduces the leakage current effectively

However, it requires additional quenching circuit

(24)	2013	ONOFIC [58]	Less leakage reduction than lector and less delay	Leakage reduction is not more as compared to other techniques
(25)	2014	INDEP [55]	More leakage saving in this approach	As a separate algorithm is needed, so the computational complexity increases
(26)	2014	Multi-bit retention register for power gated design [64]		

It reduces more leakage power than single bit register
It require multiple bit retention register as well as efficient assignment algorithm

(27)	2014	Skewed IO with split input/output cell [66]		

It reduces the leakage current substantially But, this technique needs extra PMOS and NMOS transistors

(28)	2015	Leakage power minimization of SRAM under radiation environment [67]		

It reduces Leakage and scrubbing power under radiation environment
It requires complex algorithm design

V.OPEN ISSUES

A summary on various leakage reduction techniques with their advantages and limitations have been presented in Table 6. While making such a review, we have taken most of the referred techniques from 1995 to 2015.
By referring to the above table there is tradeoff between three parameters i.e. Power, Area and Delay .In future there is wide Scope in Low power VLSI Design to minimize all above said quantities

VI.CONCLUSION

The aim of electronic design is to create a balance between power efficiency and performance in terms of speed. Design of VLSI circuits for low power applications is a multi faceted problem as the circuit designers have to follow several degrees of freedom to have acceptable power reduction.
In this paper, various strategies and methodologies used for minimizing the leakage and dynamic power are presented. The strategies and methodologies which are discussed in this paper are very much useful for the designers to design low power VLSI circuits which are used in portable and biomedical applications.

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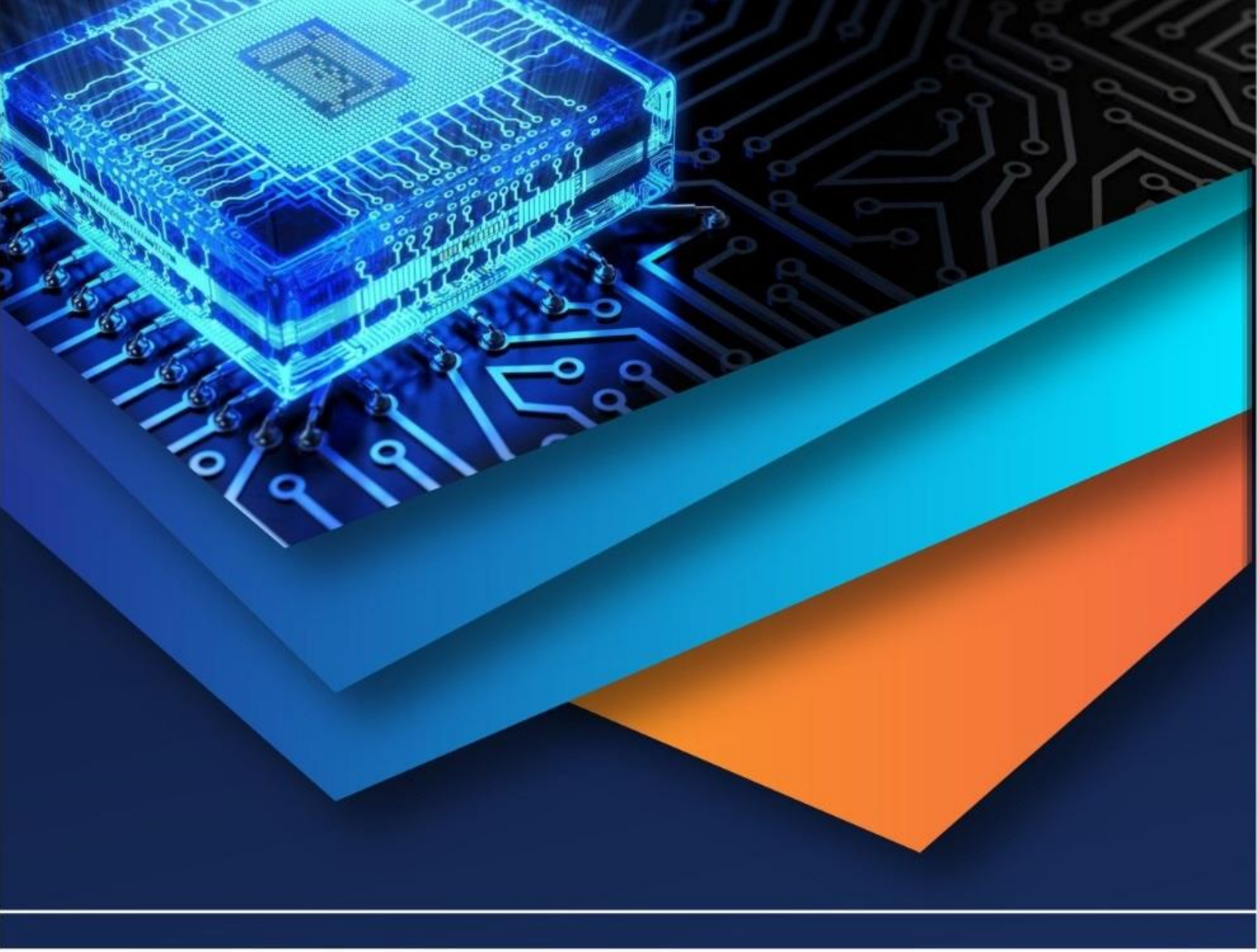

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