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Design of Low Power High Speed Hybrid 1-Bit Full Adder by using CMOS 130nm Technology

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Abstract: ***In this paper a 1-bit hybrid full adder design is reported. This design employing transmission gate, pass transistor logic and complimentary metal-oxide semiconductor (CMOS) logics. Firstly, the design was implemented for 1-bit and then it is finally extended for 64-bit also. The circuit was implemented using Mentor Graphics tool in 130-nm technology. Performance parameters such as delay, power, no of transistors, layout area and power delay product(PDP) were compared with the existing designs with proposed 1-bit hybrid full adder & modified hybrid 1-bit full adder. This design is found to be working efficiently with less power dissipation and less delay at 130-nmtechnology for 1V supply voltage. In comparing with the existing full adder circuits, the present implementation is found to offer better significant improvement in speed, power and area.***

Keywords: Hybrid CMOS, Full adder, XOR, HYBRID Adder Design, Power Delay Product (PDP), low power Simulation.

I. INTRODUCTION

The Full adders, being one of the most fundamental building block of all the aforementioned circuit applications, remain a key focus domain of the researchers over the years [1]. Demand and popularity of portable electronics is driving the designers to strive for smaller silicon area, higher speeds, longer battery life and more reliability [3]. The adders play an important role in complex arithmetic and computational circuits such as multiplier, comparator and parity checkers [2]. Several logic styles have been used in the past to design full-adder cells. Each design style has its merits and demerits. [3] Several logic styles have been used in the past to design full-adder cells. Each design style has its merits and demerits. The classical static CMOS full-adder is based on regular CMOS structure with conventional pull-up and pull-down. Transistors providing full-swing output and good driving capabilities. Another conventional adder is the complementary pass transistor logic (CPL). It provides full-swing operation and good driving capability but due to the presence of a lot of internal nodes and static inverters, there is large power dissipation. Dynamic CMOS logic style provides high speed of operation but has several inherent problems like charge sharing and high clock load. Other designs include transmission function full-adder (TFA) and transmission-gate full-adder (TGA) [3]. There is a limited amount of power available for the mobile systems. So, designers are faced with more constraints: high speed, high throughput, small silicon area, and at the same time, low-power consumption. So, building low power, high-performance adder cells is of great interest [4].
The conventional adder is the complementary pass-transistor logic (CPL). It provides high-speed, full-swing operation and good driving capability due to the output static inverters and the fast differential stage of cross-coupled PMOS transistors. But due to the presence of a lot of internal nodes and static inverters, there is large power dissipation. [5] Adder is an elementary unit of microprocessors. It is used in ALU, floating-point unit, memory address generation unit, etc. Full and half adder cells are the cores dominating the critical paths of complex arithmetic's like subtraction, multiplication, division, exponentiation, etc. Thus, their performance and complexity at transistor level directly influence the overall performance of the system. Depending on the circuits from which the adder cells are implemented, different performance parameters and design considerations are important. These factors include supply voltage**,** process tolerance, delay, power delay product, area, driving capability and whether single or dual rail logic is used [6].

II. MODIFIED METHOD

The existing full adder circuit is represented by three blocks as shown in fig9.module1 and module2 are the XNOR modules that generate the sum signal (SUM) and module3 generates the output carry signal(Cout).each module is designed individually such that the entire adder circuit is optimized in terms of power, delay, and area. These modules are discussed below in detail

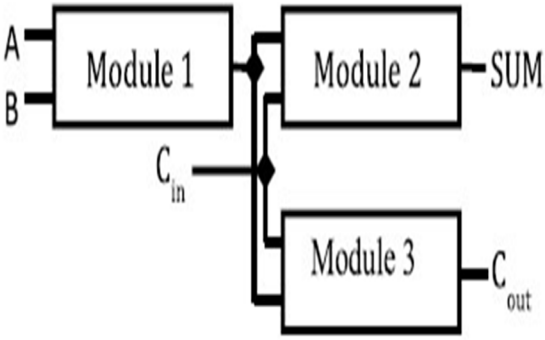

Fig 1: Schematic structure of re modified full adder.

A. XOR Module

Before we present the new adders, we first propose a new XOR gate, shown in Fig10. It resembles the inverter-based XOR shown in Fig. but the difference is that the VDD connection in the inverter-based XOR is connected to the input A. Because the new XOR gate has no power supply, it is called Powerless XOR, or
P-XOR. Similarly, we propose a new XOR gate shown in below fig:2,3.

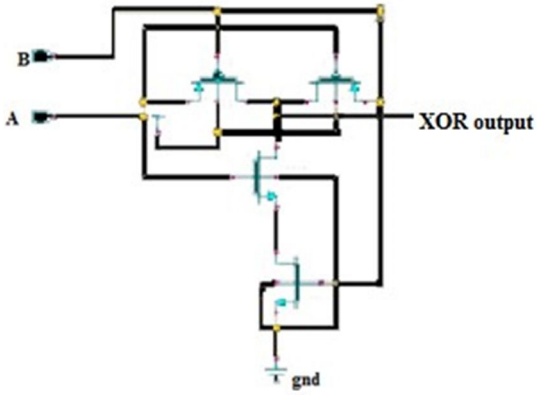

Fig2: XOR module

B. Carry Generation Module

In the circuit, the output carry signal is implemented by the transistors Mp7, Mp8, Mn7 and Mn8 are shown. The input carry signal (Cin) propagates only through a single transmission gate (Mn7 and Mp7) reducing the overall carry propagation path significantly. The deliberate use of strong transmission gates (channel width of transistors Mn7, Mp7, Mn8 and Mp8 is made large) guaranteed further reduction in propagation delay of the carry signal. [9]

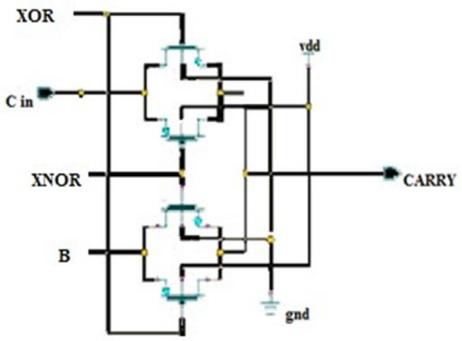

Fig3: Carry generation module

C. Sum Module

The sum module is shown in below fig. This module takes 2input XOR, 2inputXNOR and Cin as the inputs and it produce SUM as the output. For various A, B, Cin inputs this module produce necessary SUM outputs and the Schematic XOR circuit is shown in fig12.

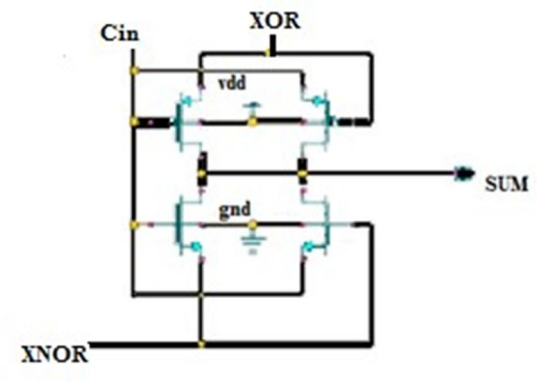

Fig4: Sum module

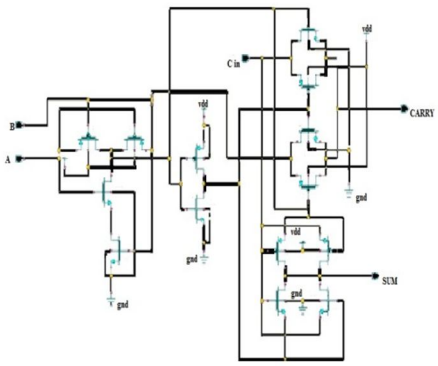

Fig5: Modified Hybrid 1-bit full adder

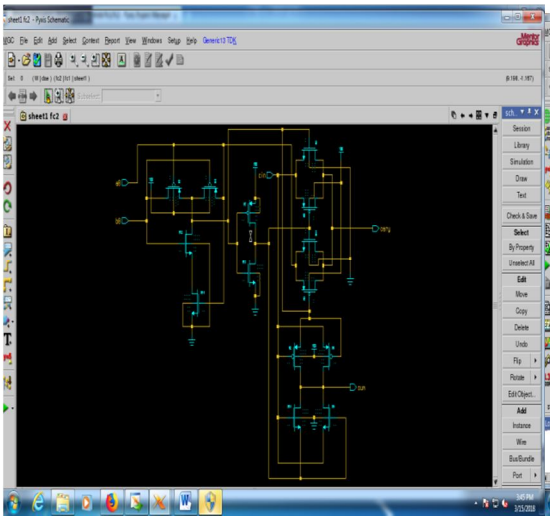

Fig6: Modified hybrid 1-bit full adder and simulation circuit

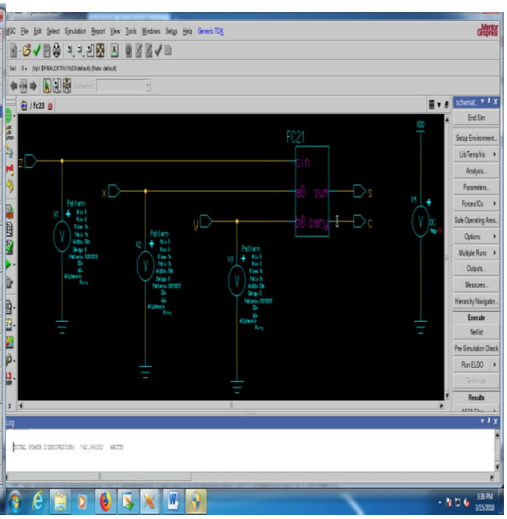

Fig7: Calculation of Total power dissipation design in pyxis schematic

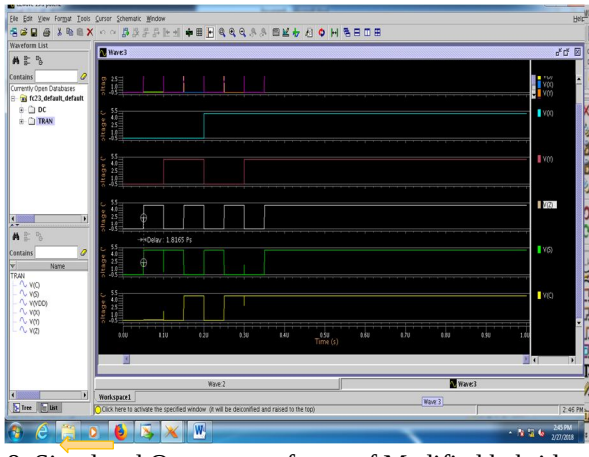

Fig8: Simulated Output waveforms of Modified hybrid

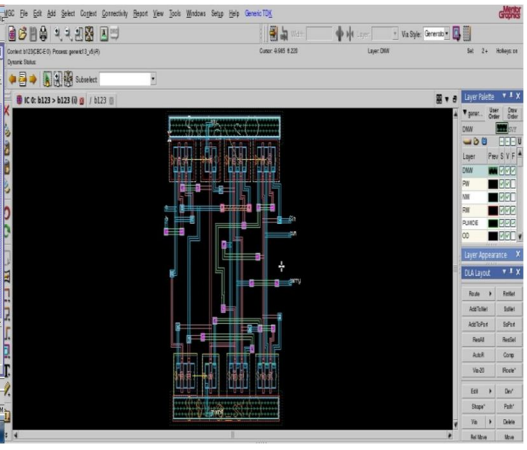

Fig9: Layout of Re modified hybrid 1-bit full adder

1-bit full adder and Delay

Design	Total power dissipation	Delay	PDP	No. of transistors
CPL	10.45nw	0.365 ns	3818.1zs	32
CCMOS	4.53nw	0.457ns	2017.4zs	28
TFA	5.196nw	0.352ns	1830.7zs	26
LEHPSC	5.022nw	0.378ns	1899.8zs	24
HPSC	3.853nw	0.376ns	1450.3zs	22
PTL	3.879nw	0.416ns	1616.8zs	20
Hybrid full adder	1.052nw	0.196ns	206.19zs	16
Modified hybrid full adder	0.742nw	1.816ps	62.30zs	14

Table1: Performance comparison in terms of Delay, PDP and number of transistors

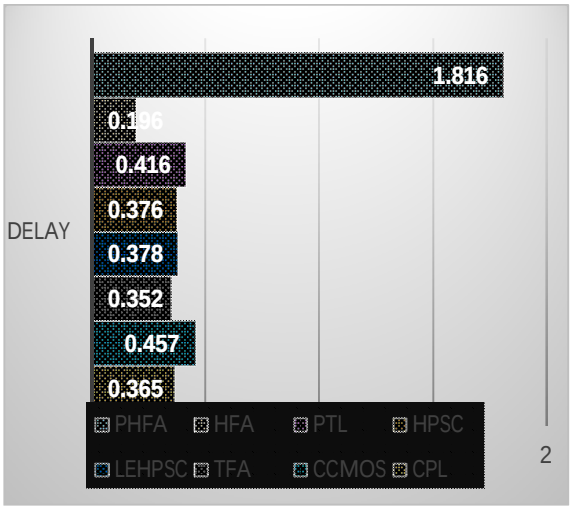

Fig10: Comparison of Total Power dissipation of various full adder designs

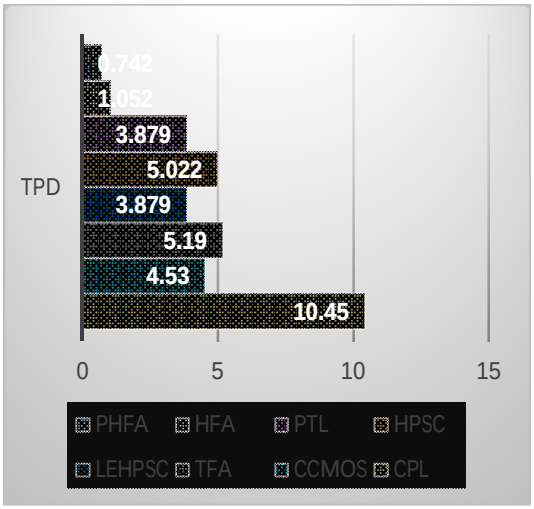

Fig11: Comparison of Delay of various full adder design

III. CONCLUSION

In this paper, a Re-modified full adder is proposed and the simulations are compared with other standard designs (CPL, CCOMS, TFA, LEHPSC, HPSC, PTL, Proposed hybrid adder). The simulation results shows that the Re-modified hybrid full adder offers less power dissipation, less delay and improved PDP compared with the existing designs. Due to the pass transistor logic the power dissipation will reduce and the efficient coupling of strong transmission gates driven by the weak CMOS inverter lead to fast switching speed. The Re-modified hybrid full adder has achieved 95.23% of power reduction and 65.75%of Delay reduction compared to CPL adder design in Mentor Graphic 130-nm Technology.

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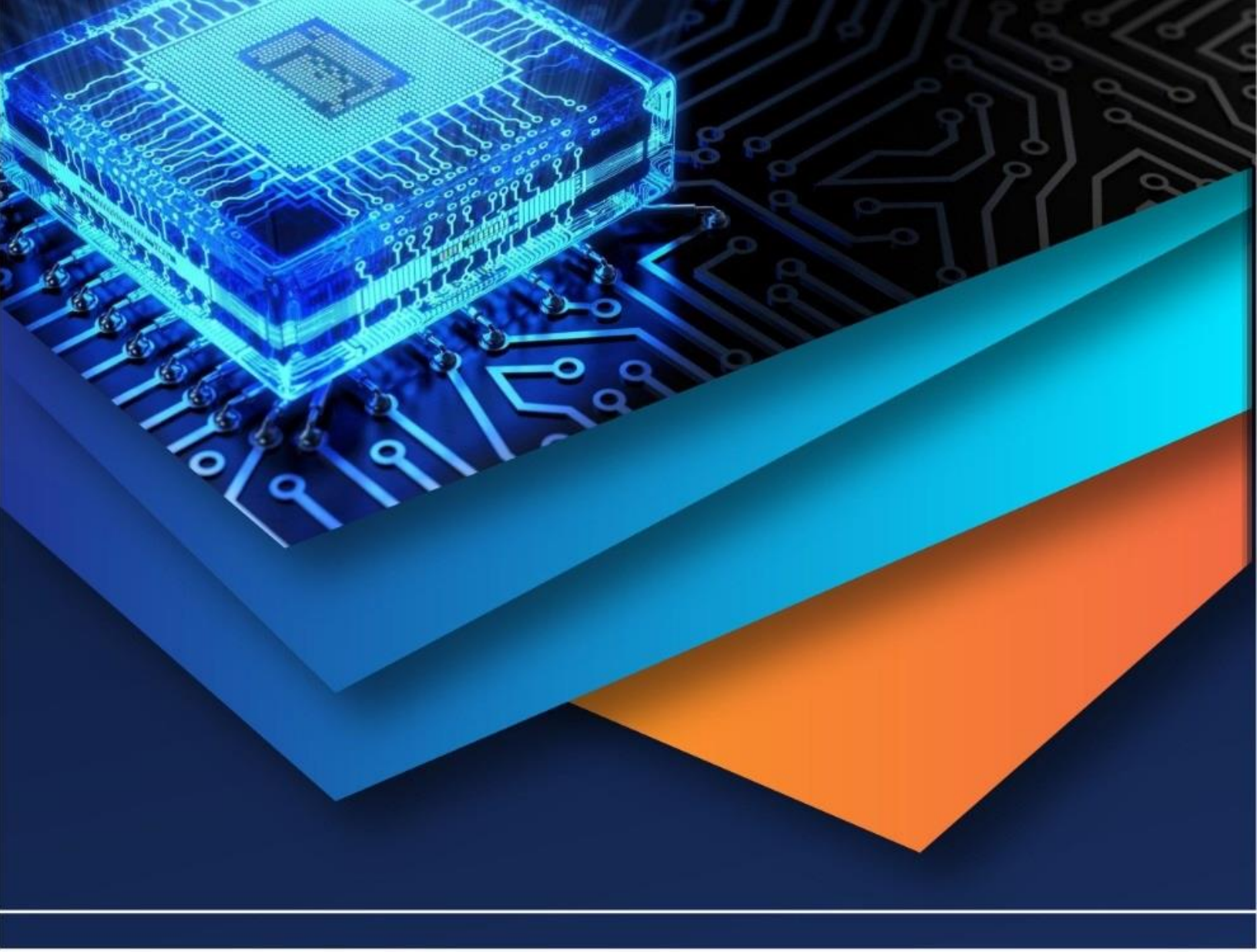

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