iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 6 **Issue:** III **Month of publication:** March 2018

DOI: http://doi.org/10.22214/ijraset.2018.3538

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International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 6.887
Volume 6 Issue III, March 2018- Available at www.ijraset.com

Analysis of Different Full Adder Designs with Power using CMOS 130nm Technology

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Abstract: ***A Full adder adds binary numbers and accounts for values carried in as well as out. A one-bit full adder adds three one-bit numbers, often written as A, B and Cin. A and B are the operands, and Cin is a bit carry. The Full adder is usually a component in a cascade of adders, which add 8,16,32,etc, bit binary numbers .This paper discuss the evalution of full adder circuits in terms of less power consumption high speed and chip area. At first we implemented conventional 28 transistor full adder and then we are implemented different types of full adders like Transmission gate full adder,conventional dynamic full adder,14T full adder, GDI structure based full adder Adder 9B ,Adder 9A,SCRF full adder,8T full adder.***
Keywords: CMOS Transmission gate (TG), Pass Transistor logic (PTL), Gate Diffusion Input (GDI), Static Energy Recovery Full Adder (SERF), Dual Rail domino logic (DRD) , Adder 9A, Adder 9B, GDI Based full adder power, Delay, Channel length.

I. INTRODUCTION

In digital electronics, adder is a digital circuit that performs addition of two numbers. As described in many computers and other kinds of processors, where they are used to calculate addresses, table indices, and many more. To humans, decimal numbers are easy to comprehend and implement for performing arithmetic. Today all the VLSI circuits on low power with high speed. The arithmetic and logic operations are essential behavior for low power high speed application like DSP(Digital Signal Processing),microprocessor,VLSI,microcontroller,ASIC(Application-Specific integrated circuit), binary numbers are more pragmatic for a given computation. This occurs because binary values are optimally efficient at representing many values. Binary adders are one of the most essential logic elements within a digital system. In addition, binary adders are also helpful in units other than Arithmetic Logic Units (ALU), such as multipliers, dividers and memory addressing. Therefore, binary addition is essential that any improvement in binary addition can result in a performance boost for any computing system and, hence, help improve the performance of the entire system.

II. TRUTH TABLE AND EQUATION

From the below truth table, the full adder logic can be implemented. Thus, We can implement a full adder circuit with the help of two half adder circuit. The first will half adder will be used to add A and B to produce a partial sum. The second half adder logic can be used to add CIN to the sum produced by the first half adder to get the final S output. The conventional logic equation for Sum and Carry are Sum = C ex-or (A ex-or B) Carry = (A and B) or C(A ex-or B)

III. DIFFERENT TYPES OF FULL ADDER CIRCUITS

In this section the different types of full adder circuits are discussed.

A. Conventional 28T CMOS Full Adder Circuit

The conventional CMOS [14] adder cell using 28 transistors based on standard CMOS topology. Due to high number of transistors, its power consumption is high. Large PMOS
transistor in pull up network result in high input capacitances, which cause high delay and dynamic power. One of the most significant advantages of this full adder was ts high noise margins and thus reliable operation at low voltages.

B. Transmission Gate Full Adder Circuit:

20 T transmission produces buffered outputs of proper polarity for both sum and carry.. In this circuit 2 inverters are followed by two transmission gates which act as 8-T XOR. Subsequently 8-T XNOR module follows. To has 4 transistor XOR which in the next stage is inverted to produce XNOR. These XOR and XNOR are used generate sum; Cin and *Cin* are multiplexed which can simultaneously to generate sum and Cout. The signals Cin controlled either by (a b) or (a ⊗b).Similarly the Cout can be calculated

by multiplexing a and Cin which is controlled by (a)and *Cin* are multiplexed which can controlled either by (a b) b). The power dissipation in this circuit is more than the 28T or (a ⊗ b). Similarly the Cout can be calculated by multiplexing a and Cin controlled by (a b). The power dissipation in this circuit is more than the 28T adder. However with same power consumption it performs faster.

C. Conventional dynamic full adder circuit

The conventional dynamic full adder cell has 16 transistors and is based on NP-CMOS logic style.

D. 14 T Full Adder Circuit

The 14T full adder contains a 4T PTL XOR gate, an inverter and two transmission gates based multiplexer designs for sum and Cout signals. This circuit compared with the previous 10-transistor full adders and the conventional 28-transistor CMOS adder.

E. 12T Full Adder Circuit

12T has been implemented using six multiplexers and 12 transistors. Each multiplexer is implemented by pass- transistor logic with two transistors. As shown in Fig. 10, there is no VDD or GND connection in this circuit and there are some paths containing three serried transistors. It causes to increase delay of producing SUM signal. The size of each transistor in mentioned path should be three times larger to balance the output and optimize the circuit for PDP. Therefore, the area of the circuit is increased.

F. GDI Structure Based Full Adder Circuit

GDI means Gate diffusion input technique. It is a recent approach in VLSI, it is used to consume the power and area. It consists of three input and one output, the inputs are G, P, N.

The G is common gate input and P represent the S or D of PMOS input& N represent the S or D of NMOS input. when G and N input is either ‘0’ or ‘1’ when P input is ‘1’,it performs A’+B operation otherwise it performs AND operation.When N,P,G has either ‘0’ or ‘1’ input it performs MUX operation. When N input is ‘0’, P input is ‘1’ and G has either ‘0’ or ‘1’,it performs NOT operation.

G. ADDER 9A AND 9B

The Static Energy Recovery XNOR gate is cascaded with the new G-XNOR gate to generate the Sum while the Cout function is implemented by simply multiplexing B and Cin controlled by (A XNOR B) as done in the previous circuits. These two new adders consistently consume less power in high frequencies and have higher speed adder. However with same power consumption it performs faster.

H. Static Energy Recovery Full Adder Circuit

In the 10T adder cell, the implementation of XOR and XNOR of A and B is done using pass transistor logic and an inverter is to complement the input signal A. This implementation results in faster XOR and XNOR outputs and also ensures that there is a balance of delays at the output of these gates. This leads to less spurious SUM and Carry signals (Fig 6). The energy recovering logic reuses charge and therefore consumes less power than non-energy recovering logic.

1) *Advantage:* It should be noted that the new SERF adder has no direct path to the ground. The elimination of a path to the ground reduces power consumption. The charge stored at the load capacitance is reapplied to the control gates. The combination of not having a direct path to ground and the re- application of the load charge to the control gate makes the energy-recovering full adder an energy efficient design.
2) *Disadvantage:* The circuit produces full-swing at the output nodes. But it fails to provide so for the internal nodes. As the power consumption by the circuit reduces the circuit becomes slower.
3) *I.8T Full Adder Circuit:* The basic of 8T full adder consists of 3 modules: 2 XOR elements and a Carry section as shown in fig.5.The Sum output is obtained by two XOR blocks in succession. For the carry section GDI based 2T MUX is used and (A XOR B) as the selection signal. The Sum and the Cout module need 6 and 2 transistors respectively. The transistor level implementation of the eight transistor full adder is shown in Fig. 8. It is obvious from the figure that both Sum and Cout has a maximum delay of 2T. It doesn’t suffer from threshold voltage loss problem. Also the noise margin has been substantially increased by proper sizing of transistors in 3T XOR. The power delay product (PDP), and the area of the proposed adder are also found better than that of the existing 10T and 14T adders. Higher power consumption due to short circuit current.

IV. SCHEMATIC DIAGRAMS OF DIFFERENT FULL ADDER CIRCUITS

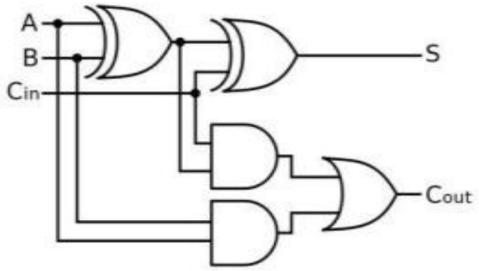


Figure: Block diagram of full adder

Table i
Truth table of full adder 1

A	B	C	S	C_{OUT}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

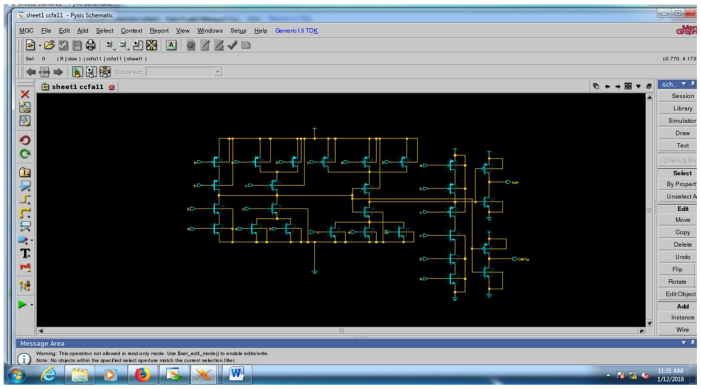


Fig (2: 28T Conventional CMOS Full adder

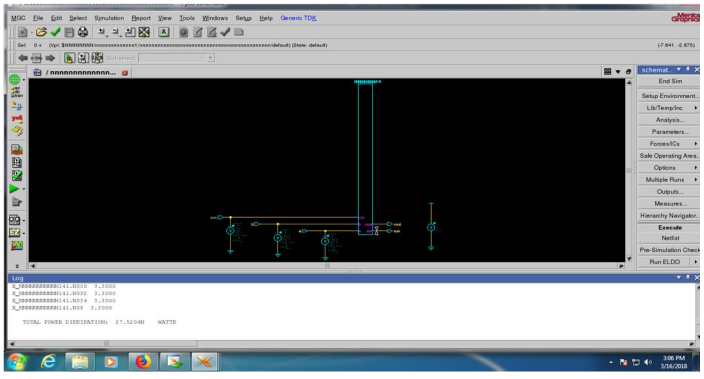


Fig (3): Power dissipation of 28T Conventional CMOS Full adder

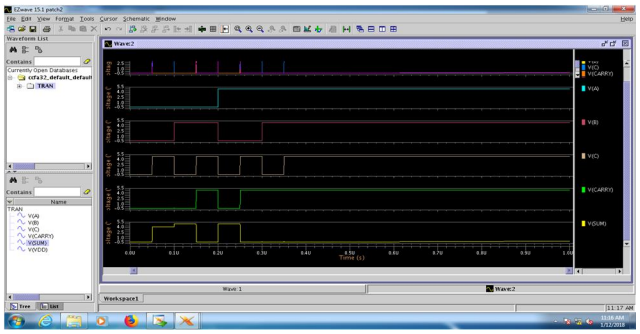


Fig (4) : Waveforms of 28T Conventional CMOS Full adder

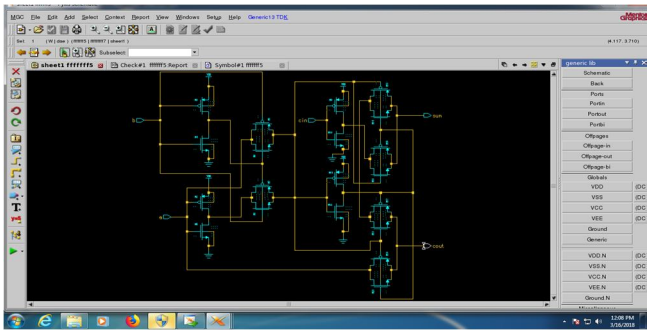
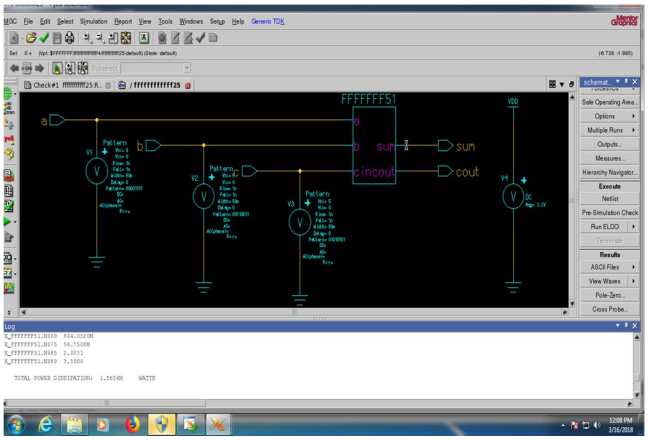
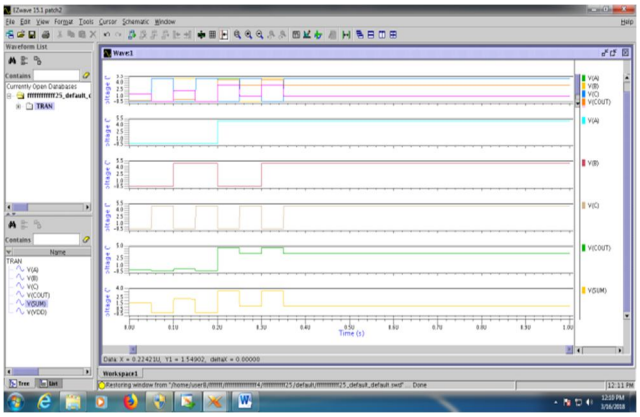


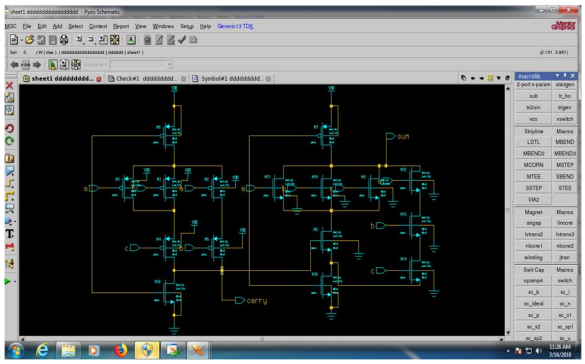
Fig (5) :Transmission gate Full adder circuit diagaram



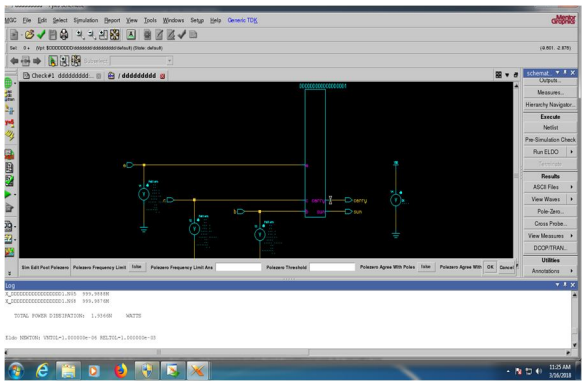
Fig(6) : Power dissipation of Transmission gate Full adder



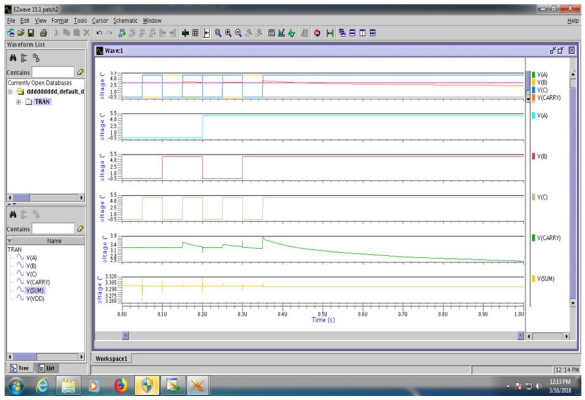
Fig(7) :waveforms of Transmission gate Full adder



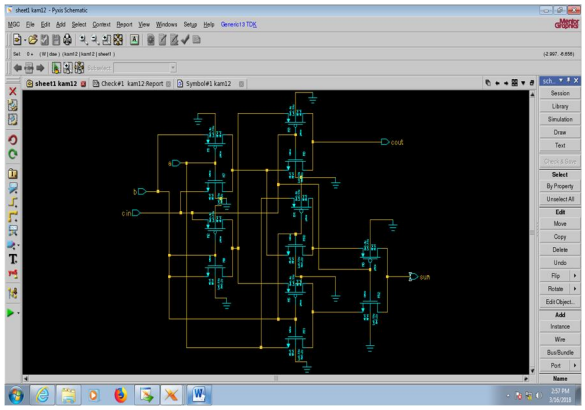
Fig(8) :Conventional Dynamic Full adder circuit diagarm



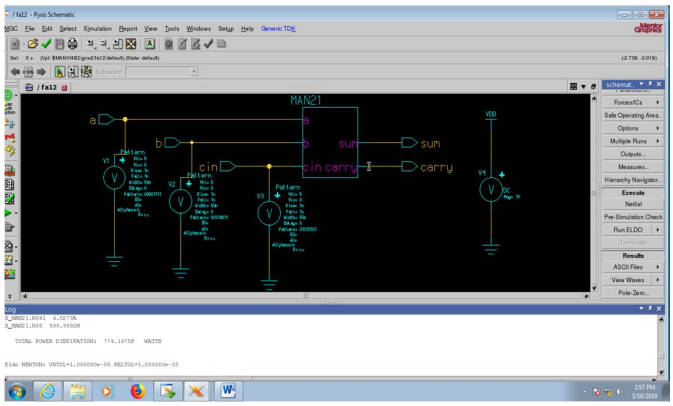
Fig(9) :Power Dissipation Conventional Dyanamic Full adder



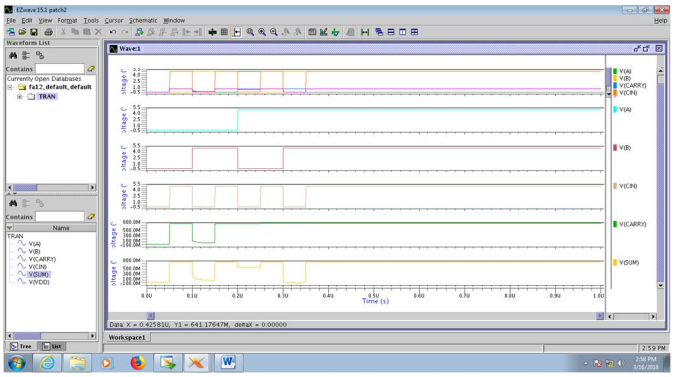
Fig(10) :Wave forms of Conventional Dynamic Full adder



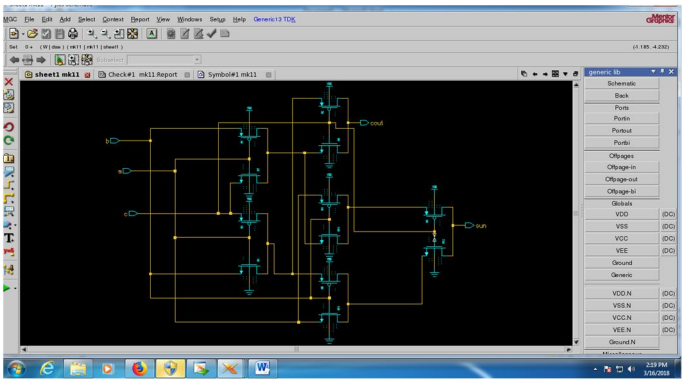
Fig(11) :14T Full adder circuit diagaram



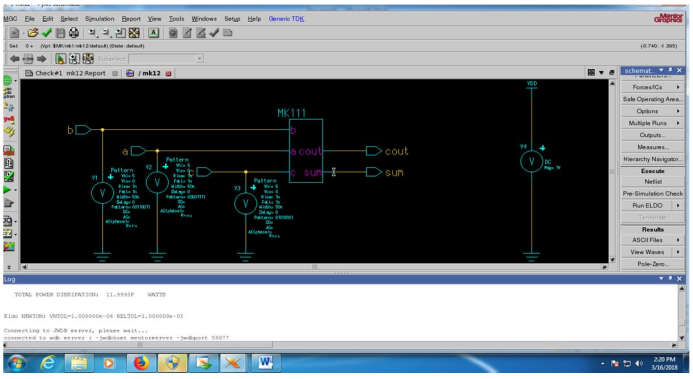
Fig(12) :Power dissipation of 14T Full adder



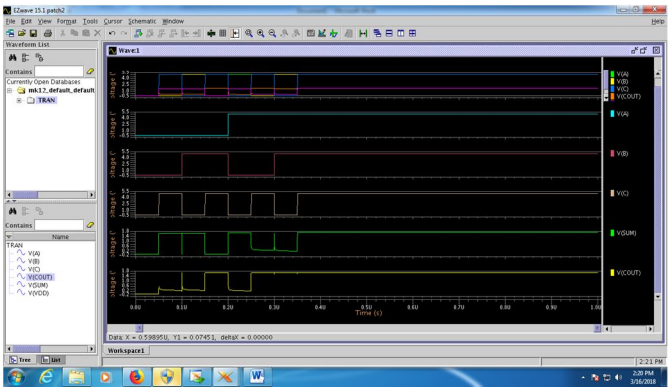
Fig(13) :waveforms of 14T Full adder



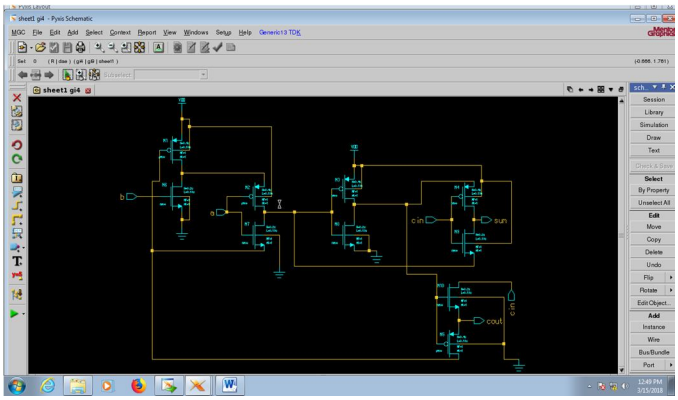
Fig(14) :Circuit diagram of 12T Full adder



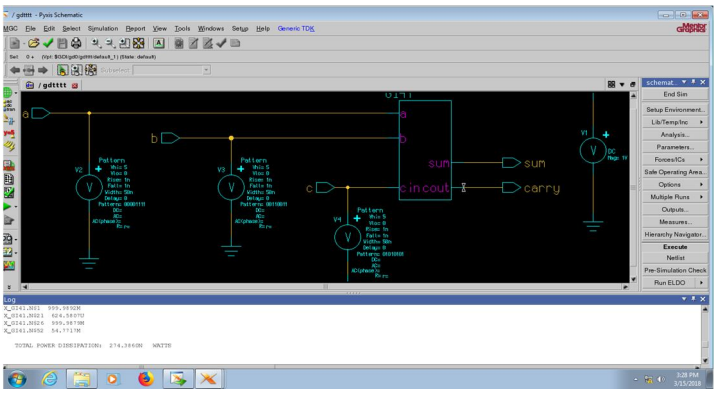
Fig(15) :Power dissipation of 12T Full adder



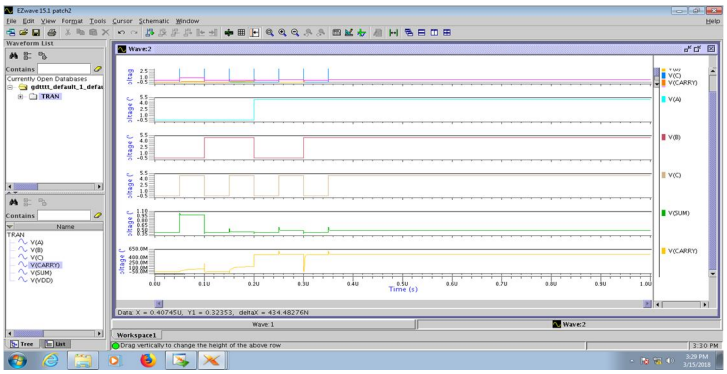
Fig(15) :waveforms of 12T Full adder



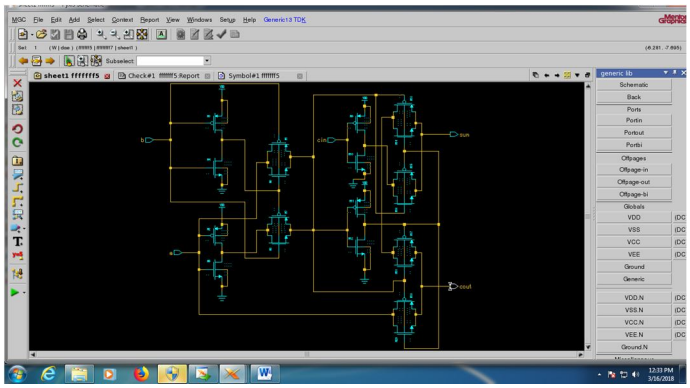
Fig(16) :GDI structure based Full adder circuit diagram



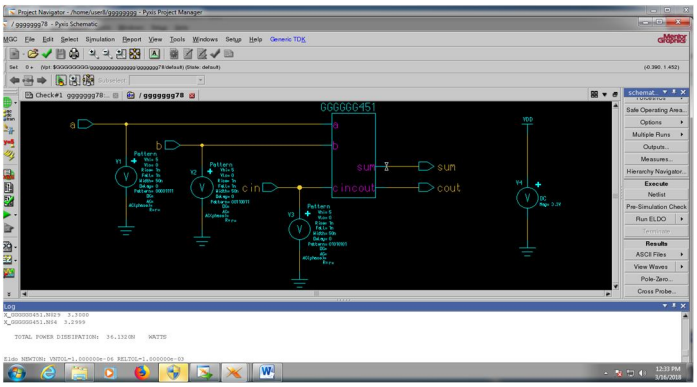
Fig(17) :Power dissipation of GDI structure based Full adder



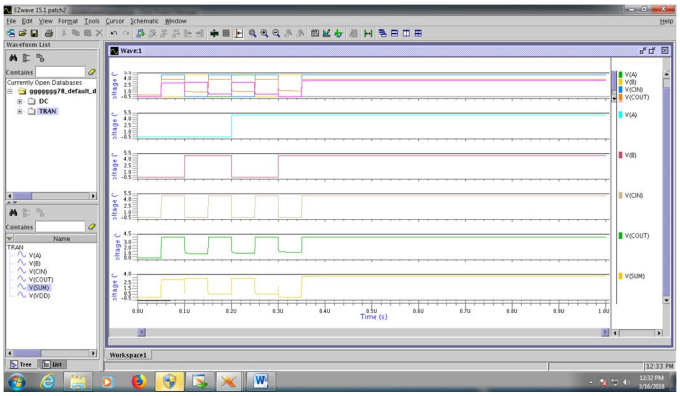
Fig(18) :Wave forms of GDI structured based Full adder



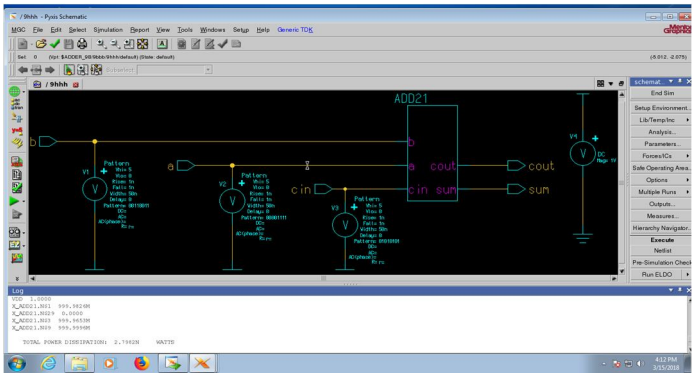
Fig(19) :Adder 9B circuit diagaram



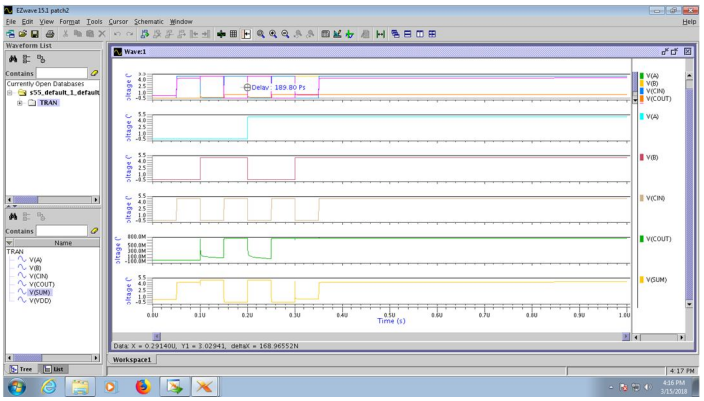
Fig(20) power dissipation of Adder 9B



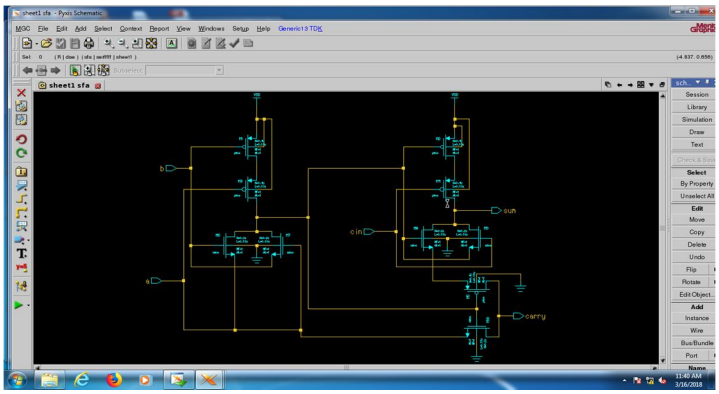
Fig(21) Wave forms of Adder 9B



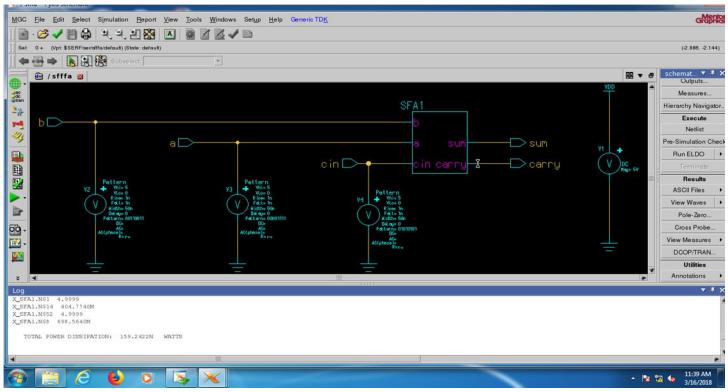
Fig(22) :Power dissipation of Adder 9A



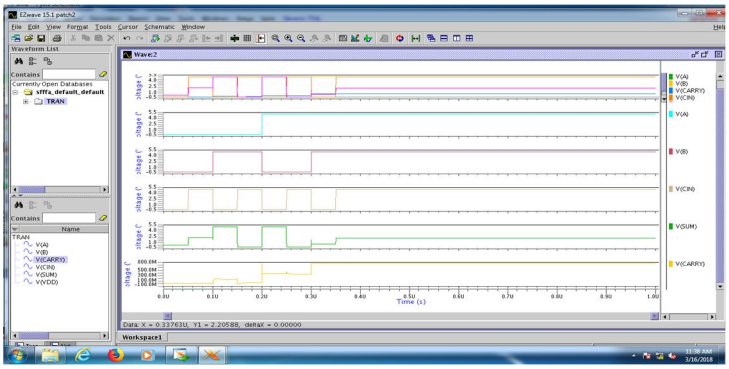
Fig(23) wave forms of Adder 9B



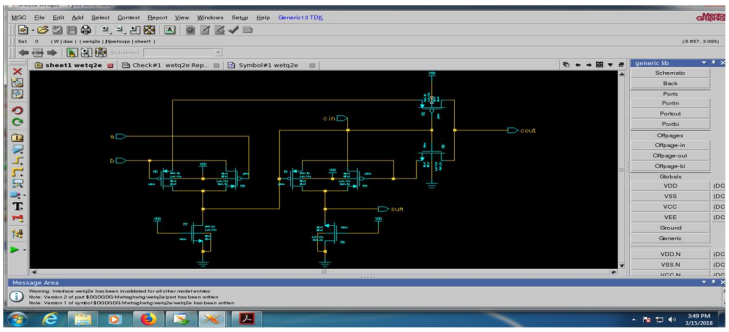
Fig(24) :SERF Full adder circuit diagaram



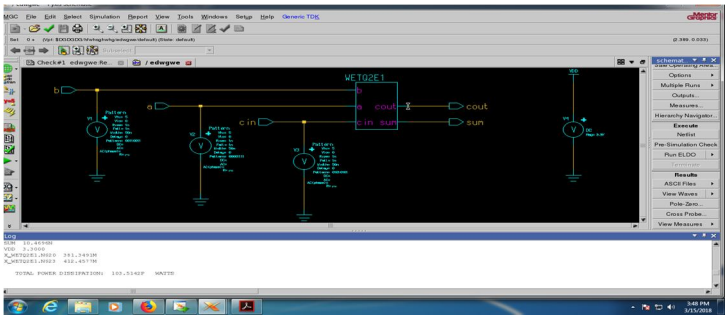
Fig(25) :Power dissipation of SERF Full adder



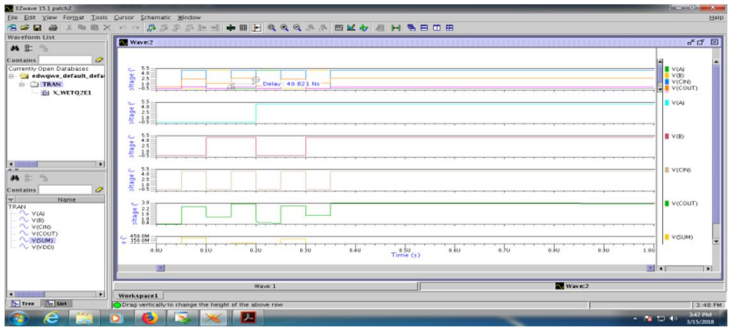
Fig(26) :Wave forms of SERF Full adder



Fig(27) :8T Full adder circuit diagram



Fig(28) :Powerdissipation of 8T Full adder



Fig(29) : Wave forms of 8T Full adder

Power dissipation table for different types of Full adders:

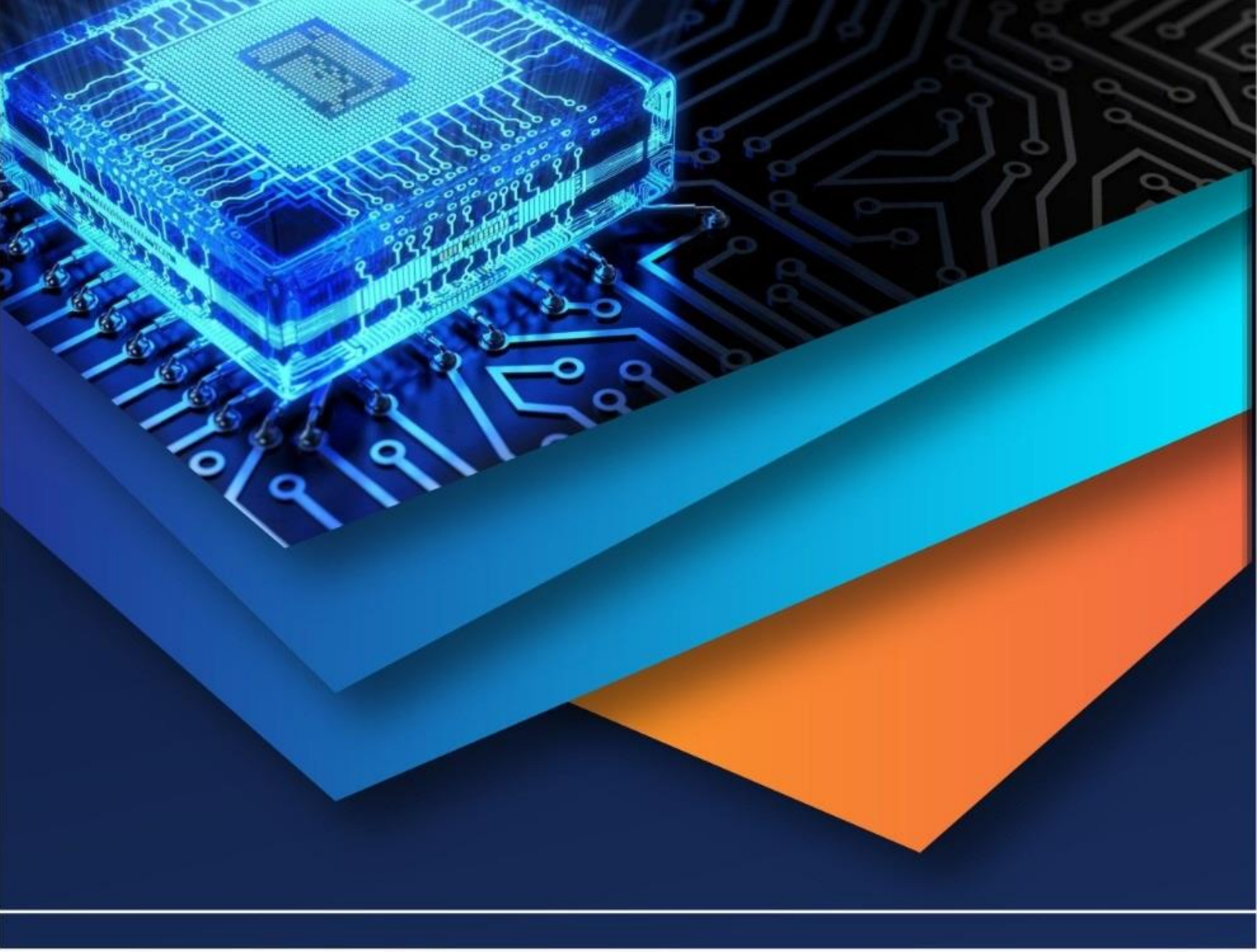
S.NO	DESIGN	NO.OF TRANSISTORS	POWER(NW)
1	28T conventional CMOS full adder	28	27.5204
2	Transmission gate full adder	26	1.5656
3	Conventional dynamic full adder	16	1.9366
4	14T full adder	14	0.7741975
5	12T full adder	12	11.99929
6	GDI structure based full adder	10	274.3860
7	Adder 9B	10	36.1320
8	Adder 9A	10	2.7982
9	SERF full adder	10	159.2422
10	8T full adder	8	0.10351423

IV. CONCLUSION

From the analysis of the above various types of Full Adder Circuits we can concluded that the power dissipation is less for 8T full adder and high for GDI Structure based full adder. We finally analyze that if the no.of transistors and power dissipation of Full adders is reduced then the size as well as power consumption of ALU is also reduced. Based on the applications, by using these full adders, we can design low power area efficient ALU'S. Today all the VLSI circuits performs on low power with high speed. The arithmetic and logic unit operations are essential behavior for low power high speed application like digital signal processing, microprocessor, VLSI, microcontroller,ASIC, etc.This paper presents the implementation of various type of Full Adders using CMOS 130nm and concluded that the dual rail domino logic based full adder circuit is fit for power dissipation.

REFERENCES

[1] Chandrakasan, R. Brodersen, ―Low Power Design‖, Kluwer Academic Publishers, 1995.
[2] A. M. Shams, and M. A. Bayoumi, ―A Novel High Performance CMOS 1-Bit Full Adder Cell‖, IEEE Transactions on Circuit and System, vol.47, NO. 5,May, 2000.
[3] J. H. Kang and J. B. Kim, ―Design of a Low Power CVSL Full Adder Using Low-Swing Technique‖, ICSE2004 Proc. 2004, Kuala Lumpur, Malaysia.
[4] A. A. Khatibzadeh and K. Raahemifar, ―A Study and Comparison of Full Adder Cells based on the Standard Static CMOS Logic.‖, IEEE CCECE 2004 - CCGEI 2004, Niagara Falls, May 2004.
[5] S. Goel, A. Kumar, M. A. Bayoumi, "Design of Robust, Energy-Efficient Full Adders for Deep-Submicrometer Design Using Hybrid-CMOS Logic", IEEE Transactions on VLSI 2006
[6] J. F. Lin, Y. T. Hwang, M. H. Sheu and C. C. Ho, "A novel High-Speed and Energy Efficient 10-Transistor Full Adder Design", IEEE Transactions on Circuits and System—I: Regular Papers, VOL. 54, NO. 5, May 2007.
[7] I. Hassoune, D.Flandre, I. O'Connor and J. D. Legat, "ULPFA: a new efficient design of a power aware full adder", IEEE Transactions on Circuits and Systems I-5438, 2008.
[8] Moradi, Dag. T. Wisland, Hamid Mahmoodi, Snorre Aunet, Tuan Vu Cao, Ali Peiravi,"Ultra Low Power Full Adder Topologies", IEEE-2009.
[9] Hung Tien Bui, Yuke Wang, Ying Tao Jiang,"Design and Analysis of low power 10 transistor Full Adder using Novel Xor and Xnor Gates", IEEE Transactions on Circuits and Systems, Vol. 49, January 2012.
[10] Raju Gupta, Satya Prakash Pandey, Shyam Akashe, Abhay Vidyarthi,"Analysis and Optimization of Active Power and Delay of 10T Full Adder using Power Gating Technique at 45nm Technology", IOSR Journal of VLSI and Signal Processing (IOSR-JVSP), Vol. 2, pp. 51-57, April 2013.
[11] Jatinder Kumar, Praveen Kaur,"Comparative Performance Analysis of Different CMOS Adders using 90nm and 180 nm Technology", International Journal of Advanced Research in Computer Engineering and Technology, Vol. 2, August 201
[12] Nidhi Tiwari, Ruchi Sharma, Rajesh Parihar, "Implementation of Area and Energy efficient Full Adder cell", IEEE International Conference on Recent advances and Innovations in Engineering (ICRAIE-2014), May 2014.
[13] Namrata V.Bhadade, Amol k.Boke,"Design and Analyse high speed, power efficient Full adder using Digital Logic Technique", IJAICTE, Vol. 1, Issue 7, November 2014
[14] M. Taheri, N. Shafiee, M. Esmaeildoust, Z. Amirjamshidi, R. Sabbaghi-nadooshan, K. Navi**A high speed residue-to-binary converter for balanced 4-moduli set** J. Comput. Secur., 2 (1) (2016), pp. 43-54



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