iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 6 **Issue:** IV **Month of publication:** April 2018

DOI: http://doi.org/10.22214/ijraset.2018.4053

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 6.887
Volume 6 Issue IV, April 2018- Available at www.ijraset.com

Design of Fault Tolerant Full Adder and Full Subtractor

Rita Mahajan[1], Sharu Bansal[2], Deepak Bagai[3]
[1, 2, 3] *Department of Electronics and Communication Engineering, Punjab Engineering College, Chandigarh, India*

Abstract: ***Now days, the complexity of integrated circuits is increasing while reliability of the components is decreasing due to small gates and transistor. One of the impacts of technology scaling is more sensitivity to transient and permanent faults. So, fault tolerant system plays important role in critical application where immediate human action is not possible. For reliable and efficient operation of a system, the detection of the transient fault is necessary. It is very difficult to detect these faults offline. The fault tolerant circuits can detect the faults and tolerate the detected faults. There are many fault tolerant full adder and full subtractor which can detect these faults online. So, an efficient fault tolerant design is proposed for full adder and full subtractor in this paper which can detect the faults with their exact location and also tolerate the faults. The proposed designs can detect the faults in single and multi net. The design has less area overhead and has less power requirements as compared to the previous techniques.***

Keywords: DFT (design for testability), double fault, Fault tolerance, Full adder, Full subtractor, Single fault

I. INTRODUCTION

With technology advancement, the complexity of circuit increases which results to increase the occurrence of the faults. The presence of these faults can destroy the functionality of overall system. Modern integrated circuits with smaller sizes are more prone to transient faults. The reason of these faults are electromagnetic noises, crosstalk and power supply noises. [1-3]. These faults can detect online by using the concept of design for design for testability and fault tolerance. Fault tolerant system performs two functions - detection and correction of the faults. The design can perform these functions with minimum hardware and area requirements [4-5]

Arithmetic operations are frequently used in VLSI circuits. Addition is a fundamental operation performed in many systems such as DSPs and microprocessor. Subtractor performs subtraction which is one of the arithmetic operations. Subtractor is also used in other parts of processor. Subtraction is carried out using adders in addition of some extra circuit like generating 2's complement of a number which is to be subtracted. There is a proposed design of adder and subtractor so that addition and subtraction can be carried out parallel which improves the performance of system. So, the design of faster and reliable adder and subtractor are of great importance in such systems. There are many approaches to achieve the fault tolerance in circuits. The researchers have introduced the concept of redundancy to detect the faults in circuits. But in order to detect and tolerate the faults there is need of an efficient fault tolerant full adder and full subtractor.

A. Fault Tolerance

Fault tolerance is the ability of the system to continue performing its functions even one or more its components have faults or failures. This capability of performing makes the system more software component. Implementation of fault tolerance technique depends on faults, design, configuration and application of the system. The faults can be of any type- hardware or software. In hardware faults mostly permanent, transient, stuck-at faults occur in the system. It is necessary to detect and repair these faults online. For detection and repairing the faults there is need of fault tolerant design which is reliable and have less area overhead and power requirements [6-7].

B. Redundancy

There are many approaches to design a fault tolerant system. The most common approach is redundancy. It is basically addition of resources beyond what is needed for normal system operation. In hardware redundancy, there is need of extra hardware to detect and tolerate the faults. The redundancy technique is N- modular redundancy [8]. For N = 2 there is DMR (double modular redundancy) in which one extra full adder or subtractor is used along with the original full adder or subtractor respectively to detect

the faults as shown in Fig.1. Outputs of both are compared by using XNOR gates and if they are not equal then it shows there is fault in the circuit. It has 200% area overhead requirements.

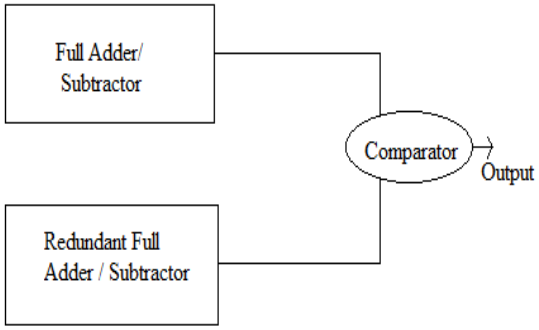


Fig.1. Double Modular Redundancy

Similarly for N = 3, TMR (triple modular redundancy) in which two redundant full adder or full subtractor is used along with the original full adder or full subtractor as shown in Fig.2. The output of three can be compared by using XNOR gates and if two generate the same output then the output of third also considered as faulty. A fault condition is there if output of any two modules is different from the third module. It also requires 300% area overhead. This technique can detect the faults but can't able to repair the faults [9]. So there is need of fault tolerant design which can detect and repair these faults.

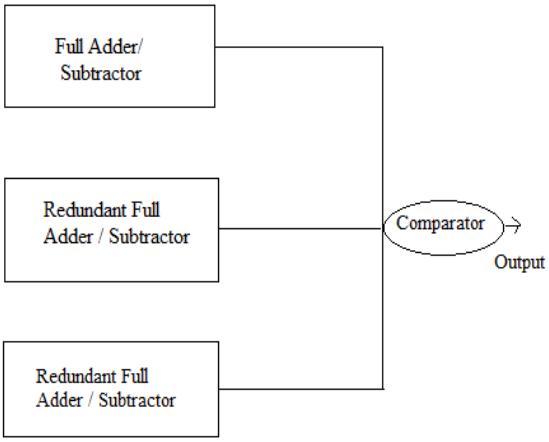


Fig.2. Triple Modular Redundancy

II. DESIGN OF FAULT TOLERANT FULL ADDER AND FULL SUBTRACTOR

In digital circuits, adder and subtractor are most important components used in various applications. Both are the combinational circuits which perform operations with three inputs. The fault tolerant circuits which are shown further have the ability to detect and correct the faults. Following are some design with can detect faults in adder and subtractor.

TABLE I
TRUTH TABLE OF ADDER WITH DFT FOR SINGLE FAULT

A	B	C_{in}	Sum	C_{out}	X1	F1	E_f
0	0	0	0	0	1	0	0
0	0	1	1	0	0	1	0
0	1	0	1	0	0	1	0
0	1	1	0	1	0	1	0
1	0	0	1	0	0	1	0
1	0	1	0	1	0	1	0
1	1	0	0	1	0	1	0
1	1	1	1	1	1	0	0

A. DFT (design for testability) for single fault

1) Full Adder

The author in [10] designed a self checking full adder as shown in Fig.3. The expressions for sum and carry out output bits are

Sum = $A \oplus B \oplus C_{in}$

$C_{out} = AB + AC_{in} + B C_{in}$

It requires single full adder, functional unit and two XNOR gate The XNOR gate X1 is used to compare sum and carry output and XNOR X2 is used to detect the faults by using the functional unit and gives the value of E_f. If the value of E_f is 0 then it shows there is no fault in the circuit, otherwise the circuit is faulty.

F1 = (A B C_{in} + A' B' C_{in}')'

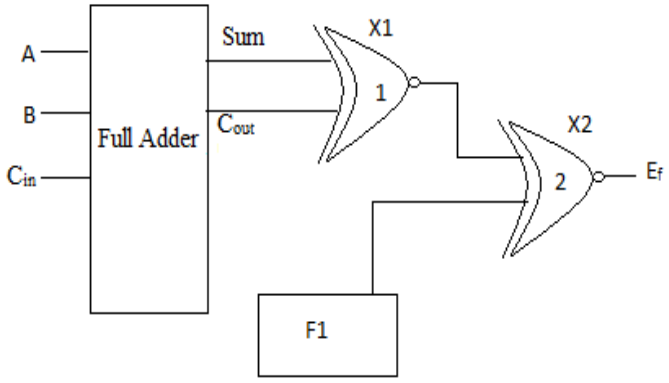


Fig.3. Full Adder with DFT for single fault

This design approach detects the single fault but not able to identify the location of fault and also not able to detect the double faults.

2) Full Subtractor

The expressions for difference and borrow out are shown below. Here, we have to calculate the value of diff (difference) and bout (borrow out) from the inputs A, B and B_{in} (borrow-in).

diff = $A \oplus B \oplus B_{in}$

$b_{out} = A' B + A' B_{in} + B B_{in}$

TABLE II

TRUTH TABLE OF SUBTRACTOR WITH DFT FOR SINGLE FAULT

A	**B**	**B_{in}**	**Diff**	**b_{out}**	**X1**	**F1**	**E_f**
0	0	0	0	0	1	0	0
0	0	1	1	1	1	0	0
0	1	0	1	1	1	0	0
0	1	1	0	1	0	1	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	1	0	0	0	1	0	0
1	1	1	1	1	1	0	0

The proposed full subtractor can be tested for faults by using the functional unit F1 as shown in Fig.4 and we have to compute the logic for functional unit and the expression for this

F1 = A B' B_{in}' + A' B Bin

By using this functional unit and two XNOR gates (X1 and X2) as shown in fig.4 we can find that the circuit works under fault free condition or not.

The gate X1 is used for XNOR operation of diff and b_{out}, gate X2 which gives final E_f is used to compare the value of X1 and F1 by the XNOR operation as given in equations.

$X1 = (diff \oplus b_{out})'$

$E_f = (X1 \oplus F1)'$

If the value of E_f is 0 then it shows there is no fault in the circuit. On the other hand if E_f is 1 then fault will be indicated. In this way, the design can detect the single fault in single net. The fault which is detected can be either in diff or bout output. The design also decreases the area overhead as compared to the previous approaches TMR and DMR.

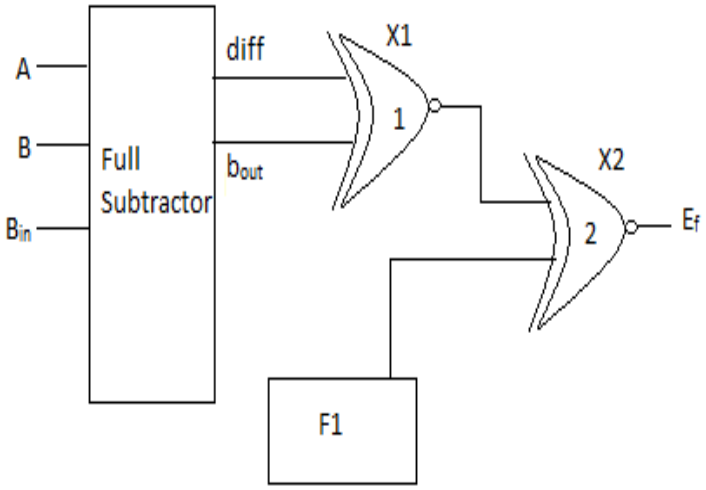


Fig.4. Full subtractor with DFT for single fault

B. DFT (design for testability) for double fault

1) Full Adder

The author in [11] proposed a self checking adder which can detect the faults. There is another proposed fault tolerant adder having different functional unit F1 as shown in Fig.5. It can be proposed by using one XOR, four XNOR gates and functional unit. The gate X1, X2 are used to detect the fault in sum output bit and the gate functional unit F1, gate X3 are used to detect the fault in C_{out} output bit. The gate X4 and X5 gives the final outputs F_s and F_c.

$X1 = A \oplus Cin$

$X2 = (Sum \oplus B)'$

$X3 = (C_{out} \oplus B)'$

$F1 = A\ B'\ C_{in} + A'\ B\ C_{in}'$

$F_s = (X1 \oplus X2)'$

$F_c = (X3 \oplus F1)'$

TABLE.III

TRUTH TABLE OF ADDER WITH DFT FOR DOUBLE FAULT

A	B	C_{in}	Sum	C_{out}	X1	X2	X3	F1	F_s	F_c
0	0	0	0	0	0	1	1	0	0	0
0	0	1	1	0	1	0	1	0	0	0
0	1	0	1	0	0	1	0	1	0	0
0	1	1	0	1	1	0	1	0	0	0
1	0	0	1	0	1	0	1	0	0	0
1	0	1	0	1	0	1	0	1	0	0
1	1	0	0	1	1	0	1	0	0	0
1	1	1	1	1	0	1	1	0	0	0

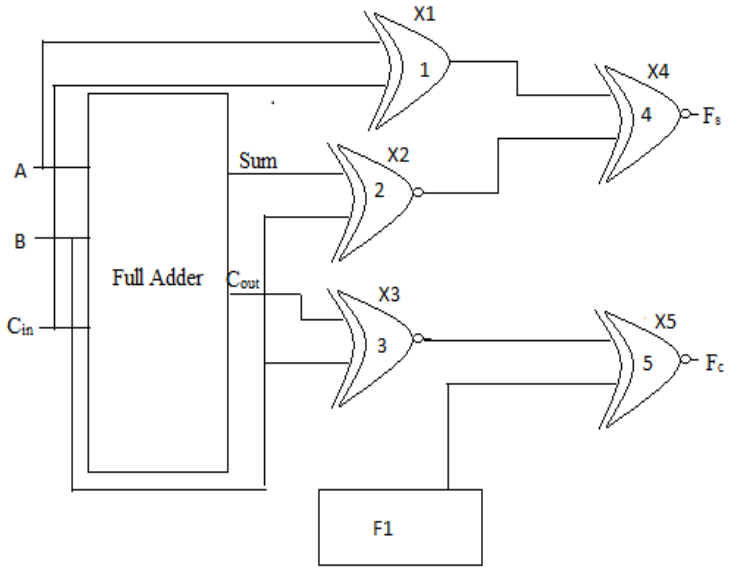


Fig.5. Full Adder with DFT for double fault

In this design, if Fc and Fs is 0 then it indicates fault free condition and if it shows 1 then there is fault in the circuit.

2) Full Subtractor

Now there is a proposed design of full subtractor is shown in Fig.6 which can detect single and double fault occur at a time and also capable of identifying the location of the fault. The diff and bout output bits are verified individually to make the design more efficient and reliable. It also reduces the hardware cost as compared to various previous approaches.

In the design, by using one XOR gate, four XNOR gate and one functional unit we can find whether the circuit works under fault free condition or not. The gate X1, X2 are used to detect the fault in diff bit and the gate functional unit F1, gate X3 are used to detect the fault in bout bit. The gate X4 and X5 gives the final outputs F_d and F_b. The expressions for all gates and functional unit are shown in following equations:

TABLE IV
TRUTH TABLE OF DFT FOR DOUBLE FAULT

A	B	Bin	diff	b_{out}	X1	X2	X3	F1	F_d	F_b
0	0	0	0	0	0	1	1	0	0	0
0	0	1	1	1	1	0	0	1	0	0
0	1	0	1	1	0	1	1	0	0	0
0	1	1	0	1	1	0	1	0	0	0
1	0	0	1	0	1	0	1	0	0	0
1	0	1	0	0	0	1	1	0	0	0
1	1	0	0	0	1	0	0	1	0	0
1	1	1	1	1	0	1	1	0	0	0

$X1 = A \oplus Bin$

$X2 = (diff \oplus B)'$

$X3 = (b_{out} \oplus B)'$

$F1 = A' B' Bin + A B B_{in}'$

$F_d = (X1 \oplus X2)'$

$F_b = (X3 \oplus F1)'$

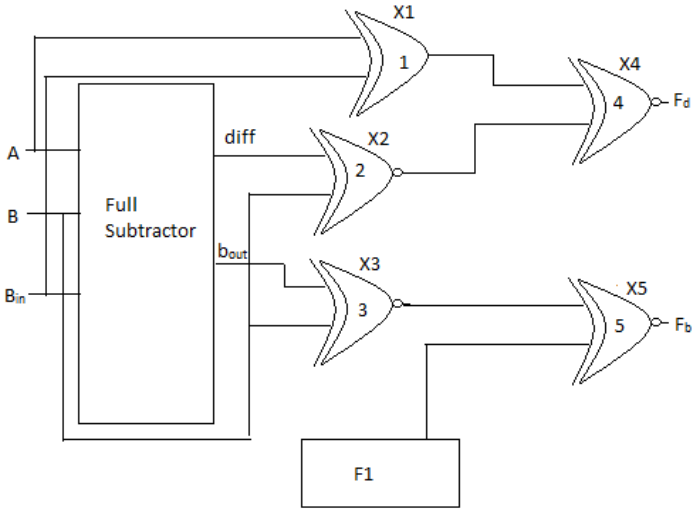


Fig.6. Full subtractor with DFT for double fault

The fault can be detected in diff and bout output bits in the form of F_d and F_b. If the value of F_d is 0 then there is no fault in difference bit and if it is 1 then it indicates the faulty condition. Similarly if value of F_b is 0 then borrow out bit is also fault free otherwise borrow out bit of full subtractor is faulty.

C. Fault tolerant full adder and full subtractor

The fault tolerant design is used for repairing the faults which are detected during testing process. The design can repair single and the double faults. The author in [11] designed a self repairing circuit to repair the faults in adder. In fig.7 there is tolerant circuit in which value of Sum/diff output bit is selected by the multiplexer under the control of F_s/F_d and value of C_{out}/b_{out} is also selected by the multiplexer according to F_c/F_b bit. If value of F_s/F_d is 0 then Sum/diff output bit is selected by the multiplexer and If F_s/F_d is 1 then multiplexer selects the inverted value of Sum/diff output. Similarly If value of F_c/F_b is 0 then C_{out}/b_{out} output bit is selected by the multiplexer and If F_c/F_b is 1 then multiplexer selects the inverted value of C_{out}/b_{out} output.

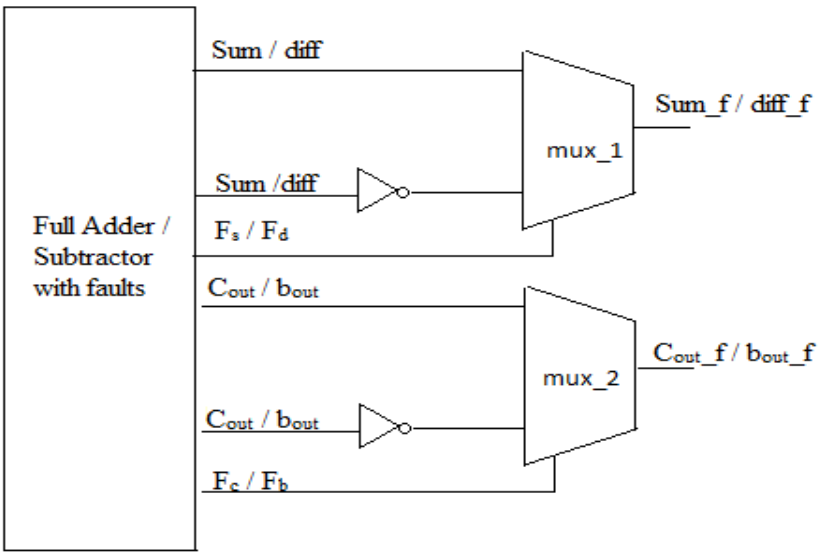


Fig.7. Fault tolerant full adder and full subtractor

III.SIMULATIONS RESULTS AND COMPARISON OF TECHNIQUES

A. Simulation Results

The designs with DFT for single fault can detect only one fault. The fault in final output can be indicated in form of E_f. If the value of E_f is high then the circuit is faulty. The output waveform fault free full adder and faulty full adder are shown in fig.8 and fig.9.

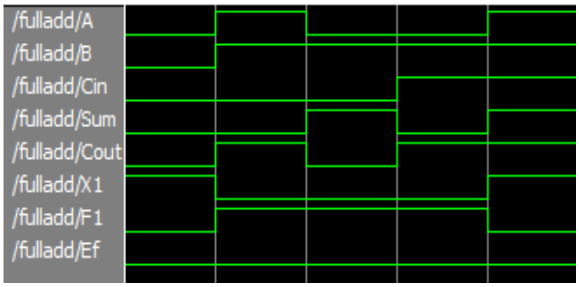


Fig.8. Output Waveform of fault free full adder for single fault

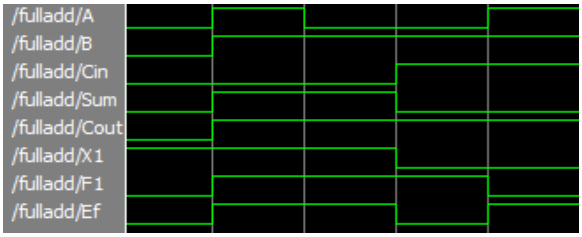


Fig.9. Output Waveform of faulty full adder for single fault

The output waveform fault free full subtractor and faulty full subtractor are shown in fig.10 and fig.11.

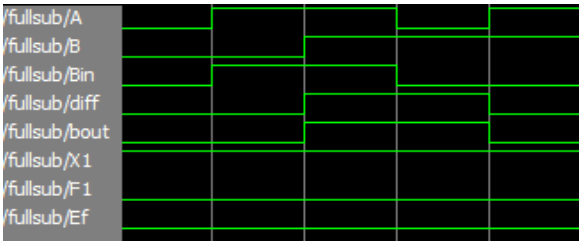


Fig.10. Output Waveform of fault free Full subtractor for single fault

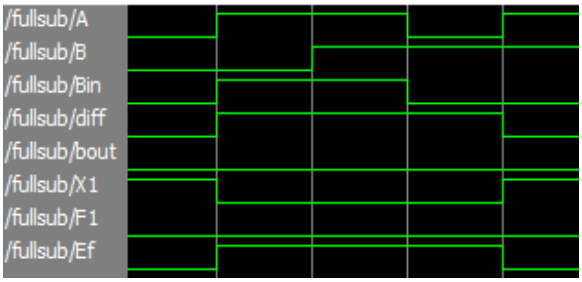


Fig.11. Output Waveform of faulty full subtractor for single fault

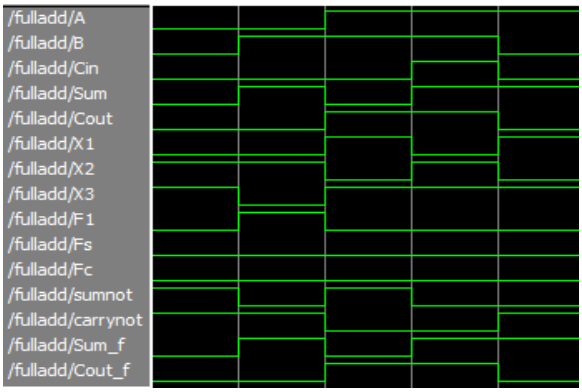


Fig.12. Output Waveform of fault free full adder for double fault

ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 6.887
Volume 6 Issue IV, April 2018- Available at www.ijraset.com

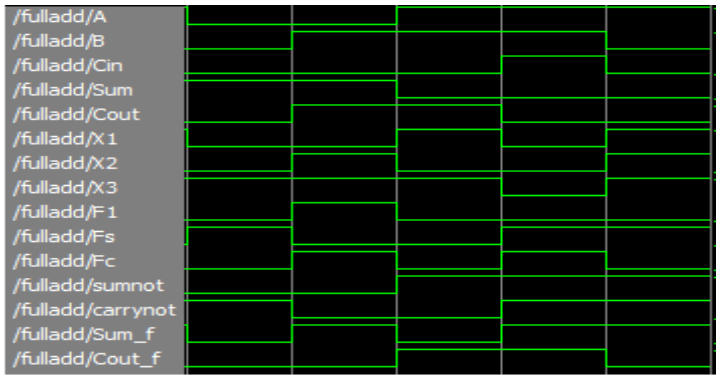


Fig.13. Output Waveform of faulty full adder for double fault

The fault tolerant design with DFT for double fault can detect single and double faults in multiple nets. The final output are in terms of F_s/F_d and F_c/F_b .If both values are low then there is no fault and if any one of them or both are high then the circuit is faulty and the fault which is detected can be corrected by the repairing circuit. The output waveforms are shown in fig.12 and fig.13 for full adder.

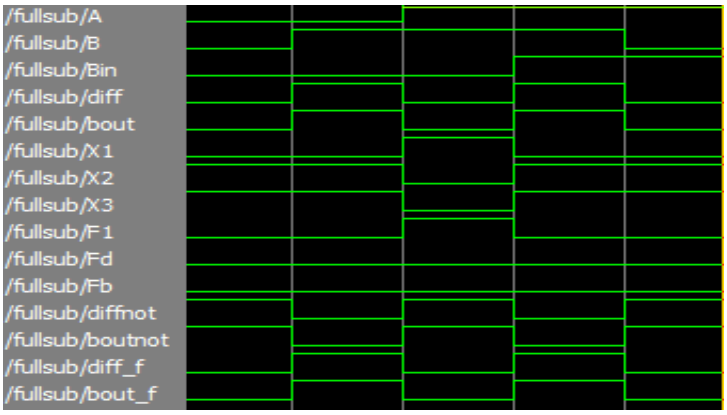


Fig.14. Output Waveform of fault free full subtractor for double fault

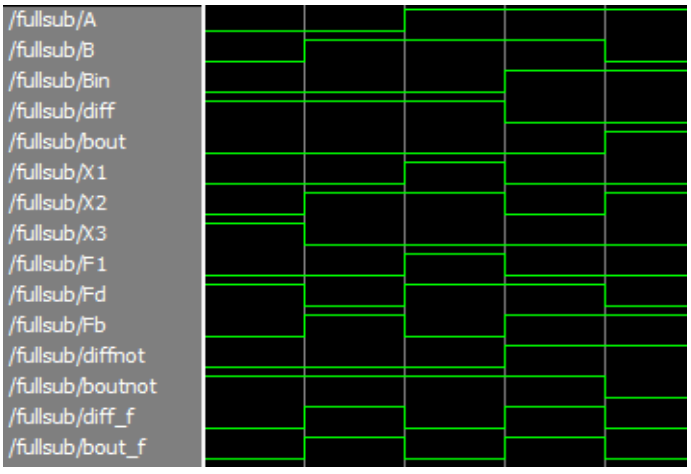


Fig.15. Output Waveform of faulty full subtractor for double fault

B. Comparison of different techniques

There is comparison of proposed designs with the existing approaches like DMR and TMR on the basis of fault detected, conditions and fault tolerated which is shown in Table V. According to the designs internal structure there is comparison of various approaches on the basis of cell used, input-output ports, nets and gates which is shown in Table VI.

TABLE V.
COMPARISON ON THE BASIS OF FAULT DETECTION, TOLERANCE AND POWER

	DMR	TMR	DFT with single fault	DFT with double fault
Faults detected	Single fault	Single fault	Single fault	Single fault and Double fault
Conditions	Output = 0 -fault free Output = 1 - faulty	Output = 0 -fault free Output = 1 - faulty	E_f =0 - fault free E_f =1 - faulty	F_d = 0 and F_b =0 - fault free F_d = 1 and F_b =0 - fault in diff output F_d = 0 and F_b =1 - fault in b_{out} output F_d = 1 and F_b =1 - fault in both output
Tolerance	Possible with double area overhead	Possible with triple area overhead	Possible with less area overhead	Possible with very less area overhead
Power	0.242 W	1.081 W	0.242 W	0.593 W

TABLE VI.
COMPARISON ON THE BASIS OF INTERNAL STRUCTURES

	DMR	TMR	DFT with single fault	DFT with double fault
Cells	8	11	6	11
I/O ports	5	5	4	5
Nets	13	17	10	15
Gates	16	23	17	20

IV. CONCLUSIONS

In this paper, firstly a fault generated by a circuit is detected by the design of full subtractor with DFT for single fault. But this design is not able to detect more than one fault. Then the circuit with DFT for double fault is designed with can detect single and double fault and capable of identifying the exact location of the fault. Then fault tolerant circuit is designed which can repair the detected faults. The design provides the higher error detection and correction capabilities. This design has less area overhead as compared to the existing designs and has less power requirements.

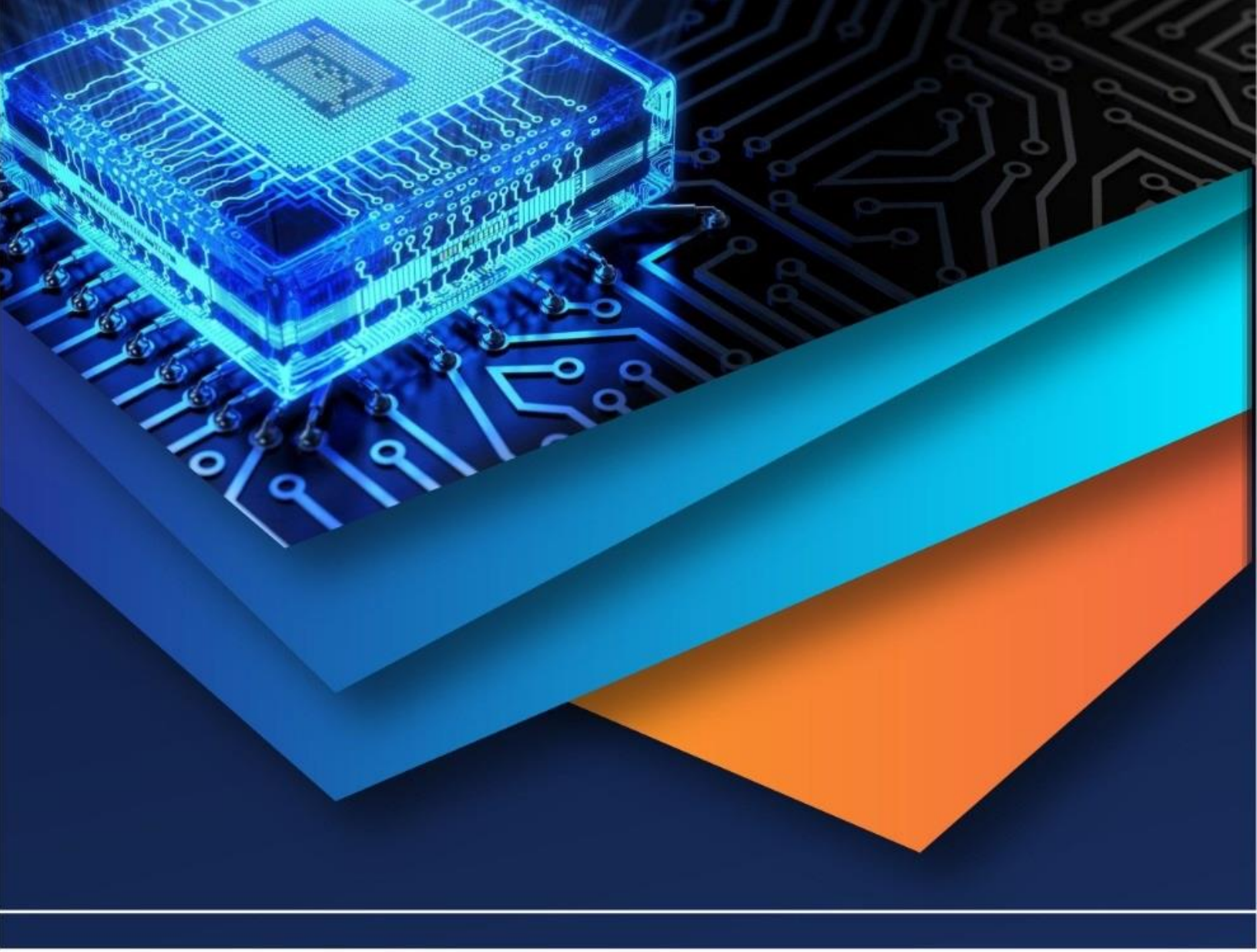
V. ACKNOWLEDGMENT

The paper wishes to acknowledge Rita Mahajan who is Assistant Professor in Punjab Engineering College, Chandigarh, Sector 12, India. She is working in Department of Electronics Engineering and Sharu Bansal is ME student in Punjab Engineering College, Chandigarh, Sector 12, India. She is a student in Department of Electronics Engineering and pursuing her ME in VLSI Design and also Deepak Bagai who is professor in Punjab Engineering College, Chandigarh, Sector 12, India. He is working in Department of Electronics Engineering

REFERENCES

[1] Meixner A, Bauer ME, Sorin DJ. Argus: "low-cost, comprehensive error detection in simple cores", IEEE/ACM international symposium on micro architecture; 2007
[2] M. Valinataj, "A novel self-checking carry look ahead adder with multiple error detection/correction", Microprocessors and Microsystems Vol. 38 No .8 pp. 1072–1081, October 2014.
[3] P. Oikonomakos, P. Fox, Error correction in arithmetic operations by I/O inversion, in: 12th IEEE Int. On-Line Testing Symposium (IOLTS), 2006, pp. 287–292.
[4] D.P. Vasudevan, P.K. Lala, J.P. Parkerson, "Self-checking carry-select adder design based on two-rail encoding", IEEE Transaction on Circuits and Systems- I Regul.ar Paper Vol. 54, No.12, 2696–2705, December 2007.
[5] C.D. Martinez, L.D. Bollepalli, D.H. Hoe, "A fault tolerant parallel-prefix adder for VLSI and FPGA Design" IEEE Southeastern Symposium on System Theory (SSST), March 2012.

[6] S. Ghosh, K. Roy, “Novel low overhead post-silicon self- correction technique for parallel prefix adders using selective redundancy and adaptive clocking, IEEE Transaction on Very Large Scale Integration (VLSI) Systems, Vol. 19, No. 8, pp 1504–1507, August 2011.
[7] M. H. Hajkazemi, A. Baniasadi, H. Asadi, “FARHAD: a fault-tolerant power-aware hybrid adder for add intensive applications,” International Conference on Application-Specific Systems, Architectures and Processors (ASAP), 2013
[8] P. Reviriego, C.J. Bleakley, J.A. Maestro, "Diverse double modular redundancy: a new direction for soft-error detection and correction", IEEE Des. Test. Vol. 30, No. 2 pp. 87–95, April 2013.
[9] M. Nicolaidis, "Time redundancy based soft-error tolerance to rescue nanometer technologies", IEEE VLSI Test Symposium, 1999.
[10] M.A. Akbar, J.-A. Lee, "Self-repairing adder using fault localization", Microelectronics Reliability, Vol. 54, No. 6, pp. 1443–1451, October 2014.
[11] Pankaj Kumar, Rajender Kumar," Real Time Fault Tolerant Full Adder Design for critical application", Engineering Science and Technology, an International Journal, Vol.19 , 1465-1472, May 2016.
[12] Pankaj Kumar, Rajender Kumar," Double fault tolerant full adder design using fault localization", International Conference on Computational Intelligence & Communication Technology (CICT), Feb 2017



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY