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A Brief Review of SRAM Architecture with Various Low leakage Power Reduction Technique in Recent CMOS Circuit

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***Abstract*— In the integrated circuits that have memories, a major share of total circuit power is required by the memory architecture of the circuit. With the day-to-day changing circuit designs, the need to store increasing amount of processing data has resulted in the growing memory size in an integrated circuit. Most of the memory data remains un-altered during the memory data handling operation. The stored data is thus affected by the sub-threshold leakage power / current that leads to the degradation of data signal quality. The data integrity is maintained using a feedback path / architecture in SRAM memory architecture. Still, the amount of power loss due to leakage contributes a major part of the total power loss of the integrated circuit. This loss increases with the decrease in the physical feature size of the component / transistors. A low power system offers the benefits like device portability, long battery life, good performance criteria, etc. Today's increasing data handling require more random access memory to process the dynamic data. In memories and also in processing and data handling operations low power dissipation is desired from the operational circuits. This survey paper use the design of SRAM architecture to reduce the leakage current and hence the leakage power. The various leakage power reduction techniques have been evolved to tackle the problem and it is still in progress. In this paper mainly, the study of various leakage power reduction technique with SRAM architecture in fab Technology. In this review paper latest work done on a new technique called LECTOR (Leakage Control Transistor Technique) is explained here.**

***Keywords* — CMOS, Dynamic Power, Leakage Control Transistor, SRAM, Sub-threshold Leakage Current, Threshold Voltage.**

I. INTRODUCTION

The basic requirement of any Integrated Circuit is high speed and low power processing of the data signals to perform the desired execution. The minimization of feature size plays an important role in increasing the performance of integrated circuits. But the feature minimization inversely affects the percentage of leakage current when compared to the total current requirement of the circuit. The main causes of the dissipation of power are: 1) short-circuit current, 2) load capacitance charging and discharging current, and 3) transistor leakage current in the sub-threshold operating condition. The data value transition activity during memory data processing is the main cause of short circuit power dissipation. There are various proposed techniques to reduce the short circuit current dissipation but at the cost of extra control and monitoring circuit. This additional circuit further contributes in the dissipation of power. The improving semiconductor processing techniques have made it possible to reduce the size of memories leading to a higher density of memory elements per square unit of area. This has also contributed in decreasing the power dissipation by reducing the load charging and discharging current due to smaller size of the parasitic capacitance of the load capacitors. The leakage current is more effective in deep sub-micron technologies. A number of leakage reduction techniques have been proposed in previous works like leakage lector technique, feedback approach, stack approach, force stack technique, sleep approach, sleeper keeper technique, zigzag approach, etc. The ensuing chart explains about how much of leakage power increases when Technology Scales down. There are two operational modes and various leakage reduction technique based on these operational modes and these operational modes are used in applications like portable mobile multimedia. The two operational modes are classified as:

A. Standby Mode

When the circuit is cut off from the rails and when the CMOS circuit in idle state.

B. Active Mode

Leakage current and leakage power is reduced during the runtime by stacking the transistor.

For example, Mobile phone have low activity factor their idle time is larger when comparing with the device in active time. In idle time also these devices are affected by the leakage power loss which reduces the battery life-time. For compete this different leakage power optimization technique are developed. Fig.1 shows the total power dissipation in various CMOS Technologies.

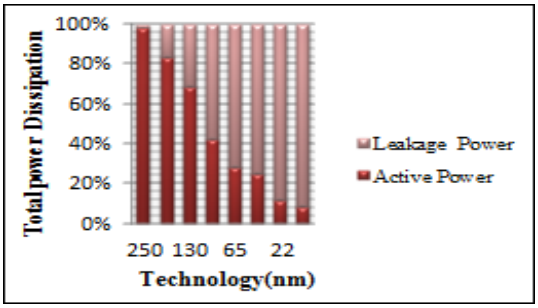

Fig. 1 Power Dissipation in various Technologies

C. Different Leakages in MOSFET Device

In a CMOS transistor there are four main sources of leakage current. The different leakages in MOSFET device shows in fig 2 are as follows:

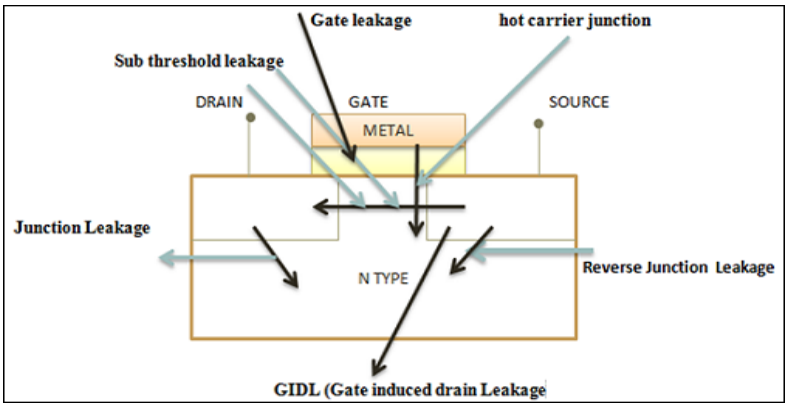

Fig. 2 Different Leakage Power Components in CMOS

1) P-N junction reverses bias current: The P-N Junction leakage current is due to the reverse biasing of the drain and source to well junctions or current can leak from source and drain into the well or substrate. Here large doping can cause Zener and band to band tunnelling The two main mechanisms of a reverse-bias P-N junction leakage are minority carrier diffusion near the edge of the depletion region and the other is due to electron-hole pair generation in the depletion region of the reverse-biased junction. It is a function of doping and junction area concentration. They are relatively minor contributor.

2) Weak inversion (Sub threshold Leakage Current): In sub threshold leakage current between source and drain the current 0 <Vgs <Vt. To make dynamic power dissipation under control, voltage supplied has to been scaled down the threshold voltage (Vth) has to be scaled too, to maintain a high drive current capability. The scaling of Vth results in increasing sub-threshold leakage currents. They are major contributor in leakage current of sources. The Sub threshold current occurs between drain and source when transistor is operating in weak inversion region, i.e., the gate voltage is lower than the Vth. The drain-to-source current is composed by drift current and diffusion current. The drift current is the superior mechanism in strong inversion regime, when the gate-to-source voltage exceeds the Vth. In weak inversion, the minority carrier concentration is almost zero, and the channel has no horizontal electric field but a small longitudinal electric field appears due the drain-to-source voltage. In this situation, the carriers move by diffusion between the source and the drain of MOS transistor. The sub threshold current is

superior by diffusion current and it depends exponentially on both gate-to-source and threshold voltage.

3) DIBL (Drain Induced Barrier Lowering): In this leakage source current, the current leaking between source and drain are the primary contributor. Their Source potential barrier lowered by high voltages on drain which is due to the depletion region of drain interacts with source and occurs near channel surface source injects carriers without gate playing a significant role . It is enhanced by short L*eff* effectively increases linear region current.

4) GIDL (Gate Induced Drain Leakage): The current leaking between drain and well or substrate. They are minority contributor High field effect in the drain junction of MOS Transistors is the cause for the Gate Induced Drain leakage. In the case of NMOS transistor important band bending in the drain makes generation of electron-hole pair, through avalanche multiplication and band to band tunnelling, when gate is grounded and drain potential is connected to VDD. Due to the reason of holes rapidly swept out, to the substrate, a deep depletion condition is developed. Meanwhile, due to the collection of the electrons in the drain GIDL current (IGIDL) is produced. Increase in drain to gate voltage and in drain to body voltage will make this leakage mechanism very worse.

5) Gate oxide tunnelling: As transistor length and supply voltage are scaled down, gate oxide thickness must also be reduced to maintain effective gate control over the channel region. Unfortunately this results in an exponential increase in the gate leakage due to direct tunnelling of electrons through the gate oxide.

6) Hot carrier injection: Their increased or decreased leakage current (DIBL, weak inversion, etc.) They minor but increasing contributor. Threshold offset caused by charge trapped in gate oxide.

II. SURVEY OF LEAKAGE POWER REDUCTION TECHNIQUES

A. Conventional 6-T SRAM Architecture

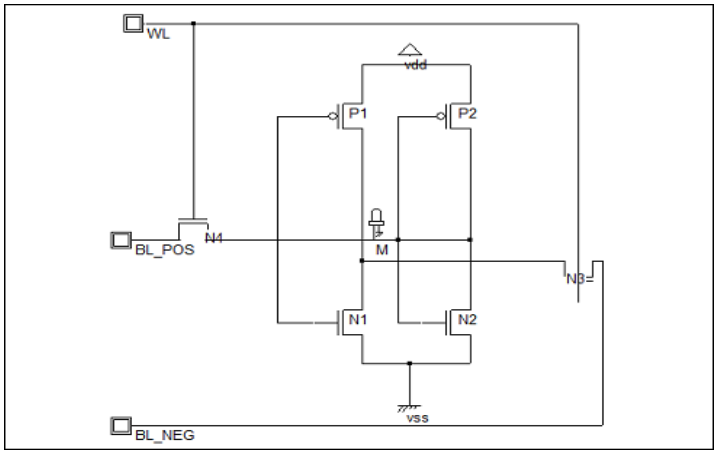

Fig. 3 Architecture of SRAM 6-T Cell

The conventional architecture of SRAM Cell has 6-transistors. It is shown in Fig-3. At deep sub-micron scale the leakage power of SRAM circuit is comparatively high as compared to the other operational circuits. The concept of SRAM architecture [2] is based on the stabilization of logic values to maintain its existence against any current or power loss with the ease of data modification using two feedbacks coupled CMOS Inverters. The output terminals of the two inverters act as internal load lines of the SRAM cell to store the memory data bit value on one of the internal load line and its complement logic value on the other internal load line.

1) *Write Operation:* The logic data bit to be written in a SRAM cell is provided on the BL_pos and its complement logic value is provided on BL_neg. The WL input is provided a logic high pulse on NMOS data access transistors to enable the transfer of charge from the data lines (BL_pos and BL_neg) to the SRAM cell internal circuit. The duration of pulse should be more than the duration in which the charge on BL_pos and BL_neg should get shared by the SRAM internal load lines to store

the desired logic value in the SRAM cell.

2) *Read Operation:* To read the data from the SRAM cell, logic high values are set on BL_pos and BL_neg. The WL input is provided a high pulse to enable the sharing of charge between the data lines, BL_pos and BL_neg, and the internal load lines. The data line (BL_pos or BL_neg) connected to the cell internal load line with logic value'1' will not show any change in the logic value after sharing of charge because of the same voltage on both the data lines. The other data line will be affected by a small change in its voltage value after sharing the charge with the cell internal load line. Since the current driving capacity of the cell is very low, the change sharing will have a small voltage change effect when logic '0' at the internal load line is shared with the logic '1' of the data line. This voltage difference developed in the load lines is measured using the sense amplifier circuit to know the logic value that is stored in the cell.

B. *Sleep Transistor Technique*

In this technique, the sleep transistors are used at two different positions. one is between the pull-up network and VDD, then the other is between the GND and the pull-down network.

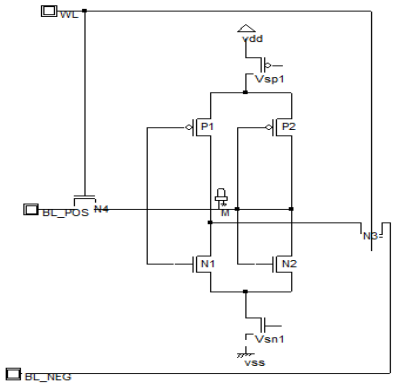

Fig. 4 SRAM Using Sleep Transistor Technique

The size of the sleep transistor is obtained with respect to the pull-up or pull-down transistors connected to the sleep transistors. Fig. 4 shows the SRAM using the sleep transistor technique. High-Vth transistors are used for sleep transistors, if dual Vth values are available. While the logic circuits are not in use, the sleep transistors are turned off. By isolation of the logic networks, with the help of the sleep transistor in the sleep mode, leakage power is reduced dramatically. Although the sleep transistors added additionally will increase area and delay

C. *Forced Stack Technique*

In this Technique every transistor in the network is duplicated with both the transistors bearing half the original transistor width in this technique.

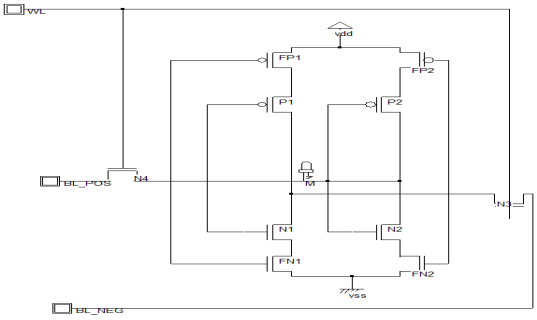

Fig. 5 SRAM Using Forced Stack Transistor Technique

When both the transistors are turned off, the duplicated transistors produce slight reverse bias between the gate and the source [9]. It obtains considerable current reduction due to the dependence of sub-threshold current on gate bias. By retaining state, it overcomes the limitations with sleep technique, but it takes more wake-up time. Fig 5 shows the structure of the SRAM Using Forced Stack Transistor Technique.

D. Sleepy Stack

Sleepy stack technique uses the existing techniques of sleep transistor and forced stack [10]. The Sleepy Stack technique offers the advantage of both these existing techniques. Mainly this technique has lower leakage power dissipation, minimum delay and it's retaining the exact state. The advantages of this technique are to have a state retain, minimal delay and reduced power dissipation.

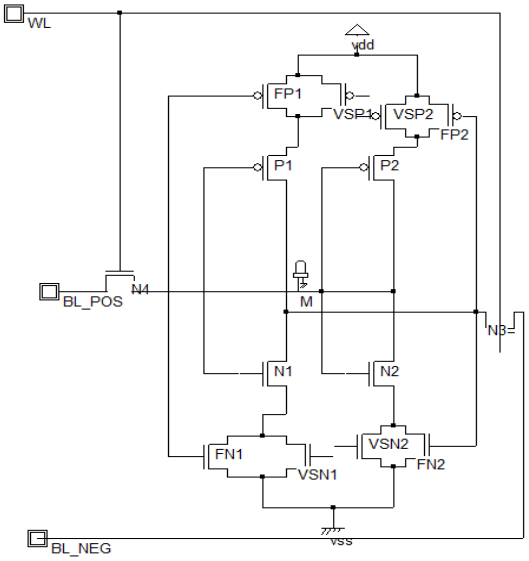

Fig. 6 SRAM Using Sleepy Stack Transistor

Now explaining how the sleepy stack works during active mode and during sleep mode. Also, explaining leakage power saving using the sleepy stacks structure. The sleep transistors of the sleepy stack operate similar to the sleep transistors used in the sleep transistor technique in which sleep transistors are turned on during active mode and turned off during sleep mode. During active mode S = 0 and S0 = 1 are asserted, and thus all sleep transistors are turned on. This sleepy stack structure [1] can potentially reduce circuit delay in two ways. Firstly, since the sleep transistors are always on during active mode, the sleepy stack structure achieves faster switching time than the forced stack structure; specifically, in Figure at each sleep transistor drain, the voltage value connected to the sleep transistor source is always ready and available at the sleep transistor drain, and thus current flow is immediately available to the low-V_{th} transistors connected to the gate output regardless of the status of each transistor in parallel to the sleep transistors.

E. Lector Technique in CMOS Circuit Design

Lector approach to reduce leakage current is based on the effective stacking of transistors between the supply voltages to the ground voltage. In Lector approach two leakage control transistors are introduced between the conventional pull-up and pull-down logic circuits of a functional block [5]. For example, the conventional CMOS NAND Gate circuit is shown in Fig-7 and the Lector based CMOS NAND Gate circuit is shown in Fig-8.

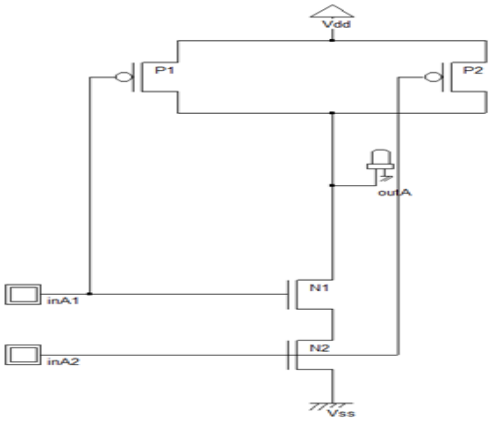

Fig. 7 Conventional CMOS NAND Gate Circuit

The LECTOR technique wiring configuration in this approach ensures that one of the two leakage control transistors is always near its cut-off region of operation irrespective of the input voltage. The Lector follows the concept that, "a state with more than one transistor OFF in a path between supply and ground voltage is less leaky than a state with only one transistor OFF between any supply and ground path". Thus the lector approach leads to a current limited resistive path between the supply voltages to reduce the leakage power dissipation through the lector circuit

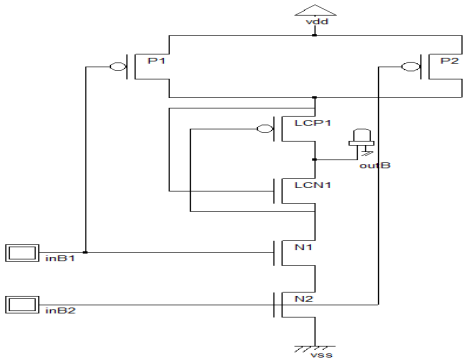

Fig. 8 LECTOR CMOS NAND Gate Circuit

III.CONCLUSION

The main aim of this paper is to give a survey of the various steps taken towards the reduction of the leakage power for VLSI designs. Memory hardware are very important and mandatory part of all real time processing hardware in the present world of emerging electronic applications. So, a power efficient design is always an expectation of fabrication technology from the hardware designers. Growing complexity of mobile applications and other latest wireless applications are the features which make the battery power problem more challenging Farther, the existing techniques can be improved in future works in accordance with the day-by-day advancing fabrication methodologies to obtain more improved performance of the memories and other operational circuits. It is concluded that the optimized leakage power reduction technique will also play an important role in reducing the leakages., Mainly focused on the high impact research area is on low power VLSI.

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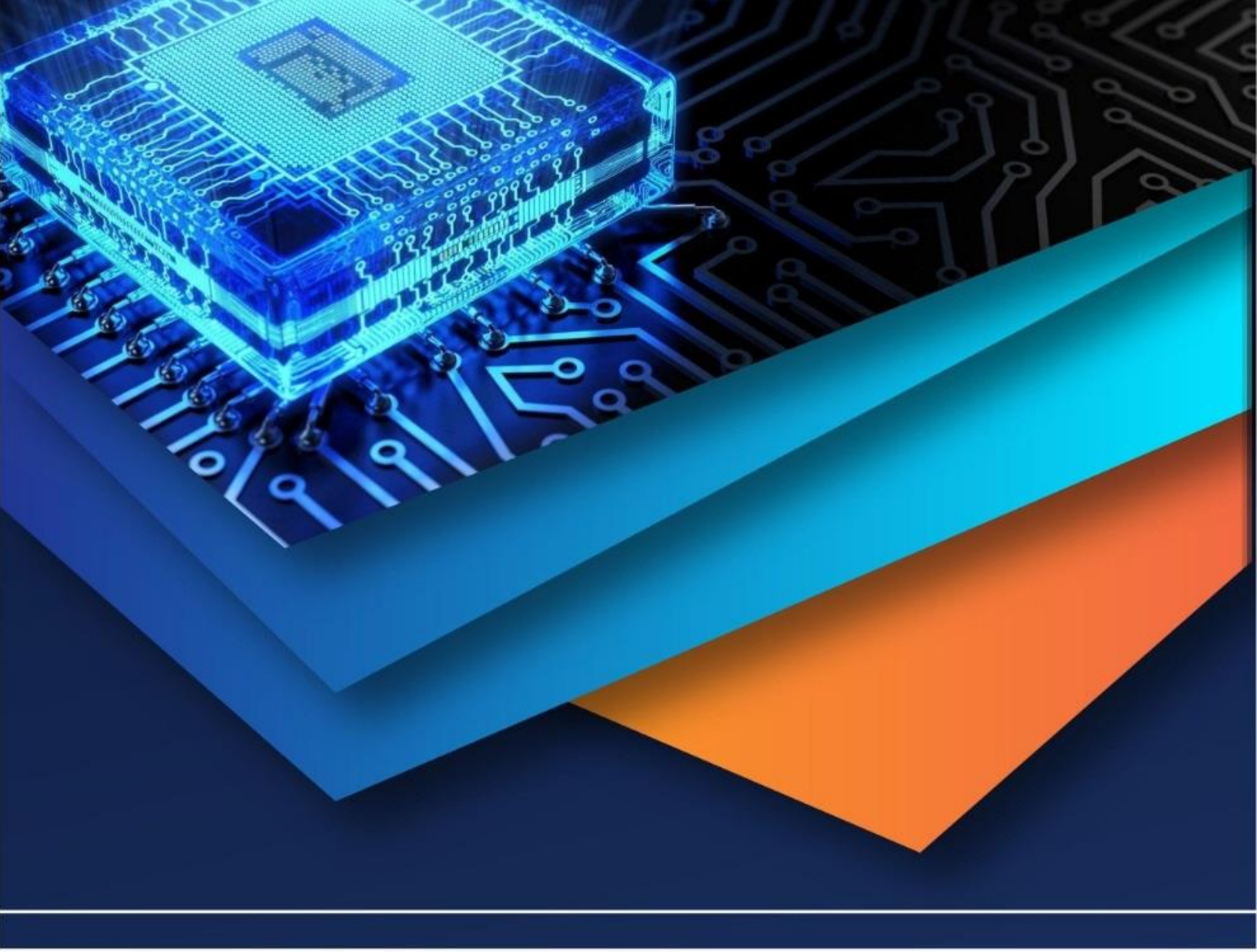

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