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Leakage Power Reduction by Using Power Gating Methods in Differential Amplifier

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Abstract: In the integrated circuits, an inverter based differential amplifier are playing major role. To improve the dynamic response of an adaptively biased low dropout regulator (AB-LDR) while maintaining a low quiescent current. To improve the performance of the inverter based differential amplifier in this paper a new efficient Sleep transistor and Multi-Threshold CMOS based efficient low-dropout Regulator is introduced. By using this proposed regulators, which will provides much better performance compared to other regulators. The proposed has implemented in 45nm CMOS technology with the help of tanner tool.

Keywords: Power optimization, inverter based differential amplifier, adaptively biased low dropout, Sleep transistor and Multi-Threshold CMOS.

I. INTRODUCTION

Now a day, Power optimization is the use of electronic design automation tools to optimize (reduce) the power consumption of a digital design, such as that of an integrated circuit, while preserving the functionality. A low-dropout or LDO regulator is a DC linear voltage regulator that can regulate the output voltage even when the supply voltage is very close to the output voltage. The advantages of a low dropout voltage regulator over other DC to DC regulators include the absence of switching noise, smaller device size and greater design simplicity. Low dropout regulators (LDRs) are capable of generating a noise-free/clean supply with a good dc regulation. Due to these characteristics, they become an integral part of any power management unit. A simple symmetric operational trans-conductance amplifier is used as the error amplifier (EA), with a current splitting technique adopted to boost the gain. This also enhances the closed-loop bandwidth of the LDO regulator. Furthermore, a fast responding transient accelerator is designed through the reuse of parts of the EA. These advantages allow the proposed LDO regulator to operate over a wide range of operating conditions while achieving 99.94% current efficiency. In the rail-to-rail output stage of the EA, a power noise cancellation mechanism is formed, minimizing the size of the power MOS transistor. In this paper a new we going to minimize the Optimized power by using two techniques, such as Sleep transistor and Multi-Threshold CMOS by using this technique which will provide much better performance compared with the existing system.

II. RELATED WORK

1) *Gabriel A. Rincon-Mora and Phillip E. Allen* has discusses some techniques that enable the practical realizations of low quiescent current LDO's at low voltages and in existing technologies. The proposed circuit exploits the frequency response dependence on load-current to minimize quiescent current flow. Other applications, like dc-dc converters, can also reap the benefits of these enhanced MOS devices. An LDO prototype incorporating the aforementioned techniques was fabricated. This circuit also works properly at the theoretical limit. However, systematic offset performance for this circuit is poor.
2) *Chang-Joon Park et.al* has present a new design techniques for a high power supply rejection (PSR) low drop-out (LDO) regulator. A bulky external capacitor is avoided to make the LDO suitable for system-on-chip (SoC) applications while maintaining the capability to reduce high-frequency supply noise. The paths of the power supply noise to the LDO output are analyzed, and a power supply noise cancellation circuit is optimizing the error amplifier.
3) *Chung-Hsun Huang et.al* introduced the fast responding transient accelerator is designed through the reuse of parts of the EA. These advantages allow the proposed LDO regulator to operate over a wide range of operating conditions while achieving 99.94% current efficiency, a 28-mV output variation for a 0-100 mA load transient, and a power supply rejection of roughly 50 dB over 0-100 kHz. The area of the LDO regulator is only 0.0041 mm^2, because of the compact architecture. They not show the dominant ESR effects of output variation during the load transient.
4) *Mohammad Al-Shyoukh, Hoi Lee, Raul Perez,* The LDO with the proposed impedance-attenuated buffer has been implemented in a 0.35-mum twin-well CMOS process. The proposed LDO dissipates 20-muA quiescent current at no-load condition and is able to deliver up to 200-mA load current. With a 1-muF output capacitor, the maximum transient output-voltage variation is

within 3% of the output voltage with load step changes of 200 mA/100 ns. The limitations are low dropout voltage, high output current, low no-load quiescent current, and small output transient undershoots.

5) *Wonseok Oh and Bertan* Bakkaloglu has defined the Current feedback amplifiers (CFAs) provide fast response and high slew rate with Class-AB operation. Fast response, low-dropout regulators (LDRs) are critical for supply regulation of deep-submicron analog baseband and RF system-on-chip designs. An LDR with an developed. The main limitation of the system is low-frequency PSR can still be improved by CFA-based second stage driving the regulation field-effect transistor is presented. The main limitation of the system is the output of the regulator is not constant.

III. PROPOSED SYSTEM

A. Low dropout regulators

Low dropout regulators (LDOs) are a simple inexpensive way to regulate an output voltage that is powered from a higher voltage input. They are easy to design with and use. For most applications, the parameters in an LDO datasheet are usually very clear and easy to understand. However, other applications require the designer to examine the datasheet more closely to determine whether or not the LDO is suitable for the specific circuit conditions. Unfortunately, datasheets can't provide all parameters under all possible operating conditions. To the designer must interpret and extrapolate the available information to determine the performance under non-specified conditions.

Standard regulators, the pass element are either a Darlington NPN or PNP output stage. Fig. 1 shows that a Darlington transistor has a high collector-to-emitter voltage drop because the gate drive voltage encounters two base-to-emitter drops before reaching the output. Standard linear regulators have voltage drops as high as 2 V which are acceptable for applications with large input-to-output voltage difference such as generating 2.5 V from a 5 V input.

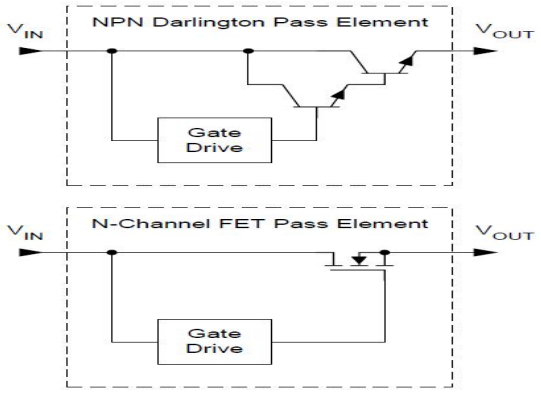

Fig.1. LDO pass elements.

Fig.2. shows an LDO block diagram in its most basic form. The input voltage is applied to a pass element, which is typically an N-channel or P-channel FET, but can also be an NPN or PNP transistor. The pass element operates in the linear region to drop the input voltage down to the desired output voltage. The resulting output voltage is sensed by the error amplifier and compared to a reference voltage. The error amplifier drives the pass element's gate to the appropriate operating point to ensure that the output is at the correct voltage. As the operating current or input voltage changes, the error amplifier modulates the pass element to maintain a constant output voltage. Under steady state operating conditions, an LDO behaves like a simple resistor.

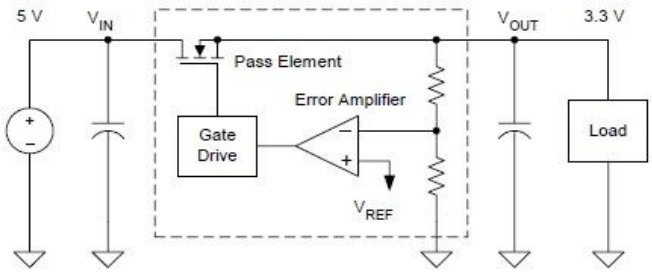

Fig:2 LDO block diagram

B. Inverter based Differential Amplifier

The inverter based differential amplifier. All the transistors operate in the subthreshold region. The design uses N-Well technology. The N-Wells are biased using an on-chip bias circuitry, while the p-substrate is connected to common mode terminal GND. In the first stage, transistors *M1A* and *M1B* form the NMOS differential pair, while the transistors *M2A* and *M2B* are the PMOS differential pair. The current sources formed by *M3* and *M4* are self biased by the output of *M1A* and *M2A* inverter pair. The source terminal of transistors *M1A* and *M2A* are degenerated by the negative feedback. This ensures proper biasing of the input differential pair against all variations in the PVT. Since four amplifier devices are present the differential gain is 6dB higher than the conventional inverter.

In order to improve the SR the threshold voltages of all the transistors are lowered by slightly forward biasing the body terminal, but away from large leakage current conduction. With the N-Well process, the body terminals of all the NMOS transistors are connected to fixed bias potential, GND. However all the PMOS transistors are connected to bias potential *VBP* to keep up to the SR at slow process corners. The threshold voltage increase due to slow process

corner drives the transistor *M7* from subthreshold to cutoff region. The resulting increase in voltage at the drain terminal of transistors *M7* and *M8* reduces the bias potential *VBP* .This reduction of the bias potential forward biases the bulk terminal of the PMOS transistors of the amplifier to enhance the SR at slow process corners. The bulk of all the PMOS could optionally be connected to fixed bias potential, GND, as done for NMOS transistors, to lower the power dissipation.

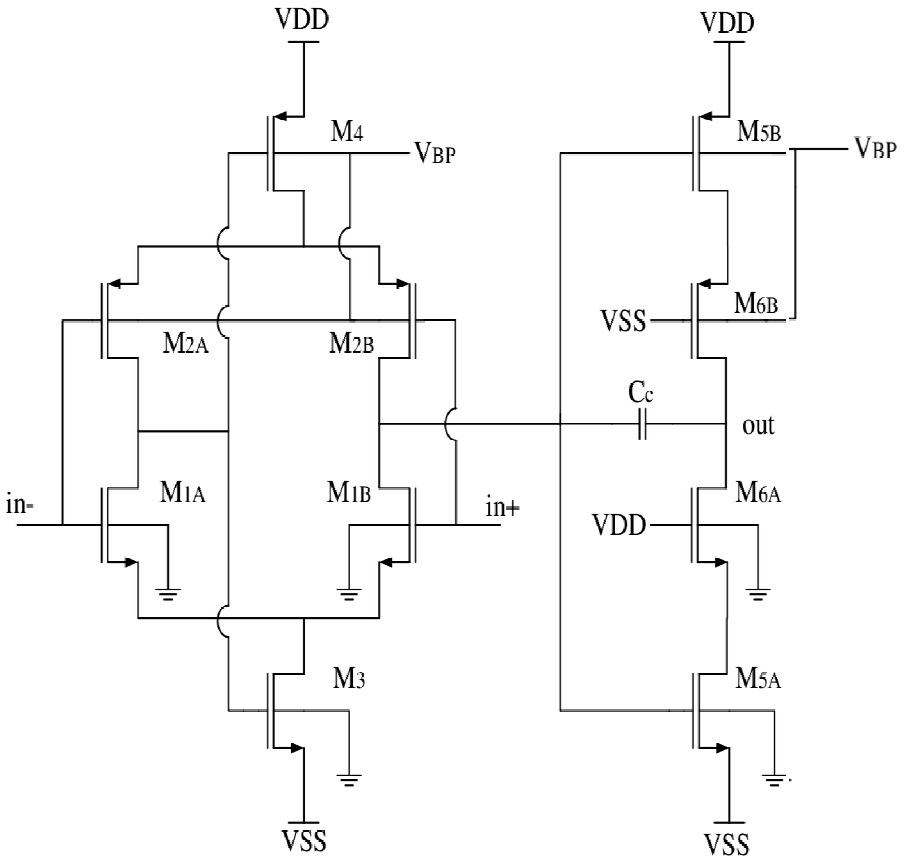

Fig:3 Amplifier Circuit

The differential input inverter based amplifier [5] is used as the first stage of the amplifier followed by the class C inverter. The amplifier is compensated by a small miller capacitance at the output stage. All the transistors are designed to operate in the subthreshold region. A dual power supply is used, thereby eliminating requirement of body bias voltage generation. The common mode voltages of input and output are at GND. To improve the SR, the threshold voltage of all NMOS transistors are reduced by fixed body bias and that of the PMOS transistors are reduced by connecting the body terminal to an on chip body bias circuit.

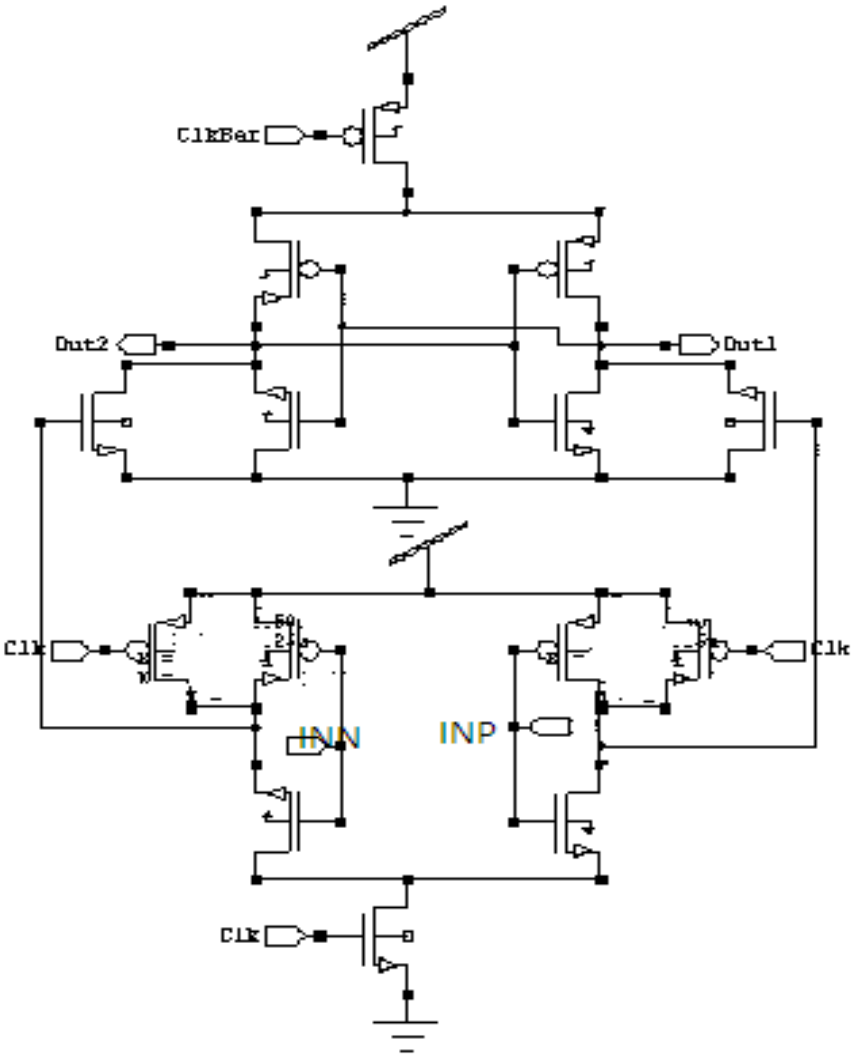

Fig 4: Circuit diagram of Inverter Based Differential Amplifier

C. Sleep Transistor

A sleep transistor is either a pMOS or nMOS high VT transistor and is used as a switch to shut off power supplies to parts of a design in standby mode. The pMOS sleep transistor is used to switch VDD supply and hence is called a "header switch." The nMOS sleep transistor controls VSS supply and hence is called a "footer switch." In designs at 90nm and below, either a header or footer switch is used due to tight voltage margin and too large area penalty when both header and footer switches are implemented. Although the concept of the sleep transistor is straight forward, optimal sleep transistor design and implementation are a challenge due to various effects, introduced by the sleep transistor and its implementations, on design performance, area, routability, overall power dissipation, and signal/power integrity. Optimal sleep transistor design also depends on design specific goals and chosen CMOS technology and process. A number of decisions need to be made including the choice of header or footer switch, normal or reverse body bias, optimal transistor size, and layout implementation details such as single or double row and extra rail or direct via-pillar for permanent power connection.

D. Multi-Threshold CMOS

A variation of CMOS chip technology which has transistors with multiple threshold voltages (V_{th}) in order to optimize delay or power. The V_{th} of a MOSFET is the gate voltage where an inversion layer forms at the interface between the insulating layer (oxide) and the substrate (body) of the transistor. Low V_{th} devices switch faster, and are therefore useful on critical delay paths to minimize clock periods. The penalty is that low V_{th} devices have substantially higher static leakage power. High V_{th} devices are used on non-critical paths to reduce static leakage power.

IV. RESULT AND DISCUSSION

The presented amplifier has been designed and simulated using Tanner tools with 45 nm technology.

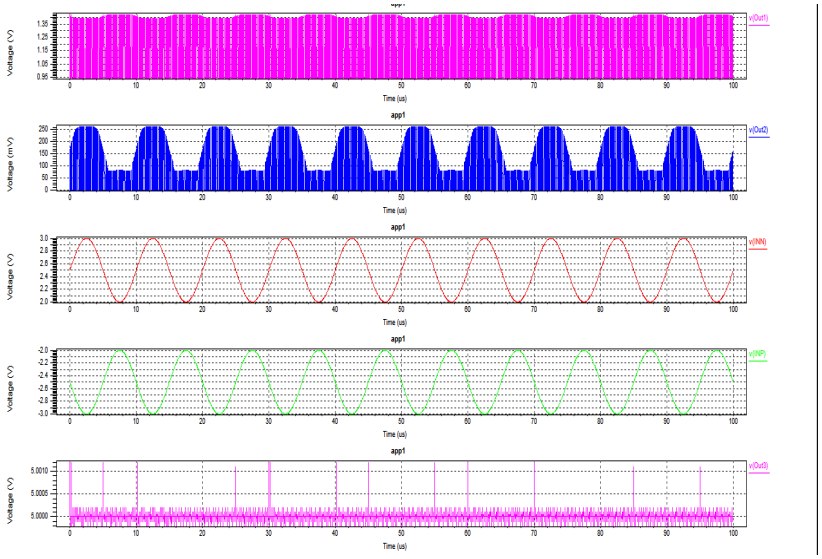

Fig 5: LDO OUTPU

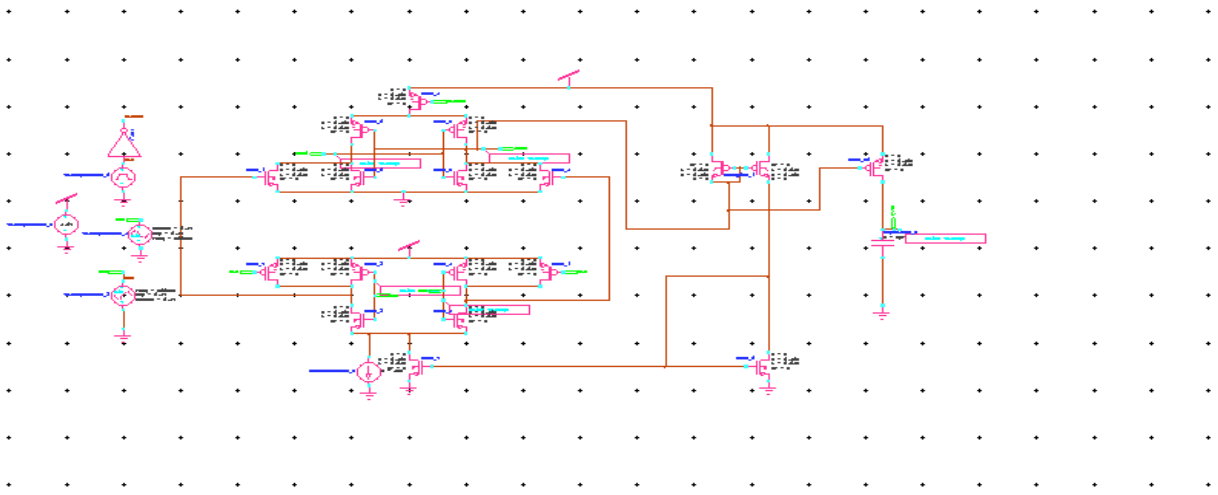

Fig 6: Circuit Diagram of LDO based Differential Amplifier

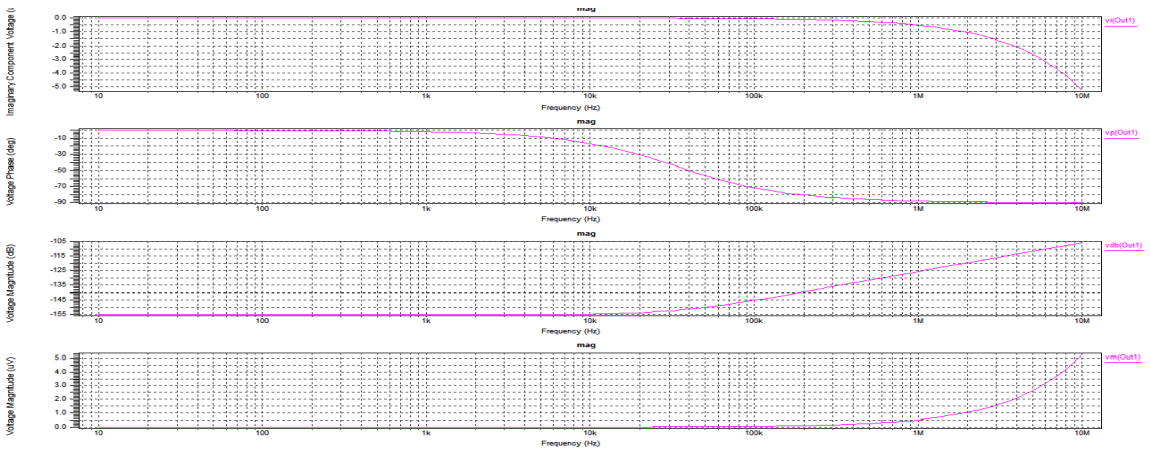

Fig 7: PHASE AND MAGNITUDE

V. CONCLUSION

A low voltage and low power inverter based differential amplifier is been presented. The amplifier provides high gain and remain stable at all process corners. The input stage of the amplifier is fully differential giving high CMRR and the output stage employs class C inverter to provide high differential gain.

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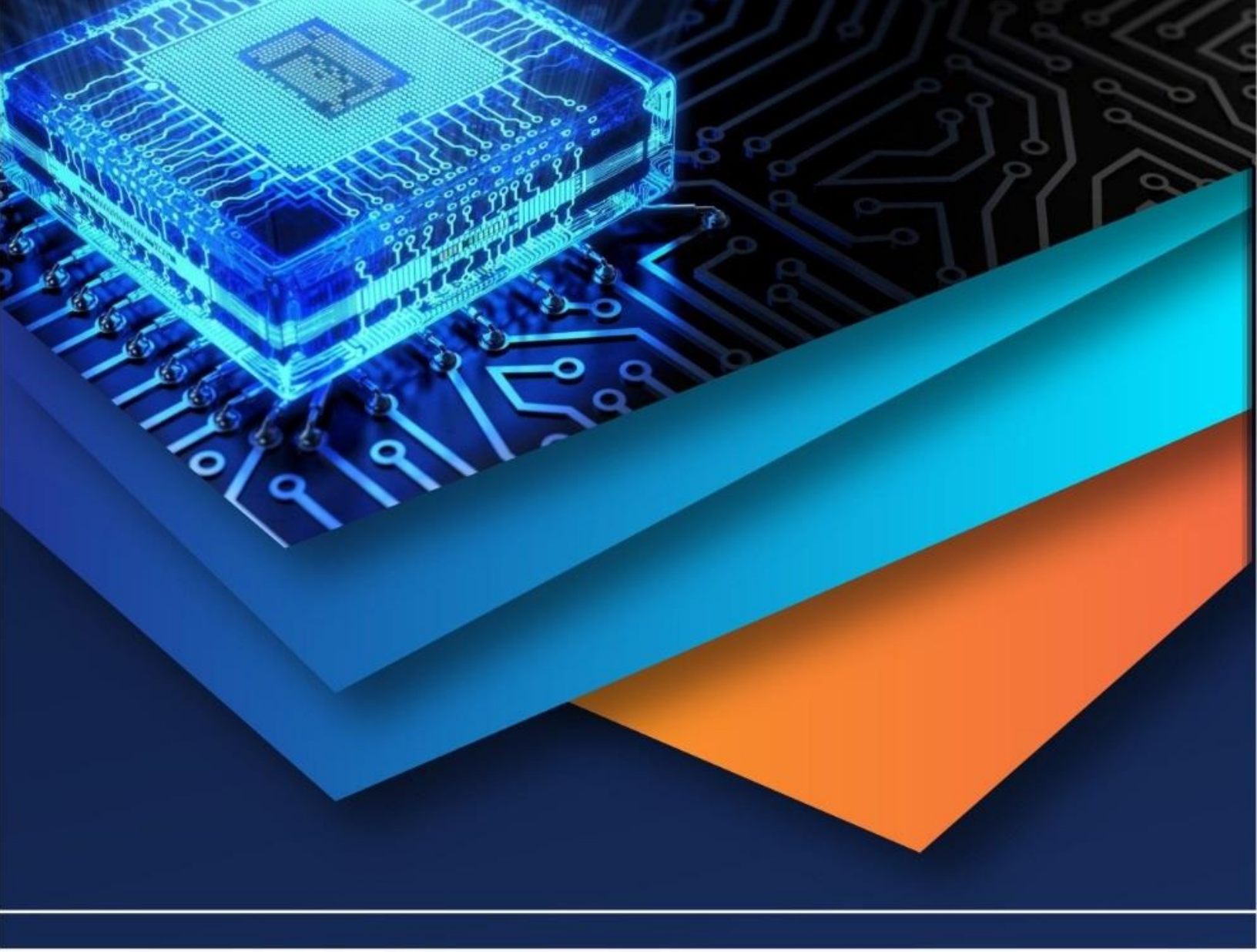

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