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Design of High Gain Low Voltage CMOS Comparator

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Abstract: ***Comparators used in most of the analog circuits like analog to digital converters, switching circuits, and communication blocks and also plays a vital role in mixed mode integrated circuits. Analog circuits which work on low voltage and consume low power are the requirements of present day. This paper presents a two stage CMOS comparator which operates at 1V power supply and designed using TSMC 1um CMOS technology. The comparator is designed to exhibits gain of 91dB with low power dissipation of 14uW. The external resistance of 60K and load capacitance 1pf is used. Design and simulation of the COMS has been carried out in Pspice tool.***
Keywords: CMOS comparator, Low power, Offset, Slew rate, Propagation Delay, PDP

I. INTRODUCTION

Low voltage and low power circuits are required now days due to the rapid growth of portable applications which promotes battery operation. That means in future power supply of 1V or less will be used for the implementation of mixed analog – digital design. Both the analog and digital portion of the circuit is operated with the same supply voltage in mixed – signal design. To achieve higher speed and reduce power consumption many digital applications such as microprocessors, microcontrollers, and memories derives technology scaling and reduced power supply.

A comparator may be defined as a circuit which compares a signal voltage applied at one input of an operational amplifier with a known reference voltage at the other input and produces either a high or a low output voltage depending on which input is higher. Operational amplifier in an open loop configuration or sometimes a positive feedback configuration can be used as a comparator. A comparator must amplify small voltage into logic levels for a pipeline analog to digital converter. The comparators input offset voltage, the delay and input signal range directly affects the speed and resolution of an analog to digital converter. So with high gain and low power a comparator must satisfy all the above parameters. The power dissipation can be reduced in analog circuits by reducing the power supply or bias current or reducing both.

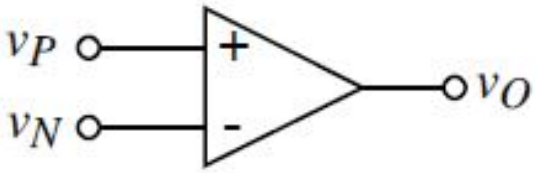
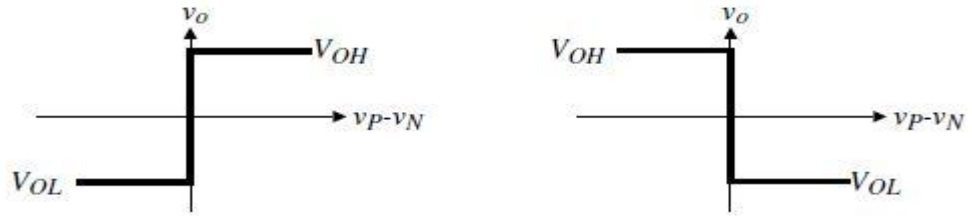


Fig. 1: Comparator symbol

A. Non – INVERTING and Inverting Comparator

The output of comparator is binary with the two levels of outputs –
V_{OH} = the high output of comparator
V_{OL} = the low level output of comparator



(a) (b)

Fig. 2: (a) Voltage transfer function of ideal Noninverting comparator, (b) Voltage transfer function of ideal Inverting Comparator

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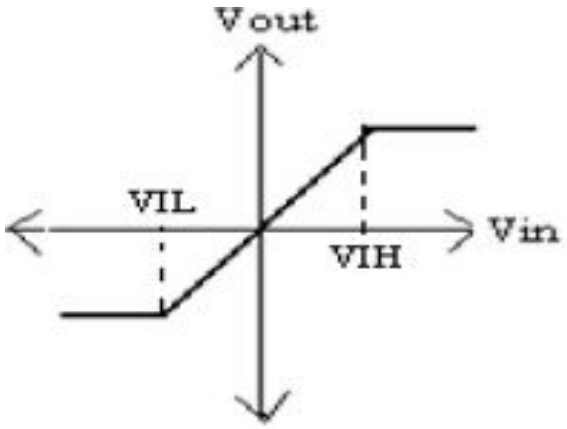

Fig. 3: Voltage transfer function of Practical Comparator

Where
V_{IH} = Smallest input voltage at which the output voltage is V_{OH}
V_{IL} = Largest input voltage at which the output voltage is V_{OL}
The delay can be reduced by cascading the gain stages in a comparator. The propagation delay is inversely proportional to the input voltage applied. So by applying the larger voltage the delay can be improved up to the limits set by the slew rate. Propagation delay and settling time are the most important dynamic parameters that determine the speed of a comparator. If the propagation delay time is determined by the slew rate of the comparator, then this time can be calculated as

$$T_P = \Delta T = \frac{\Delta V}{SR} = \frac{VOH - VOL}{2SR}$$

Where
Tp (or) ΔT = propagation delay
ΔV = Change of the output voltage
SR = Slew rate.
VOH = Upper limit of the comparator
VOL = Lower limit of the comparator

II. TWO STAGE CMOS COMPARATOR

Open loop comparator with two stages comprises of two differential inputs. It consists of differential amplifier, input stage and output stage. One of the advantages of two stage CMOS comparator is that the circuit requires minimum number of transistors and so the circuit area is small.

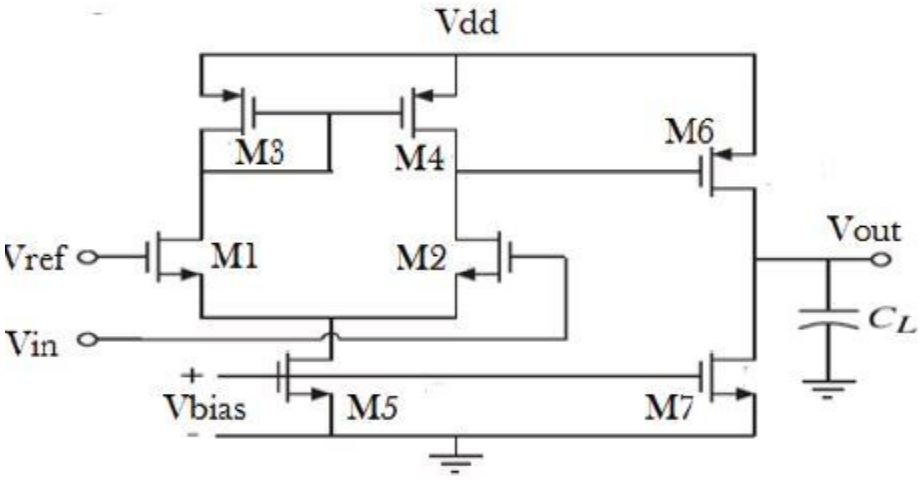

Fig. 4: Two stage CMOS Comparator

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For the implementation of a high gain two stage open loop comparator, the design without compensation will be an excellent option. To get the desired resolution comparator needs differential input and moderate gain. That's why two stage operational amplifiers make a very good implementation of the comparator. So the circuit will be simplified because it is not essential to compensate the comparator because generally it will be used in an open loop mode. Indeed, the largest bandwidth is possible for comparator, if it is not compensated and hence the large bandwidth gives faster response.

The circuit has shown in figure.4 consists of a cascode of Voltage to Current and Current to voltage stages. First stage consist of a differential amplifier of NMOS transistor (M1, M2) converting the differential input voltage to differential currents. Which are applied to a current mirror load of PMOS transistor (M3, M4) recovering the voltage. Transistors M1, M2, M3, and M4 form the first stage of the op amp the differential amplifier with differential to single ended transformation. Transistors M1 and M2 are standard N channel MOSFET (NMOS) transistors which form the basic input stage of the amplifier. The gate of M1 is the inverting input and the gate of M2 is the non-inverting input. A differential input signal applied across the two input terminals will be amplified according to the gain of the differential stage. The gain of the stage is simply the transconductance of M2 times the total output resistance seen at the drain of M2. The two main resistances that contribute to the output resistance are that of the input transistors themselves and also the output resistance of the active load transistors, M3 and M4. The current mirror active load used in this circuit has three distinct advantages. First, the use of active load devices creates a large output resistance in a relatively small amount of die area. The current mirror topology performs the differential to single-ended conversion of the input signal, and finally, the load also helps with common mode rejection ratio. In this stage, the conversion from differential to single ended is achieved by using a current mirror (M3 and M4). The current from M1 is mirrored by M3 and M4 and subtracted from the current from M2. The differential current from M1 and M2 multiplied by the output resistance of the first stage gives the single-ended output voltage, which constitutes the input of the second gain stage.

The second stage consists of common source MOSFET converting the second stage input voltage to current. This transistor is loaded by a current sink load, which converts the current to voltage at the output. C_L is the load capacitor. The purpose of the second gain stage, as the name implies, is to provide additional gain in the amplifier. Consisting of transistors M5 and M6, this stage takes the output from the drain of M2 and amplifies it through M5 which is in the standard common source configuration. Again, similar to the differential gain stage, this stage employs an active device, M6, to serve as the load resistance for M5. The gain of this stage is the transconductance of M5 times the effective load resistance comprised of the output resistances of M5 and M6. M6 is the driver while M7 acts as the load.

III. DESIGN OF A TWO STAGE CMOS COMPARATOR

A. Design steps

The following are the steps to design a two stage CMOS comparator.

Step 1 – Current drive requirement of M_7.

$$I_{D7} = C_L\left(\frac{dV}{dt}\right) = C_L(SR)$$

Step 2 – Size of M_7 and M_6

$$(W/L)_7 = \frac{2I_{DS7}}{K_N(V_{DS7(SAT)})^2}$$

$$(W/L)_6 = \frac{2I_{SD6}}{K_P(V_{SD6(SAT)})^2}$$

Step 3 – Gain of second stage

$$A_{V2} = -\left(\frac{g_{m6}}{g_{ds6} + g_{ds7}}\right) = -\frac{\sqrt{2K_P I_{SD6}(W/L)_6}}{I_{SD6}(\lambda_P + \lambda_N)}$$

Step 4 – First stage biasing current

$$I_{SD4} = \frac{(W/L)_4}{(W/L)_6} I_{SD6}$$

Step 5 - Using the minimum size for M5, determine the current I_{DS5} that mirror with M7. That is,

$$I_{DS5} = \frac{(W/L)_5}{(W/L)_7} I_{DS7}$$

Step 6 – Size of M1

$$A_{V1} = \frac{g_{m1}}{g_{ds2} + g_{ds4}} = \frac{\sqrt{2K_N I_{DS1}(W/L)_1}}{I_{DS1}(\lambda_N + \lambda_P)}$$

Step 7 – Size of M5

$$(W/L)_5 = \frac{2I_{DS5}}{K_N (V_{DS5(SAT)})^2}$$

Step 8 – Size of M3

$$V_{G1(max)} = V_{DD} - \sqrt{\frac{2I_{SD3}}{K_P (W/L)_3}} - |V_{T3}| + V_{T1}$$

Step 9 – Size of M8

$$(W/L)_8 = \frac{2I_{DS8}}{K_N (V_{GS8} - V_{TN})^2}$$

The external resistor Rb connected between V_{G8} and ground must be chosen to provide the required current for M8.

$$R_b = \frac{0 - V_{G8}}{I_{DS8}}$$

B. Circuit Diagram

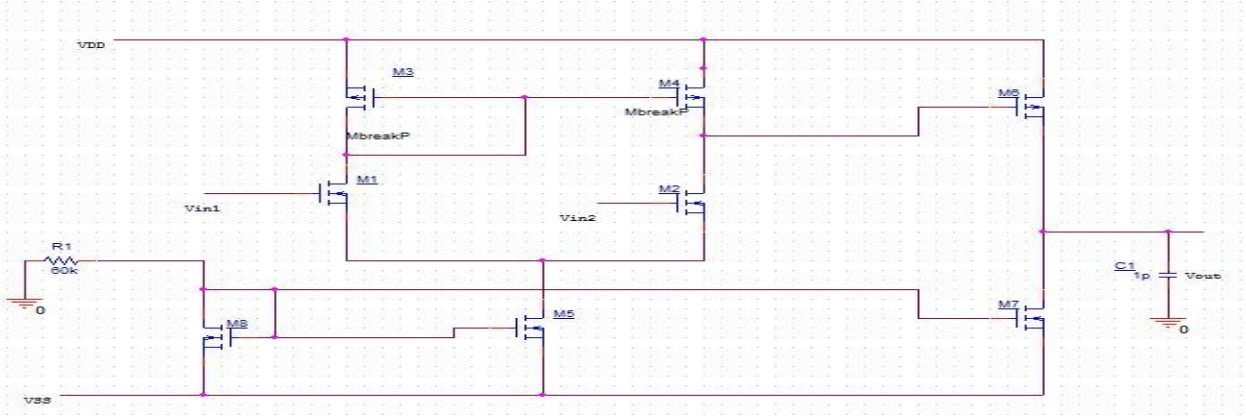
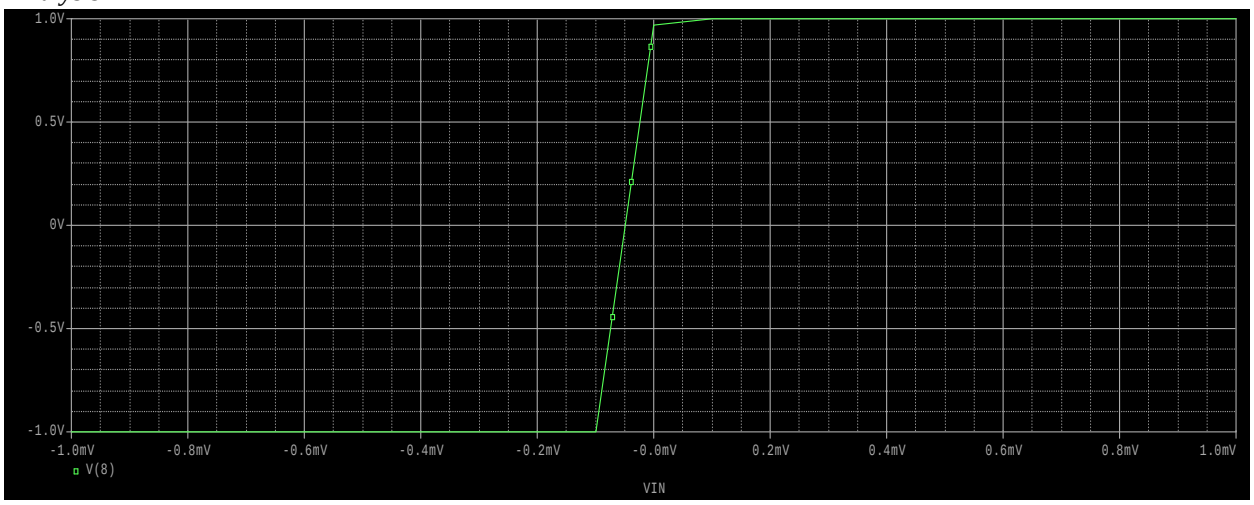


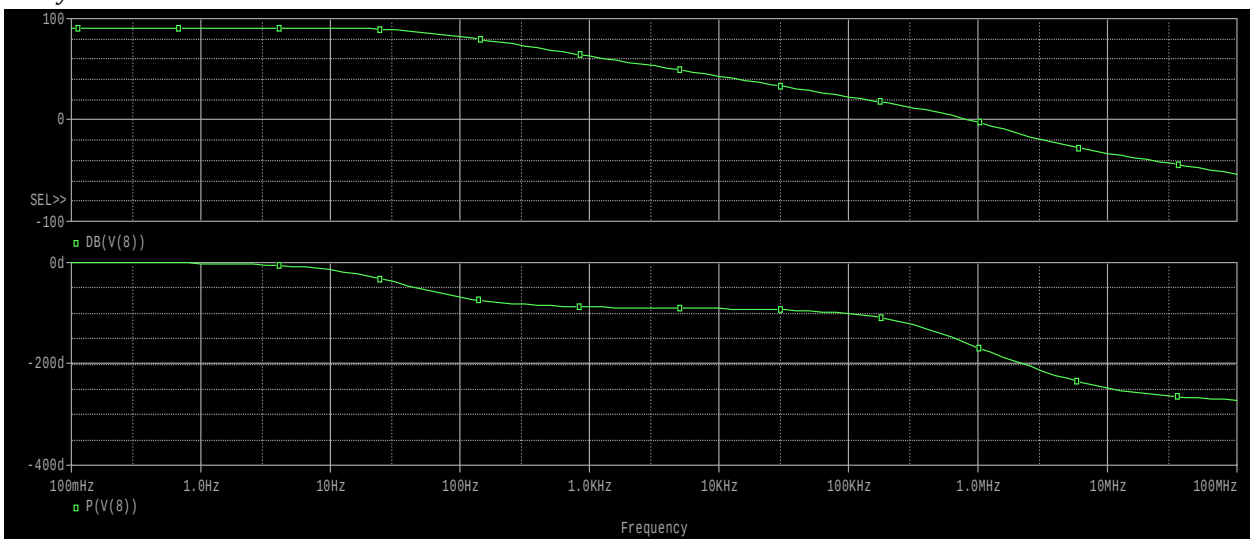
Fig. 5: Two stage CMOS OP-Amp Circuit

IV. SIMULATION AND RESULT

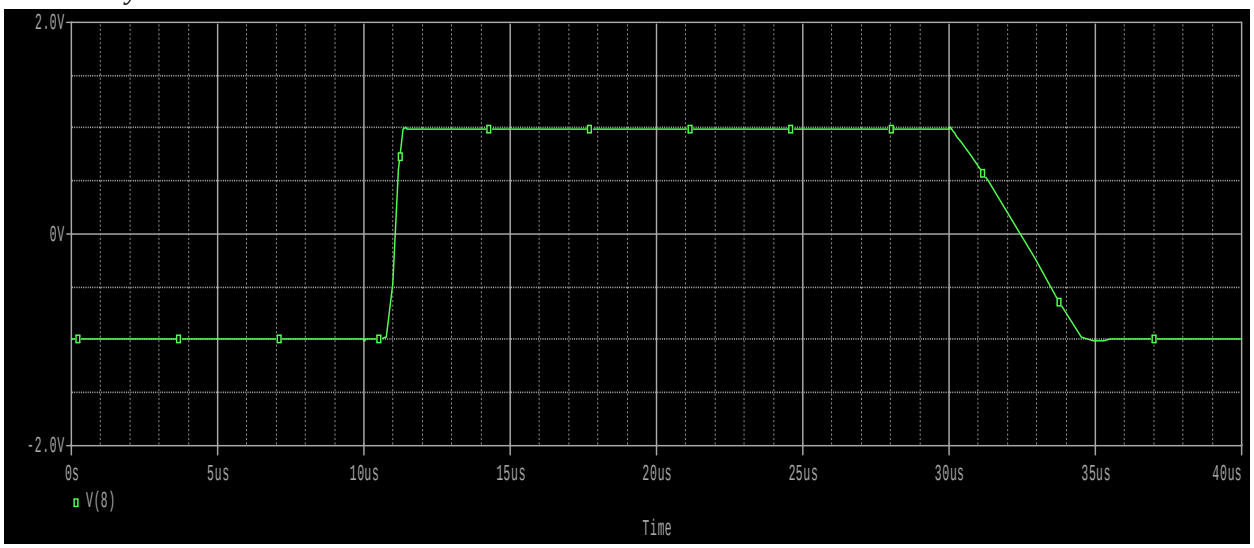
A. *DC Analysis*



B. *AC Analysis*



C. *Transient Analysis*



The geometric dimension incorporated and the electrical parameter yielded

Table 1

The Design Parameters		The Electrical Parameters Yielded	
M1	200/1 um/um	Phase margin	23˚
M2	200/1 um/um	Gain	91db
M3	1/1 um/um	UGB	1MHz
M4	1/1 um/um	Slew Rate[Rise]	20.87V/ms
M5	1/1 um/um	Slew Rate[Fall]	63.1V/ms
M6	12.5/1 um/um	Output Swing	± 1V
M7	5.88/1 um/um	Gain Margin	6.6˚
M8	40/1 um/um	Power Dissipation	14uW
VDD	1V	Delay	50us
C_L	1pf	PDP	700
R_b	60K	Output Resistance	45kΩ

V. CONCLUSION

This paper presented the full design and analysis of a two stage CMOS comparator. The comparator presented in this paper operates in saturation mode and regulates its bias current. The comparator has low power dissipation as well as low voltage. This comparator circuit exhibits slew rate of 20V/ms with high gain of 91db and low power dissipation of 14uw. As there is always some scope of improvement, here we can increase gain bandwidth with improving slew rate and reducing the delay.

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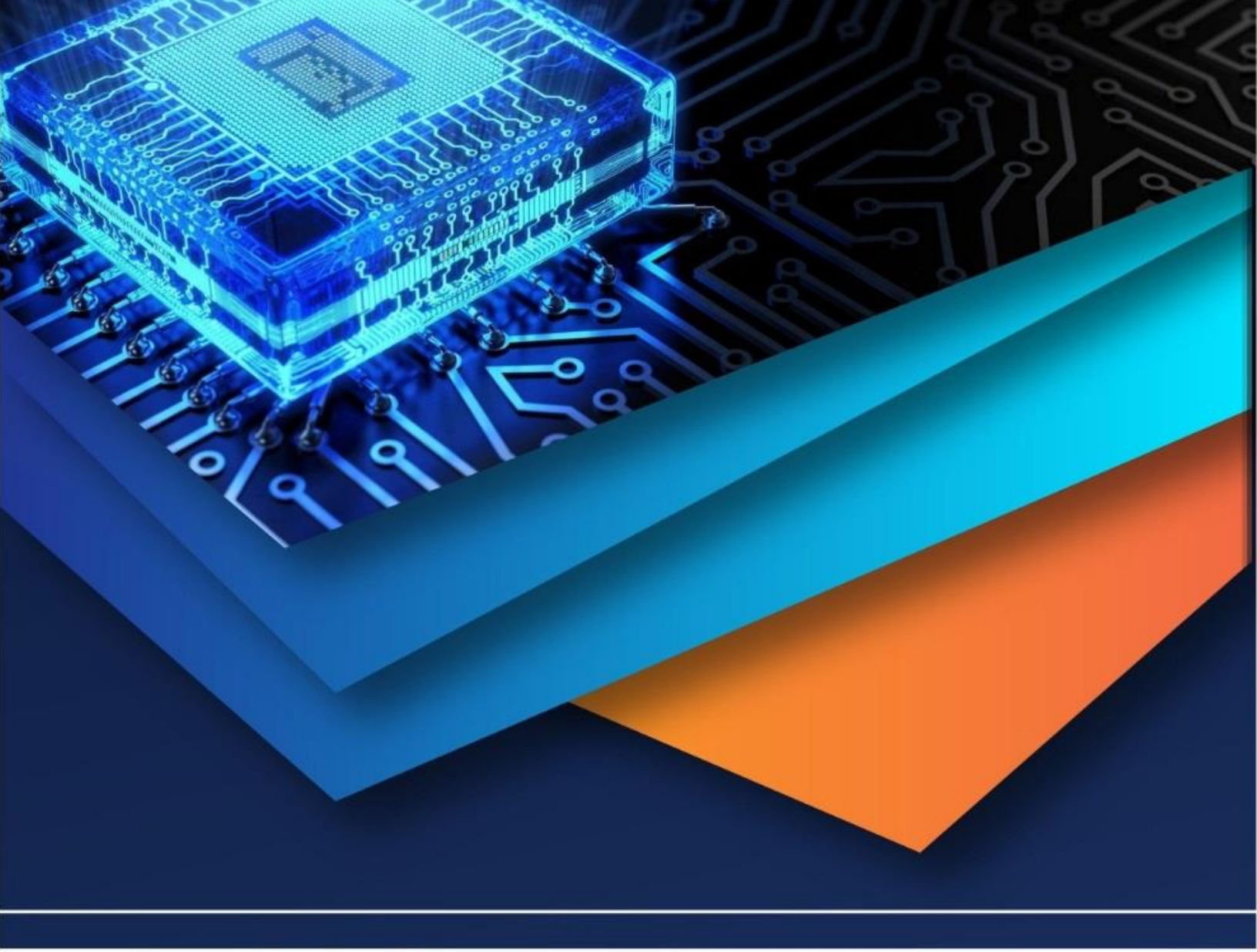

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