iJRASET
International Journal For Research in
Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 6 **Issue:** IV **Month of publication:** April 2018

DOI: http://doi.org/10.22214/ijraset.2018.4435

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 6.887
Volume 6 Issue IV, April 2018- Available at www.ijraset.com

PV Interfacing Multi-Level Inverter Design For Compensation of Harmonics Due To Fluorescent Lamp Load and Personal Computer Load

Aravind. C[1], Madhumitha. R[2], Gokula Brindha. S[3]
[1]*Department of EIE, Kongu Engineering College, Erode, Tamilnadu*
[2, 3]*Department of EEE, Velalar College of Engineering and Technology, Erode, Tamilnadu*

Abstract: Due to the increased usage of non-linear loads, the harmonics present in the current has been increased which has become a greater concern from the utility side. To mitigate the harmonic distortions the active or passive filters are used. Now-a-days the shunt active filters involving capacitors are used for harmonic mitigation. But it introduces harmonic resonance. Due to the development of power electronic converters, interfacing of Renewable Energy Sources (RES) to the distribution system has been increased. Improving power quality with the help of Distributed Generation (DG) has become a promising idea. In this proposed method, a novel control strategy is presented that utilizes the grid-connected Distributed Energy Resources (DERs) to achieve maximum benefits from them when implemented in 1-phase 2-wire distribution systems. It utilizes a 15-level inverter to connect the DERs to the grid which reduces the Total Harmonic Distortion (THD) below 2.87% as reduced by the conventional inverter while connecting different non-linear loads when compared to the conventional inverter. The 15-level inverter is controlled to perform as a multi-function device by incorporating shunt active power filter function for harmonic rejection with power injection. The performance of the multi-level inverter is tested with fluorescent lamp load and personal computer load.
Keywords: Distributed Energy Resource, Harmonic Compensation, Multi-level Inverter, Power Injection, Renewable Energy Source

I. INTRODUCTION

The major problem faced by the electric utilities and end users of electric power is the increasing energy demand. Fossil fuel is the only resource that is used for meeting the seventy five percentage of the energy demand of the world. The major issues faced in using the fossil fuels include air pollution, global warming, and reduction in fossil fuel availability which in turn has increased the research interests in RES as an alternative for power generation. DG is a developing research area of interest which involves the integration of RES at the distribution side.

This may cause stability, voltage regulation and Power Quality (PQ) issues. Therefore, a strict technical and regulatory system has to be complied for the DG systems for safe, reliable and efficient operation of the network. The power electronics based equipment involving non-linear loads generate harmonic current, which reduces the quality of power as stated IN [1]. Since there is a great improvement of digital control strategy, the PQ can be enhanced by actively controlling the DG systems. The harmonics in current may result in the harmonics in voltage.

The compensation of load current harmonics is usually carried out with shunt Active Power Filters (APF) at distribution level. The active power filtering is also incorporated with the inverter interfacing the RES with the grid, which reduces the extra hardware complexity. The conventional inverter can be replaced by the multi-level inverter to provide better harmonic rejection as suggested in [2] and someof the advantages of multi-level inverter include reduced stress in bearings of motor, it operates at both low and high switching frequency and it draws current with less distortion.

The block diagram of the proposed method is shown in the Figure 1. The AC source represents the power from the secondary side of the distribution transformer.

The power flows through the short transmission line (<80km) to the load side. The non-linear load connected to the grid produces the harmonics in the current waveform as stated in [2]. In the existing system, the harmonics are mitigated with the help of the Shunt Active Power Filters fed by the capacitors. But the usage of capacitor introduces harmonic resonance in the system.

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 6.887
Volume 6 Issue IV, April 2018- Available at www.ijraset.com

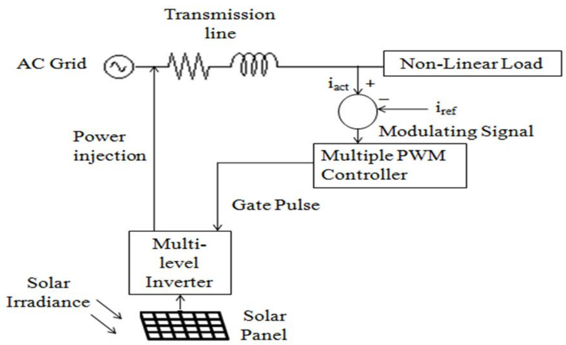


Figure 1 Block Diagram of Proposed Harmonic Mitigation Method

Due to the increased power outages, the utilities started to generate power on the distribution side with the help of RES. The solar energy is the widely available RES for power generation, where DC power is generated and is converted to AC using the PV interfacing inverters which can also be used to mitigate the harmonics as proposed in [3]. Since the multi-level inverter provides better harmonic rejection as stated in [2], it is proposed to use the multi-level inverter instead of the conventional inverter for PV interfacing and harmonic mitigation. The switches of the multi-level inverter are controlled by the Multiple Carrier Pulse Width Modulation (PWM).

The modulating signal for the Multiple Carrier PWM is generated based on the error between the actual current and the reference current. The actual current varies with the load and hence the reference current also changes based on the load. Hence, the reference current has to be found out based on the power consumed by the load and the DC link voltage across the panel.

II. SYSTEM MODELLING

A. Solar Panel Modelling

Solar energy is generally used in the form of solar irradiance to produce electricity. The PV cell works with the Photoelectric effect principle which states that the light energy is converted to electric energy. These cells are made of semiconductor materials like silicon. A typical silicon solar cell generates about 0.5~0.6 volts in normal operation. Many solar cells are connected in series to form a module and many solar modules are connected to make solar arrays to meet the voltage requirement of the system.

As stated in [2], the rating of a solar module is given by the maximum output or maximum power it can deliver. The output of a solar module depends on the number of cells in the module, type of cell and the total surface area. The output of a module changes depending on the amount of solar irradiance, the angle of the module with respect to the sun, the temperature of the module and the voltage at which the load is drawing power from the module. The Figure1 shows the equivalent circuit of the solar cell.

The solar panels are connected in series and parallel and it is used to convert solar energy into electrical energy. The electrical energy produced from the solar cell depends on the internal parameters of the cell, solar irradiance and cell temperature.

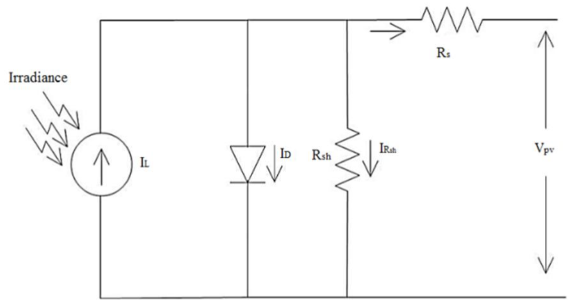


Figure 2 Equivalent Circuit of Solar Cell

To increase PV Voltage solar cells are connected in series. In order to increase current they are connected in parallel. A solar panel of 48 V voltage rating has been used for the simulation purpose. 72 cells are connected together in series to form a module to produce 48 V. Each 48 V solar panel is connected to each stage of multi-level inverter. Table 1 shows the parameters for one cell in 48V module. Normally the solar irradiance value under Standard Test Condition (STC) is 1000 W/m^2, 25^o C.

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 6.887
Volume 6 Issue IV, April 2018- Available at www.ijraset.com

TABLE 1 SOLAR CELL PARAMETERS

Parameters	Values
Short Circuit Current	7.34 A
Open Circuit Voltage	0.6 V
Ideality Factor	1.5
Series Resistance	0.037998 Ω

B. Multi-level Inverter Modelling

Plentiful multilevel converter topologies have been proposed during the last two decades. The modified laddered multi-level inverter topology as proposed in [3] with the least number of switches has been used in order to overcome the disadvantage. This topology uses one voltage source and two switches for each stage. For m-level inverter, (m-1)/2 stages are enough to produce m-levels of voltage. The number of batteries and switches required are reduced to half. If each stage is capable of producing voltage E, then n stages are capable of producing peak voltage of n*E. The output from these stages is a positive pulsed waveform. This output is converted to AC with the help of two pole two throw switch.

In this topology, the 48V solar panel is connected to each stage. A peak voltage of 336 V is generated with 7 stages. The 15 level output voltage is generated. These stage switches are controlled by the gate pulse generated

C. AC Source Modelling

An AC Source is modeled to be the voltage generated from the voltage side. The Voltage Source is modeled to produce a peak voltage of 336V with the frequency of 50Hz. The peak voltage of AC Source is assumed to be equal to the peak voltage generated with the help of multi-level inverter.

D. Transmission Line Modelling

Power generated from the generation side is fed through the transmission line to the load side. The transmission line has its own resistance, inductance and capacitance values. The resistance value in the transmission line is due to the opposition to the flow of current by the conductor. The inductance value of the transmission line is due to the magnetic field around the conductor produced by the current flowing through the conductor. The capacitance value is due to the charges between the lines. Here a short transmission line has been used. Hence it contains only resistance and inductance. Based on the works done in [4] the transmission lines have been modelled. The source side transmission line parameters are 0.1Ω and 3mH and the load side transmission line parameters are chosen as 0.1Ω and 1 mH. The line feeding from the Active Power Filter to the load has resistance and inductance value as 0.1Ω and 2mH.

E. Load Modelling

Nonlinear loads used in industries introduce current harmonics at the utility. This causes malfunctioning of the sensitive loads connected at the PCC. Hence harmonic analysis of the nonlinear loads is essential. Computer simulation is the most convenient way of harmonic analysis provided that the system components are modelled accurately and verified either through measurements or mathematically.

The harmonic current has different components that are multiples of the fundamental frequency of the system. The amplitude and phase angle of a harmonic is dependent on the circuit and on the load it drives. For a fundamental power frequency of 50Hz, the second harmonic is 100Hz, the third harmonic is 150Hz, and so on. The harmonic currents flow toward the power source through the path of least impedance. For validating the proposed system, PC model and Fluorescent lamp model are used as non-linear loads.

1) *Personal Computer Model:* PCs are the most widely used electronic loads in modern life. It constitutes non-linear loads since they incorporate SMPS. The PC current is mainly dominated by the third and fifth harmonic components. It produces harmonic current especially when there is a large concentration of the PCs in a distribution system. It utilizes the SMPS which draws highly non-linear currents that contain large amounts of third and higher order harmonics. SMPS has a large capacitor which maintains approximately constant voltage for the DC bus in the power supply.

A typical PC load model uses an SMPS and comprises of a full wave rectifier, a DC storage capacitor (C), a diode bridge resistance (R) and a series Radio Frequency (RF) choke which is represented by an inductance L. The power supply the PC converts the input AC voltage of 50 Hz frequency to a desired direct current output voltage by means of a single-phase rectifier circuit. The simulation model of PC is shown in Figure 3.

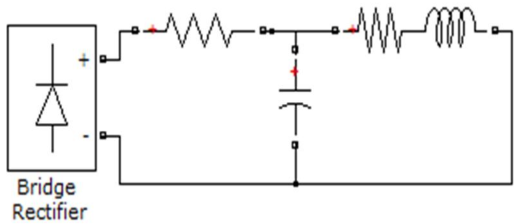


Figure 3 Computer Load Model

The R, L and C circuit parameters are adjusted to match the practical data. Series RL values are chosen as 10Ω and 100mH. The shunt Capacitor value is chosen as 500µF and the Resistance connecting the capacitor to the bridge rectifier is chosen as 0.2Ω based on the works carried out in [9].

2) Fluorescent Lamp Model

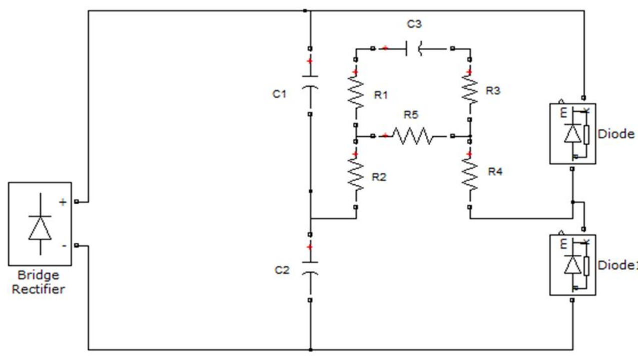


Figure 4 Fluorescent Lamp with Electronic Ballast Model

Fluorescent lamps have a negative dynamic resistance behaviour, which necessitates the use of a ballast to limit the current as stated in [10]. The electronic ballast employs a half wave inverter and an LC filter used to acquire the nonlinear characteristics of the lamp. Simulation model for the fluorescent lamp, shown in Figure 4, is built with the electronic ballast as half-bridge inverter. The values of R_1, R_2, R_3 and R_4 are chosen as 4.8Ω and the value of R_5 is chosen as 200Ω and the values of C_1 and C_2 are chosen as 2.2µF and the value of C_3 is chosen as 0.017µF based on the works carried out in [9].

III. GATE PULSE GENERATION

A control system presented in [5] is concise and requires less computational effort than many others found in the literature. It is formed by a DC voltage regulator and reference current calculation. Also Multiple PWM Generation is used for generating switching signals to force the desired current into the system. Control algorithm as a flow chart in Figure 5.The compensating current of active filter is calculated by sensing the load currents, DC bus voltage, and peak voltage of the AC source (V_{sm}). The instantaneous voltages of AC source can be represented in Eqn. (1).

$$V_{sa(t)} = V_{sm}\times \sin(\omega t) \quad (1)$$

The basic function of the proposed shunt active filter is to eliminate harmonics and also to provide a power injection. After compensating, the AC source feeds fundamental active power component of the load current and losses of inverter for regulating the DC link voltage. Therefore the peak of source reference current (i^*_{sm}) has two components.

The first component is corresponding to the average load active power (i^*_{smp}). The second component of AC source current (i^*_{smd}) is obtained from DC capacitor voltage regulator. Instantaneous power of load (at Kth sample) can be represented as given in the Equation. (2).

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 6.887
Volume 6 Issue IV, April 2018- Available at www.ijraset.com

$P_{load}(k)=V_{sa(k)}I_{la(k)}$ (2)

The average power of load (P_{Lavg}) is obtained by passing P_{load} (k) to low pass filter. The average power of load (P_{Lavg}) is given in the Equation (3) and the number of samples is given in the Equation (4).

$P_{Lavg} = 1/n \sum P_{load(k)}$ (3)

$n=Tf_s; T=1/f$ (4)

Here,f is the fundamental system frequency,$f_s$is the sampling frequency.

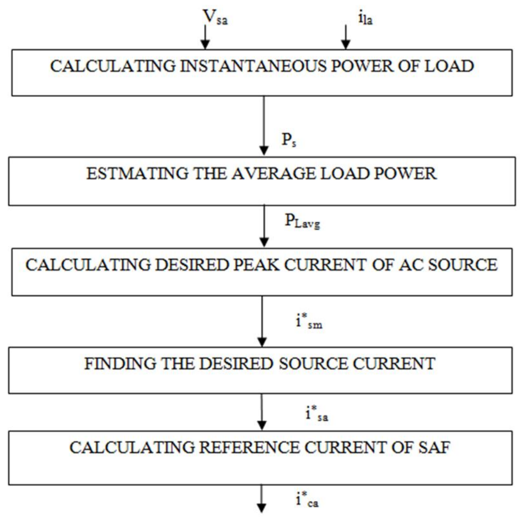


Figure 5 Flow Chart for Reference Current Generation

In order to compensate the current harmonics and reactive power of load, the average active power of AC source must be equal with P_{Lavg}. Considering the unity power factor for AC source side currents the average active power of AC source can be represented as the Equation (5).

$P_s= V_{sm}i^*_{smp}= P_{Lav}$ (5)

In the Equation (6) the first component of AC side current can be represented and named i^*_{smp}.

$i^*_{smp}=P_{Lavg}/V_{sm}$ (6)

The second component of AC source current (i^*_{smd}) is obtained from DC capacitor voltage regulator can be represented as in the Equation (7).

$V^*_{cdc} = V_{dcref} - V_{cdc}$ (7)

This (V^*_{cdc}) will be given to the PI controller and divided by the virtual resistance as stated in [6] to obtain i^*_{smd}. The K_p and T_i values are chosen as 0.345 and 34.9 based on the work done in [7]. The desired peak current of AC source can be given as the Equation (8).

$i^*_{sm} = i^*_{smp}+i^*_{smd}$ (8)

The AC source current must be sinusoidal and in phase with source voltages. Therefore the desired currents of AC source can be calculated by multiplying peak source current to a unity sinusoidal signal. The Equation (9) represents unity signals.

$u_a=V_{sa}/V_{sm}$ (9)

The desired source side current can be represented as given by the Equation (10) and it is denoted as i^*_{sa}.

$i^*_{sa}=i^*_{sm}\times u_a$ (10)

Finally, the reference currents of active filter can be obtained by subtracting the load current from the reference source current. This can be represented as the Equation (11).

$i^*_{ca}=i^*_{sa}-i_{la}$ (11)

This reference current will be given to the switching circuit, i.e., PWM controller for producing the necessary switching pulse to the voltage source inverter. So the voltage source inverter with the closed loop system acts as a controlled current source and produces the exact reference waveform at the output. This output of the shunt active filter compensates the line harmonics and the line current becomes sinusoidal and also injects the power generated.

The Multicarrier PWM technique is simulated as per the circuit shown in the Figure6. In the Figure6, the error signal as reference through the 'In' connection port and the gate signals generated apply to the stages of multilevel inverter through the 'Out'

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 6.887
Volume 6 Issue IV, April 2018- Available at www.ijraset.com

connection port. As stated in [8] inverter with 15-level, 7 carriers with same frequency f_c and the same peak to peak amplitude A_c are disposed. The reference or modulation waveform has peak to peak amplitude A_r and frequency f_r. The reference waveform is compared with carrier signals and if it is greater than a carrier signal, then switch/device correspond to that carrier is switched ON and if the reference is less than carrier signals then device correspond to carrier is switched OFF. The frequency of the reference signal for determining the inverter output frequency f_o and its peak amplitude Ar controls the modulated index M and then in turn the rms output voltage V_o. Here the modulation index is defined as the ratio of amplitude of reference signal to the amplitude of the carrier signal. The rms output voltage can be varied by varying the modulation index M. If δ is the width of each pulse, then the rms output voltage can be found from the Equation (12).

$$V_o = V_s \sqrt{\frac{p\delta}{\pi}} \tag{12}$$

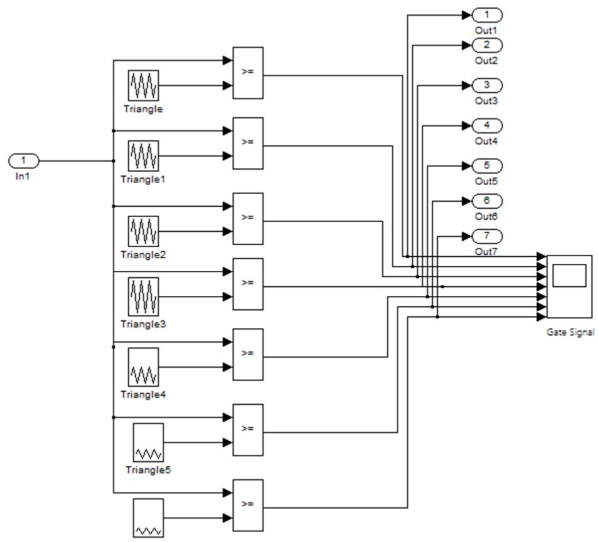


Figure 6 Simulation of Gate Pulse Generation

IV. RESULTS AND DISCUSSION

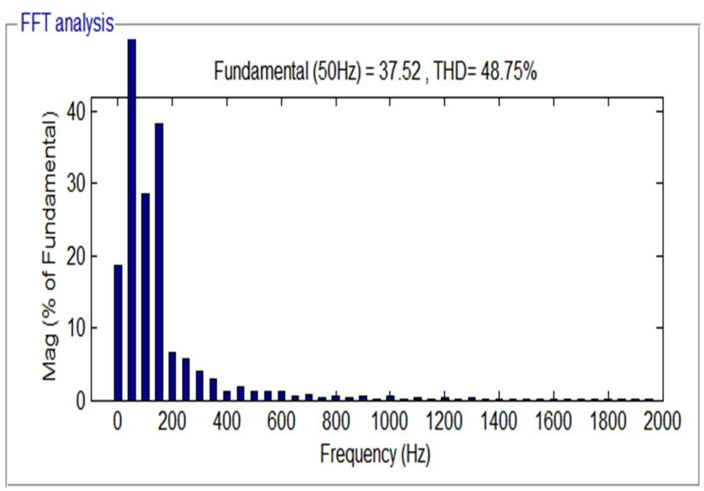


Figure 7 Grid Current Harmonics without filter forPC Load

The harmonics of the grid current waveform when PC load is connected to the grid is shown in the Figure 7. From the Figure 7, it is inferred that the THD of the grid current Waveform is 48.75% due to the non-linearity of PC load, which is above the IEEE standards and it has to be reduced by introducing shunt APF.

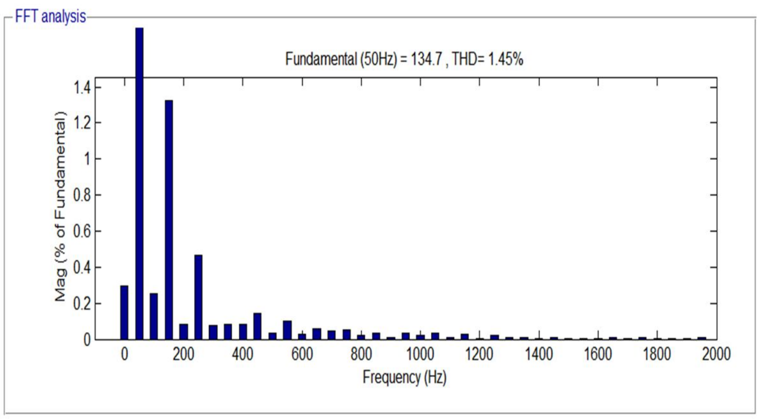


Figure 8 Grid Current Harmonics with Filter for PC Load

From the Figure 8, it is inferred that the THD of the grid current has been reduced to 1.45% which is within the limits of IEEE standards.

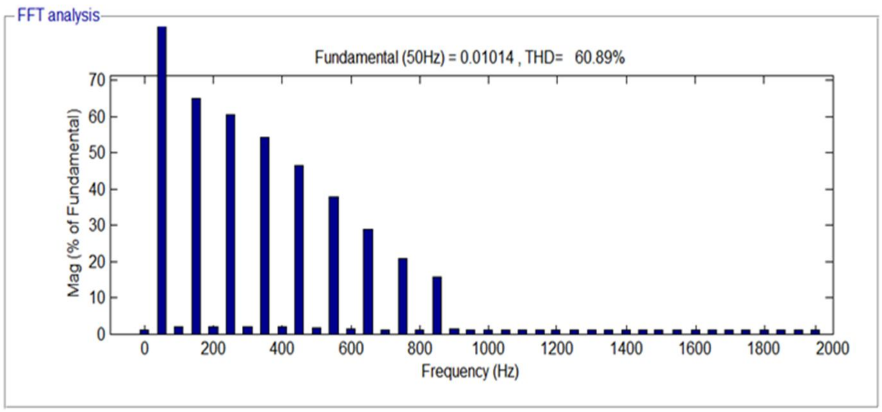


Figure 9 Grid Current Harmonics without filter for Fluorescent Lamp Load

The Figure 9 shows the harmonics present in the grid current when fluorescent lamp is connected to the grid without any filter connected to the grid. The THD of the grid current is observed to be 60.89%.

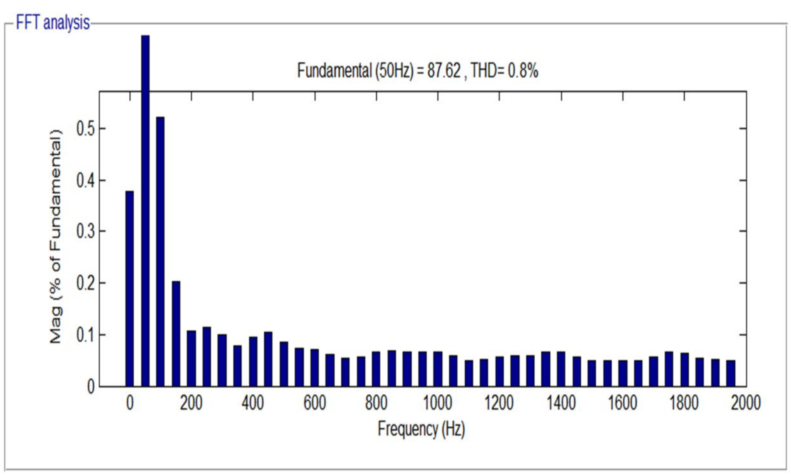


Figure 10 Grid Current Harmonics with Filter for Fluorescent Lamp Load

From the Figure 10, it is inferred that the THD of the source current has been reduced to 0.8% which is within the limits of IEEE standards.

TABLE II CURRENT HARMONICS FOR PC AND FLUORESCENT LAMP LOADS

Load	THD Without Filter (%)	THD With Filter (%)
PC	48.75	1.45
Fluorescent Light	60.89	0.8

From the Table 5.2 it is inferred that after connecting the filter to the grid, the THD of current has been reduced to 0.8% for PC load and THD of current has been reduced to 1.45% for Fluorescent Lamp load.

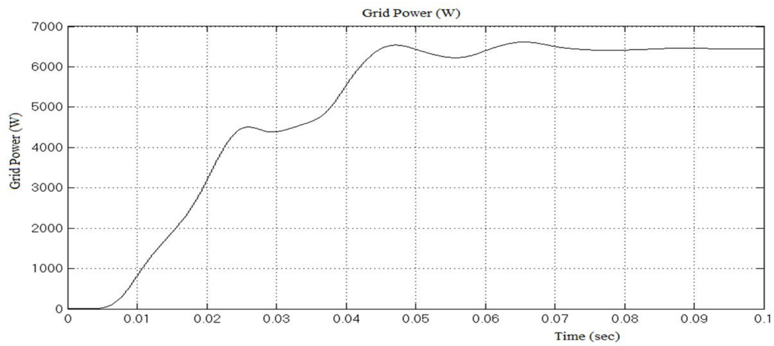


Figure 11 Grid Power without Filter for PC Load

The power in the electricity grid when the Filter is not connected to the load is shown in the Figure 11. It is inferred that the PC load draws 6500W of active power.

Figure 12 Grid Power with Filter for PC load

Figure 12 shows the active power drawn by the load across the electricity grid after connecting the filter to the grid. The active power has been reduced to 2250W after connecting the filter to the grid. The remaining power drawn by the load is fed by the filter.

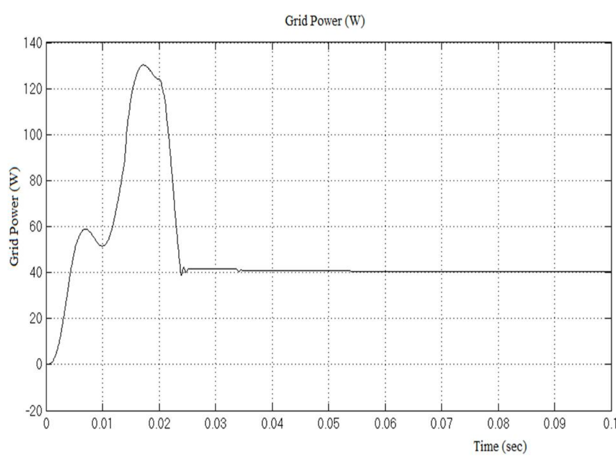


Figure 13 Grid Power without Filter for Fluorescent Lamp Load

The active power of 42W drawn by the fluorescent lamp load when connected across the electricity grid is shown in the Figure 13.

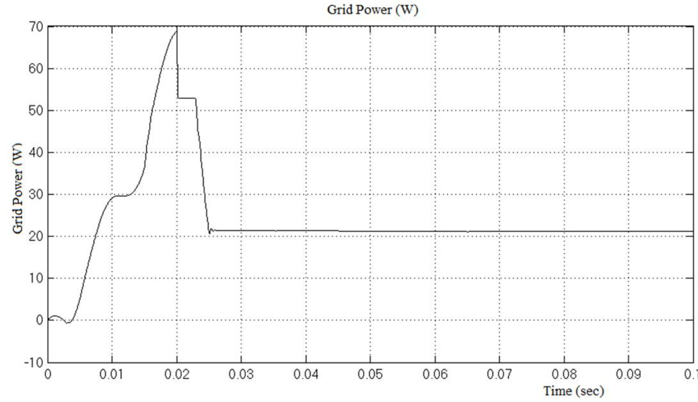


Figure 14 Grid Power with Filter for Fluorescent Lamp Load

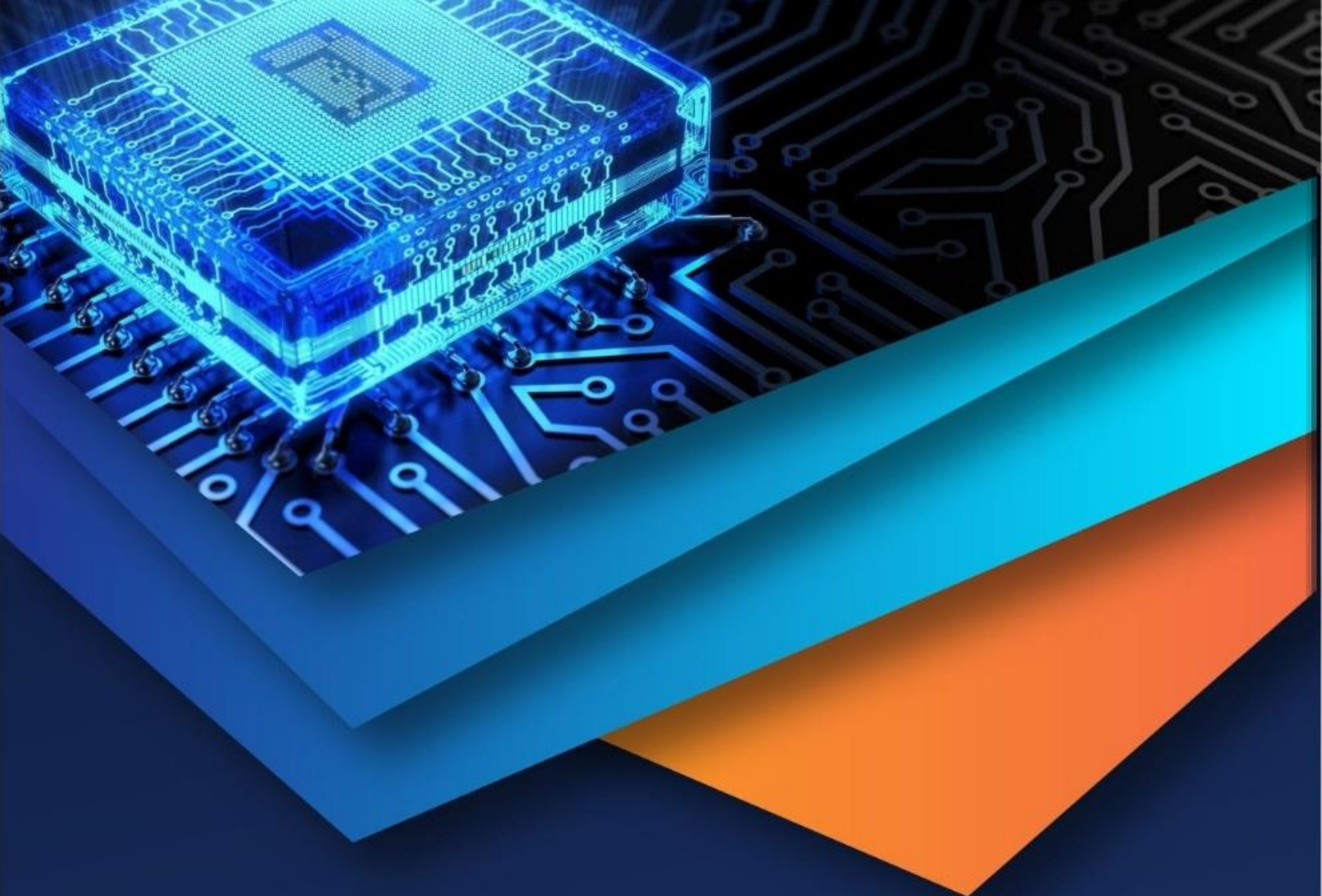
The Figure 14 shows the grid power across the electricity grid drawn by the Fluorescent Lamp Load when filter is connected to the grid. It is inferred that the power supplied from the grid is reduced from 40W to 20W after connecting the filter and it shows that the remaining power is supplied by the filter.

V. CONCLUSION

The grid interfacing inverter has been effectively utilized for power conditioning along with its normal operation of real power transfer. The grid interfacing inverter can be utilized to inject real power generated from RES to the grid and operate as a shunt APF. This method eliminates the need for additional power conditioning equipment to improve the quality of power. Extensive MATLAB- Simulink has been used to validate the proposed method and the results show that the grid - interfacing inverter can be utilized as a multi-function device. The current harmonics are compensated effectively so that the current waveform is improved near to pure sinusoidal. On controlling the proposed multilevel inverter topology, the THD of current has been reduced from 48.75% to 0.8% in case of PC load and from 60.89% to 1.45% in case of fluorescent light which are in the allowable limit of IEEE. This work can be extended to three phase system with the multi-level inverter topology.

REFERENCES

[1] Anooja. C. L, Leena. N (2013), ‘Single Phase Shunt Active Filter with Fuzzy Controller for Harmonic Mitigation’, International Journal of Scientific and Engineering Research, Vol.4 No.9 pp. 445-451.
[2] Borup. U, Blaabjerg. F, Enjeti. P. N (2001), ‘Sharing of Non-Linear Load in Parallel-Connected Three Phase Converters’, IEEE Transactions on Industrial Application, Vol. 37 No.6 pp.1817-1823.
[3] Cervi. M, Seidel. A. R, Bisongo. F. E (2002), ‘Fluorescent Lamp Modelbased on the Equivalent Resistance Variation’, IEEE International Conference on Industrial Applications, Vol.1, pp.680-684
[4] Cesar A. Silva, Leopoldo A. Cordova, Pablo Lezana, Lee Empringham (2011), ‘Implementation and Control of a Hybrid Multilevel Converter with Floating DC Links for Current Waveform Improvement’, IEEE Transactions on Industrial Electronics, Vol.58 No.6 pp.2304-2312.
[5] Enslin. J. H. R, Heskes P. J. M (2004), ‘Harmonic Interaction between a Large Number of Distributed Power Inverrters and the Distribution Network’, IEEE Transactions on Power Electronics, Vol.19, No.6, pp. 1586-1593.
[6] Fang Lin Luo, Hong Ye (2013), ‘Laddered Multilevel DC / AC Inverters Used in Solar Panel Energy Systems’, IET Journal on Power Electronics, Vol.6 No.9, pp. 1769-1777.
[7] JaumeMiret, Miguel Castilla, Josep. M. Gurrero, Juan C. Vasquez (2009), ‘Selective Harmonic Compensation Control for Single-Phase Active Power Filter with Harmonic Rejection’ IEEE Transactions on Industrial Electronics, Vol. 56, No.8, pp.3117-3127.
[8] Jintkosonwit. P, Fujita. H, Akagi. H, Ogasawara. S (2003), ‘Implementation and Performance of Cooperative Control of Shunt Active Filters for Harmonic Damping throughout a Power Distribution System’, IEEE Transactions on Industrial Applications, Vol.39 No.2 pp.556-564.
[9] MdShirajumMunir, Yun Wei Li (2013), ‘Residential Distribution System Harmonic Compensation using PV Interfacing Inverter’, IEEE Transactions on Smart Grid, Vol.4 No.2 pp.816-827.
[10] Mukthiar Singh, VinodKhadkikar, Ambrish Chandra, Rajiv K. Varma (2011), ‘Grid Interconnection of Renewable Energy Sources at the Distribution Level with Power-Quality Improvement Features’, IEEE Transactions on Power Delivery, Vol.26 No.1 pp.307-315.



10.22214/IJRASET

INDEX COPERNICUS
45.98

IMPACT FACTOR:
7.129

TOGETHER WE REACH THE GOAL
IMPACT FACTOR:
7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY