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IC Layout Design of Carry Look ahead Adder at 90nm Technology using GNU/Electric

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Abstract*: *Adder circuits have many applications in addition, multiplication, division, and in address calculation. Carry Look Ahead Adder is one of the most efficient adder since it can conserve the time of propagating the carry bits. In this paper we have discussed the review of design of an Integrated Circuit(IC) layout for different bits of Carry Look Ahead Adder using full custom method with 90nm scaling. The layout will be designed by using an open source software namely Electric-9.07 VLSI EDA tool. In order to produce the layout, the basic knowledge of fabrication process and IC design rule check is necessary. The layout will undergo Design Rule Check set by the Electric VLSI tool to check for any Design Rule Error. Both layout and schematic circuit of CLA were then going to simulate through LVS (Layout Versus Schematic) to ensure they both are identical. LT Spice will be used as a simulator to carry out the simulation work and verifying the validity of the circuit function.
Keywords: Carry Look Ahead Adder (CLA), EDAc, IC Layout, Electric VLSI , LT Spice

I. INTRODUCTION

In the present world the designing of IC's comes with many different tools and some of them are available to us as free open source and few are paid versions. It will be difficult to use paid version tools as not all can able to afford it and generate designs in it. One of the tool which is capable of handling almost all functionalities that are present in advance tools like cadence, mentor graphics etc. is Electric. Electric is one of the most efficient tool which is excellent in performing VLSI design operations like creating schematics, layouts, and many other simulation designs. This tool can also handle hardware description languages like VHDL and Verilog. It also contains the inbuilt simulations like ALS simulation which is more efficient compared to other free source tools available It can also handle many technologies like complementary metal-oxide-semiconductor(CMOS), n-channel MOSFETs, bipolar technologies based on integrated injector logics, newer layout technologies like thin film, carbon nanotubes and photonics etc. this paper has been designed using technology called as MOCMOS technology which is elaborated as MOSIS CMOS technology where the MOSIS is the foundry name and CMOS is the design using complementary MOSFET devices. As the technology improvises, there is an urge for minimizing the transistor size, reducing the delay, improving the efficiency and reducing the overall chip area. In this paper, using the created standard library cell using 90nm technology we have designed the layout for Carry Look Ahead Adder using the above created cells along with generation of GDS file and 3D layout structure.

II. LITERATURE SURVEY

A. System Necessities

Electric is capable of supporting multiple OS and it is written in JAVA and CPP programming languages separately. There are two version of jar file – with or without source code. We are using the version without source code i.e. binary version.

B. Supportive file Formats

Electric has its own specific format of reading and writing circuitry files. Yet, it supports an exhaustive array of file formats to match compatibility with other EDA tools. File formats include Caltech Intermediate Format (CIF), Graphic Database System (GDS II), Electronic Design Interchange Format (EDIF) etc. VHDL and Verilog languages, schematic capture packages like EAGLE, PADS. Output synthesis and Analysis properties are also supported by Electric. Electric has many advanced analysis and synthesis tools including DRC and NCC. DRC tool checks and notifies the user whether the schematic or layout designed is error free or not. It also had the capability of auto correction if few nodes are overlapping by special commands. The NCC check is similar to that of LVS where it continuously checks the schematic with layout that is designed. Compared to other designed tools the NCC check is relatively faster which is in milli-seconds.

C. Advantages of Using Electric

1) No node extraction is present
2) Tools are capable of detecting errors simultaneously along with design process
3) Simpler design process for both schematic and layout.
4) Automatic Icon generation.

III. DESIGN AND IMPLEMENTATION

The process flow for creating a library cell is mentioned below. The generation of CLA schematic was performed first using the logic circuit. After the schematic design the design is made to undergo the DRC check which checks the errors in connectivity of pin overlaps between the nodes or arcs. Once the errors are completely resolved. The basic thing which is necessary in layout design is Lambda rules, based on the lambda rules the designed layout then design is then converted to layout using manual placing of cells from the standard library cell which was created previously and verification process like DRC, LVS is performed.

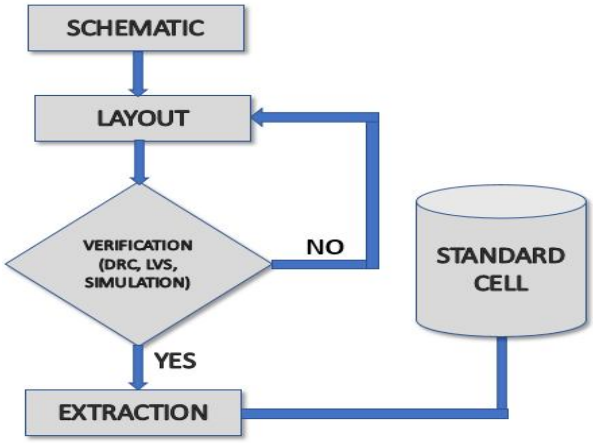

Figure 1: Flow diagram

A. Carry Look Ahead Adder

All the schematic diagrams and layouts of the basic gates drawn have to go through the physical verification process before simulation. These are the essential procedures to ensure the validity outputs results of the system.

Based on the logic diagram of CLA, the schematic circuit and its IC layout was designed using Electric VLSI Design System tool, as shown in Fig. 2 and Fig. 3 respectively.

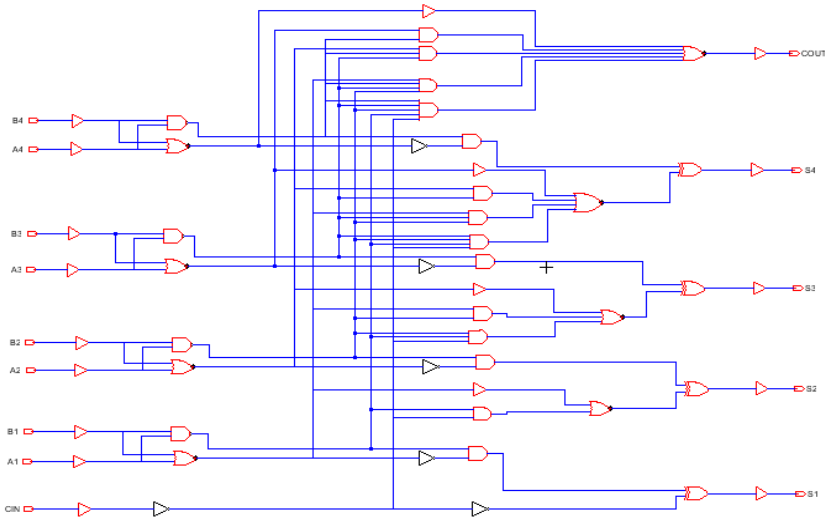

Figure 2: Schematic design of CLA

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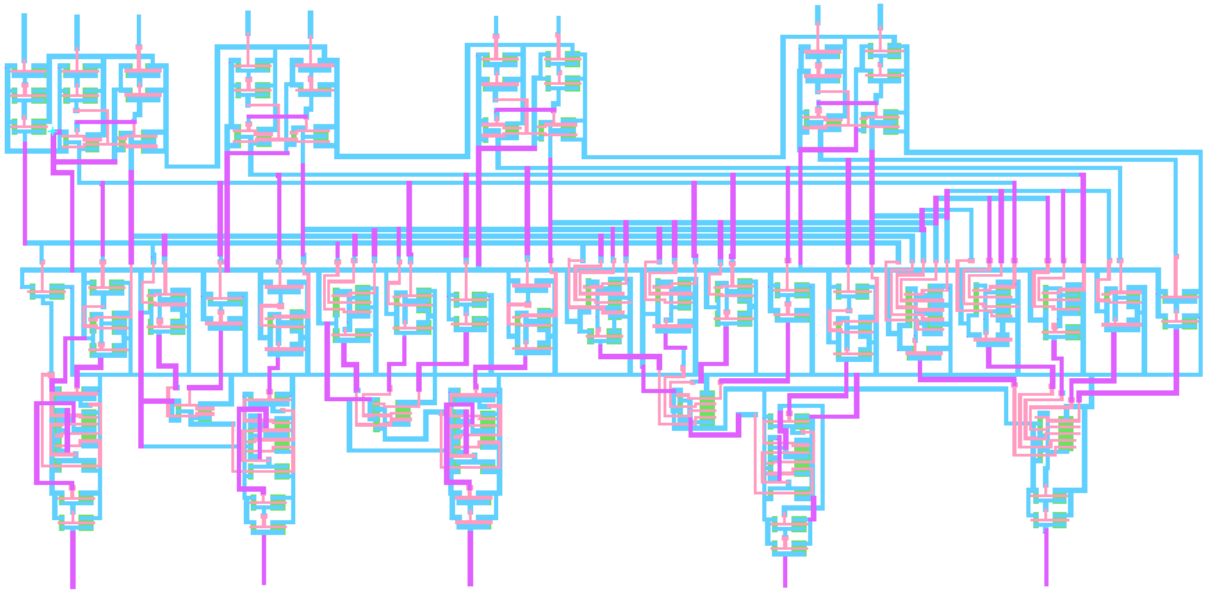

Figure 3: Layout design of CLA

This is a two-level circuit. The study on ripple carry adder results in a limiting factor which is it takes time to propagate the carry. This lead to the development in circuit which is termed to be Carry Look Ahead Adder. This resolves the problem by calculating the carry in
advance with respect to the inputs. The working of CLA can be explained by the manipulation of the boolean expression dealt with full adder.

The Propagate P and Generate G in full adder is given by

Pi = Ai ⊕ Bi Carry propagate

Gi = AiBi Carry generate

These propagate and generate depends on the input bits which will be valid after one gate delay.

The new expressions for the output sum and the carryout are given by:

Si = Pi ⊕ Ci-1

Ci+1= Gi + PiCi

Using these equations for a 4-bit adder:

C1 = G0 + P0C0

C2 = G1 + P1C1 = G1 + P1(G0 + P0C0) = G1 + P1G0 + P1P0C0

C3 = G2 + P2C2 = G2 + P2G1 + P2P1G0 + P2P1P0C0

C4 = G3 + P3C3 = G3 + P3G2 + P3P2G1 + P3P2P1G0 + P3P2P1P0C0

The above equations imply that C2, C3 and C4 does not depend on previous carry in.

Thus, C4 does not need to wait for C3 to propagate. As soon as C0 is computed, C4 can reach into
steady state.

The same is true for C2 and C3.

The general expression is

Ci+1= Gi + PiGi-1 + PiPi-1Gi- 2 + ……. PiPi-1…. P2P1G0 + PiPi-1 …. P1P0C0.

B. 3D view of CLA layout

Electric has an extra special ability to view the designed layout in a 3 dimension. The fascinating part of 3D viewer is that we are able to view the complete structure if the layout which we have designed. When displaying 3D, we can rotate, zoom, and pan the image to get a better view, and once the 3D window is on we can no longer change the circuit. 3D is based on JAVA 3D viewer which is installed in the system.

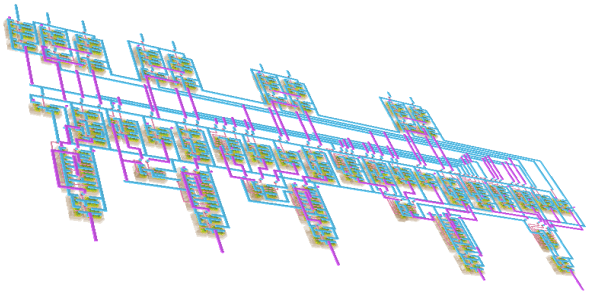

Figure 4: 3D view of CLA

C. Lambda (λ) Rules for Designing IC Layout

Design rules are the basic parameters which is to be followed before implementing the circuit onto the silicon wafer. It allows translation of circuits (usually in stick diagram or symbolic form) into actual geometry in silicon. It also acts as a interface between the layout designer and the fabricator. Design rules also specify geometry of masks that provide reasonable yield.

In the figure we can observe that that the spacing between metal layer and polysilicon is designed based on lambda rules. The spacing between two metal-1 should be 3 λ. The spacing between two polysilicon's should be 3 λ. The metal layer and the polysilicon layer can overlap each other as they come in different layers during fabrication. The separation between the contacts should be 3 λ, with contacts having an area of 2 λ*2 λ.

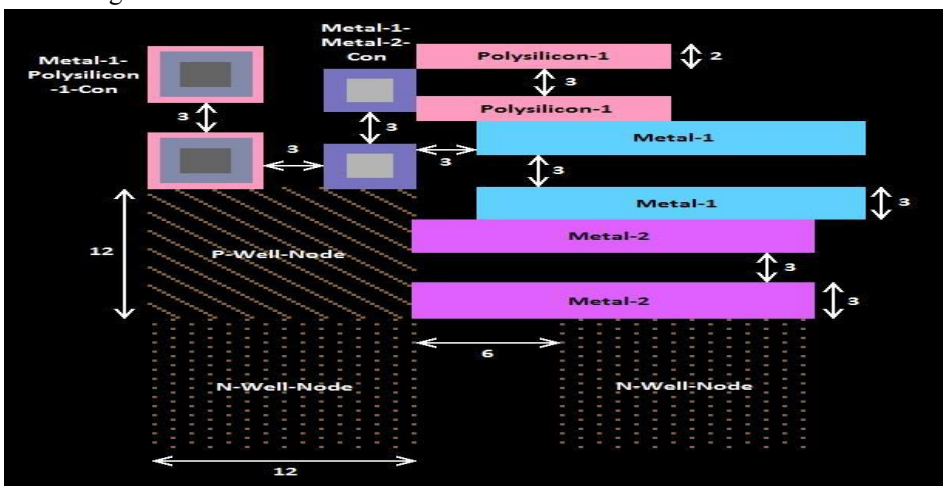

Figure 5: Lambda based rules

IV. GDSII FILE VIEWER

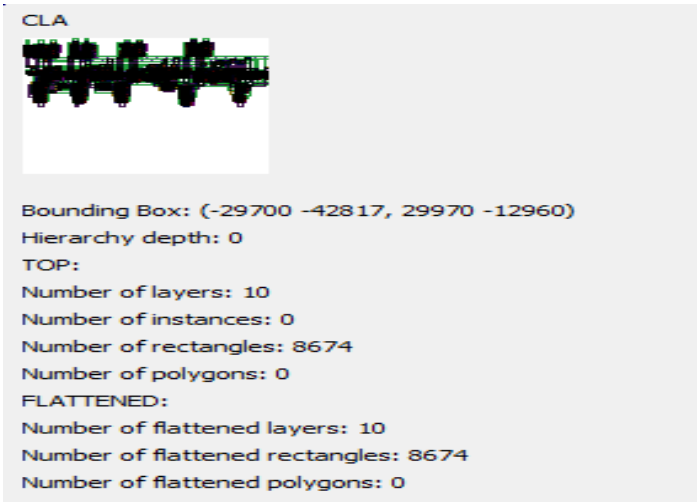

Figure 6: GDS File format

GDSII is a database file format which is the industry standards for creation of the integrated circuit. The GDSII file is in binary format as the creation of layout is finished the layout file is been exported from jelib format file to gds file and this GDS file format which is in binary form is then given to the foundry for the fabrication of the IC's.

V. RESULT ANALYSIS

From the table given below fig 11, we can show the outputs that will be obtained from CLA circuit which we have designed and the layout for the above takes less area means lesser power dissipation and also lesser heat dissipation. Hence a large number of chips can be integrated into a small area also, the rise time and fall time of the circuits are less. This will lead to faster execution with only a little delay.

A	B	Ci	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 1: Full adder logical output

VI. CONCLUSION

A standard library cell using 90nm technology was created which includes Basic gates and universal gates. This cell can be used in complex circuit design. By the use of standard cell, we have successfully created a layout for CLA at 90nm technology and we have also verified the DRC and LVS checks. CLA reduces the propagation delay by introducing more complex hardware. From the table it can be concluded that there is a substantial amount of reduction in these parameters when compared to past sub-micron technologies. Further, standard library cells can be designed in Electric VLSI design system using 45nm technology, carbon nano-tubes also.

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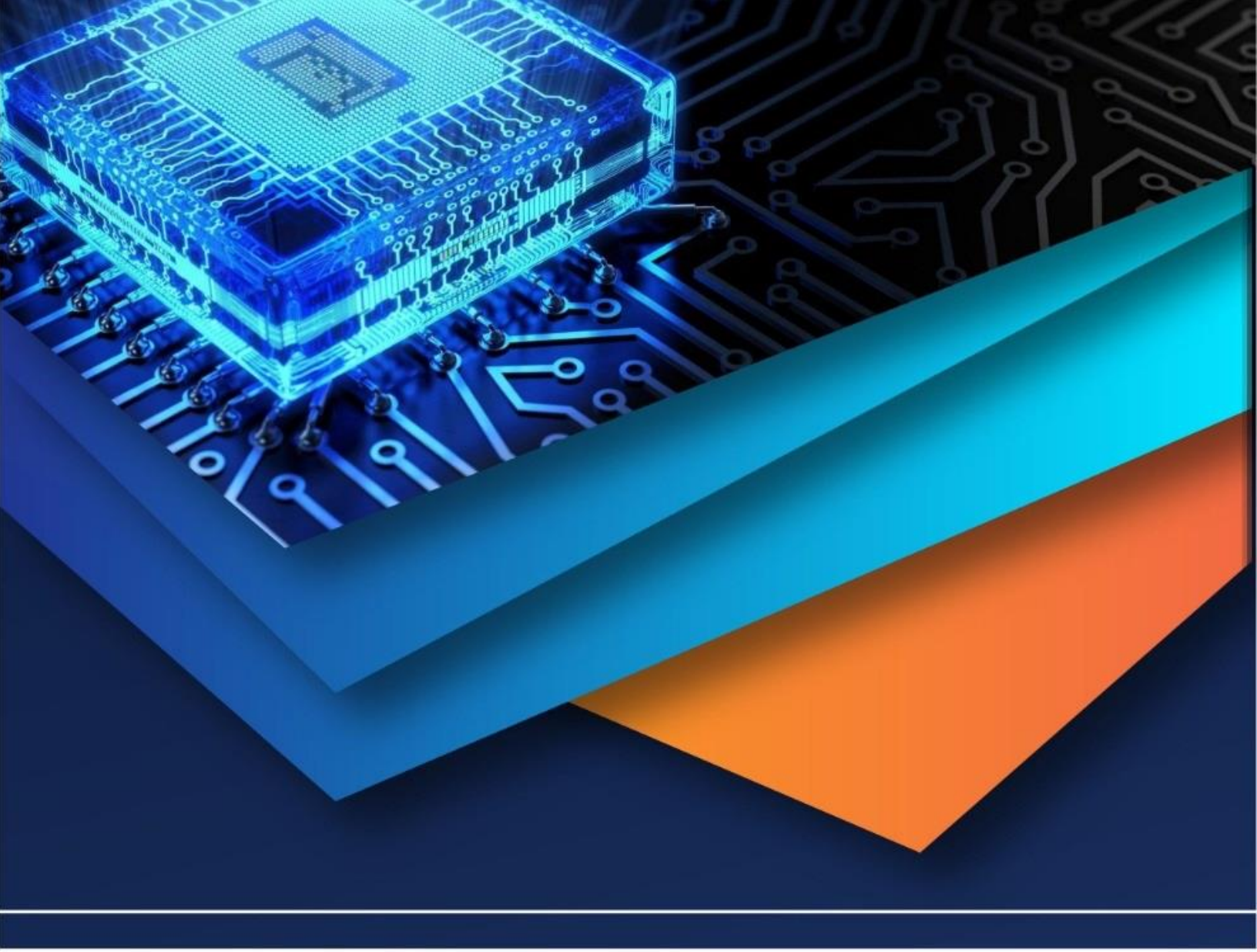

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