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Improvement of Power Quality of Boost Converter using Proportional Integral (P-I) Controller

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Abstract*: This manuscript presents a power factor correction based only key in lone output based converter with bargain add up to semiconductor device. In this anticipated converter on its own exchange is second-hand to corrected record output boost converter has enhanced warrant reason of the system and look up purgative excellence at enter AC mains. The anticipated converter is analyzed on MATLAB / SIMULINK platform and results are presented in this term paper.
Keywords: Power factor correction, lone boost converter/ dual-boost converter, AC-DC converter, anticipated converter.

I. INTRODUCTION

In existing years, the necessity of pure energy is increase hurriedly and with the energy is increase hurriedly and with the excellent progress of electronics technologies habit of AC-DC warrant/strength converter system has been adapted to a broad array of application that consist of industrial residential and commercial and railway grip system, nearly all of applications such that laptops, desktops, SMPS &, VPSS and VFD desired DC resources.

The global power quality principle like IEC 6000-3-2 or European line up current harmonics confines ISC 1000-3-2 and IEEE 579. Standard provides guidelines for nation property principle for AC-DC warrant convert less [1]-[2]. To endure the above said principle, the power factor correction (PFC) becomes a segregate of potential part of electronics converters.

For power factors correction (PFC) a number of passive and in force approaches exhibit been power for linear heaps as passive filters are especially responsive to mutually frequency and load, therefore these filters may not react hastily if the load power factor issue comes to vary.

The amplified mass, magnitude and volume are bonus drawbacks of passive PFC based converters systems. Instead of passive PFC we are using active PFC techniques which provide more reliable and effective liquid by providing controlled solid-state switches in tie with passive quantity (resistors, inductors and capacitors).

Passive PFC circuits are heavier and larger [4]-[7]. A continues inductor current mode (CICM) operated boost converter has been broadly established for power factor correction (PFC).

The boost converter is ideal among another active PFC topologies appropriate to its high power factors (HPF), high power transfer capability and low electromagnetic interference (EMI) fallout at high input mains consequences at effort mains, condensed THD, extraordinary efficiency and low price bulk of machinery[8]-[9].

In this manuscript a power quality increased lone input lone output boost converter with bargain mechanism is presented. The output of both boost converters is controlled by using MOSFET switch. This PFC convert posses a climax control feature (0.96) and THD in track down (source) current a reduced amount of than 8%.

II. . CONFIGURATION OF PROPOSED CONVERTER

This portion of paper represents the plan of the new planned converter topologies. Originated equations are offered and the value of components is established. The interrelated topology of the planned power factor corrected single input lone output boost convertor is offered shown in [10]. This DC to DC topology formerly customized into PFC based lone input lone output boost converter (converter I) which is given in figure 1.

This adapted PFC based lone input lone output boost converter topology transformed into new reduced semiconductor components which is shown in figure 2.The converter system consists of participation enablement source diode bridge rectifier / diode link rectifier, two boost converter units fixed in series, two boost inductors (Lb1, Lb2), two boost diodes (Db1 , Db2), one MOSFET switch, two capacitors(Ca1, Ca2) and one lead(L1).

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A. Circuit Diagram

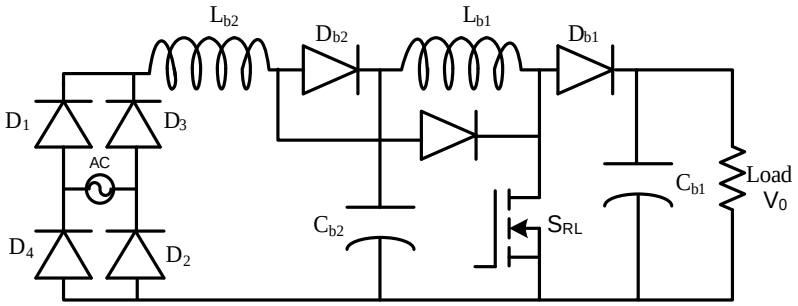

Fig.1 Layout of single input single output boost converter.

Specification of proposed converter system

Input voltage	175 V_{ac}-240 V_{ac}
Output voltage	390 V_{dc}
Lead	400W for each converter
Switching frequency	50Hz
Inductor ripple current	10%
Output voltage ripple	10V
Hold-up time	30MS at 370V

The aim of completely machinery of the converter system.
i.e. boost inductors(L_{b1}, L_{b2}), output capacitor(C_{o1}) and a filter capacitor(C_f) are calculated as follows:

A. Design of Filter Inductor (LF)

The filter inductor (LF) rate is firm based on the maximum inductor current ripple. The equation of filter inductor is articulated as follows-

$$Lf = \frac{1}{\%Ripple}.\frac{Vac.min^2}{Po}.\left\{1-\sqrt{2}.\frac{Vac.min}{Vo}\right\}.T$$

Now substituting all the values in eq.1, we get

$$Lf = 3116\mu H = 3.116mH$$

So, due to simple availability the rate of this filter inductor is ideal from 3mH to 4mH.F

B. Design of Boost Inductor ($L_{b1,}$ L_{b2})

Value of boost inductors

$$Lb1 = Lb2 = \left[\frac{Vin(Vdc-Vin)}{fsw.\Delta Ic.Vdc}\right]$$

$$Lb1 = Lb2 = 5.319mH$$

So, the value of inductors that we will use for this circuit should lie between 5mH to 6mH.

C. Design of output Capacitor (C_{o1})

The output capacitor is considered to endure hold up time and voltage ripple requirement.
The value of capacitor is calculated as follows:

$$Co1 \geq \frac{2Po\ thold}{(Vdc^2 - Vdc.min^2)}$$

$$Co1 \geq 3116\mu F$$

So, the value of capacitor is calculated as follows

$$Co1 \geq \frac{Po}{2\pi fline\Delta Vdc\ Vdc}$$

Substituting all the values in above equation, we get

$$Co1 = 3266\mu F$$

Therefore, the output capacitor is elected of bigger value of 3116μF but appointed to promote availability the value of output capacitor will be selected as 3200μF.

III. CONTROL APPROACH

In this manuscript, the mean current mode control proposal is used for proposed power factor corrected lone input lone output boost converter to complete harmonics fewer than 8%.

The mean current mode control (MCMC) invent consists of a PI (Proportional Integral) convert controller, a PI voltage controller, suggestion current generation and at last the PWM generation and power MOSFET for providing switching signals. A proportional Integral (PI) is used for voltage source and it is preferred to control the output voltage. The source voltage (Vdel) is after that compared with set reference voltage (Vref). The consequential voltage fault (Vern) at the nth moment is shown in below equation.

$$Ve(n) = Vref(n) - Vdc1(n)$$

And hence the output of the proportional integral(PI) of a voltage controller at the nth sampling instantaneous can be shown as in the below equation.

$$Ic(n) = Ic(n-1) + Kp\{Ve(n) - Ve(n-1)\} + Ki.Ve(n)$$

When, Kp and Ki represents the integral and proportional gains of PI voltage controller.

A Proportional Integral of current source controller is select/chosen to insist the input alternating current (AC) mains current to admire the input waveform of voltage which fallout in unity power factor and lesser the harmonics of current. To perquisite up the power factor, the current signal must be equivalent to the rectified voltage as accurately as feasible. The output of proportional integral (PI) voltage controller is multiplied with the sensed rectified voltage (Vref) and consequential signals forms the recommendation for input current as in below given equation

$$Iref(n) = Ic(n) * Vrec$$

V_{rec} represents the sensed rectified voltage.

The consequential current error $I_c(n)$ at nth sampling instantaneous after comparing the reference current ($I_{rec)}$ and that current error $I_{c(}n)$ is shown in below equation

$$Ie(n) = Iref * (n) - Irec$$

The output of proportional integral (PI) of current controller is at the nth sampling instantaneous is given `as

$$Iavg(n) = Ic(n-1) + Kp\{Ie(n) - Ie(n-1)\} + Ki.Ie(n)$$

Here, in proportional integral the K_P and K_i are the proportional gain and integral of voltage controller.

This current signal is next compared with present frequency carrier signal for solid state power MOSFET switch of the projected power factor corrected lone input lone output boost converter topology.

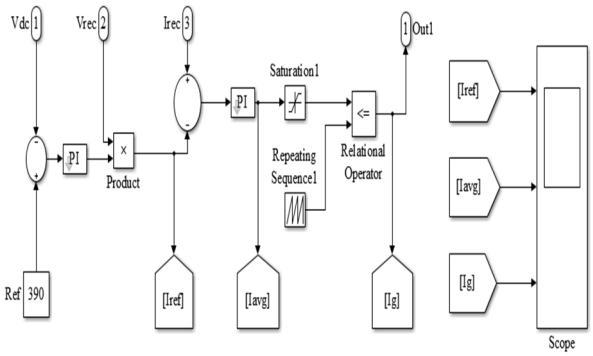

Fig 2Controller of this proposed converter.

IV. SIMULATION MODEL, RESULTS AND DISCUSSIONS

The modeling and simulation is designed to legalize the design of anticipated power factor corrected single input single output boost converter which has better the power factor of the system and enhance power quality at contribution to AC mains. The anticipated power factor corrected single input single output converter is simulated on MATLAB .The model is exposed in fig 3. The boost converter pattern operated at high switching frequency of 50 kHz fig3 gives you an idea about the simulated presentation of converter.

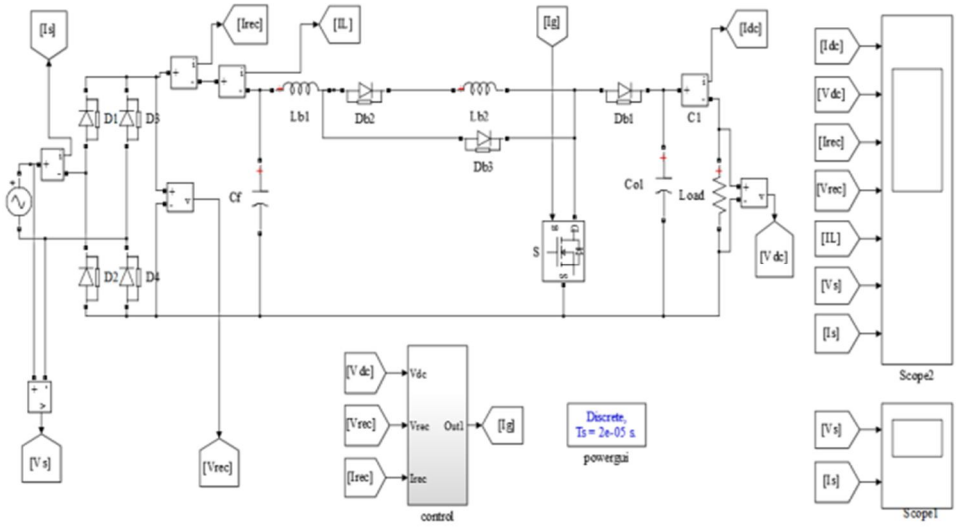

Fig3. Simulation model of correction of power quality of single input single output boost converter.

This below figure represent the simulation model of proposed converter system. This simulation made consist of control and scopes. Here scope 2 consist of I_{dc} as a voltage current ,V_{dc} as a output voltage, I_{rec} as a rectifier current, V_{rec} rectifier voltage, I_L as a load current, Is as a source current, Vs as a source voltage. Scope 1 represents the current and voltage of source side. And this contains the harmonics distortions less than 8%. The simulation waveforms are given as follows:

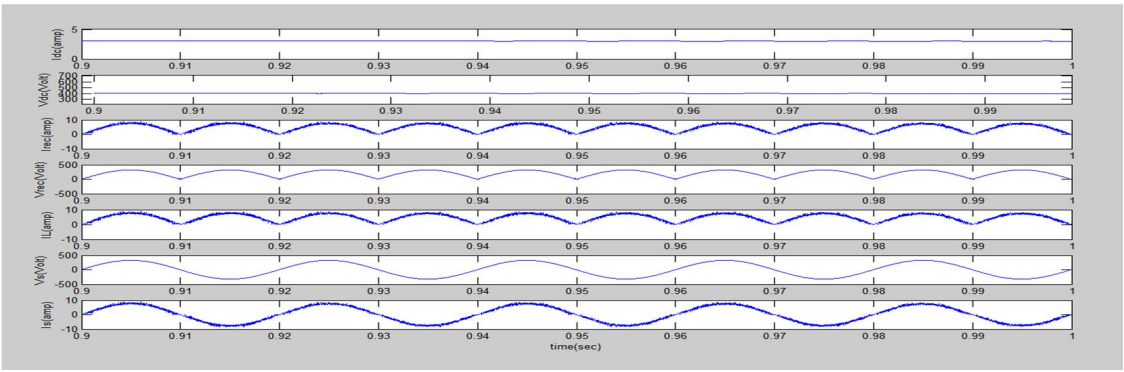

Fig4:Output waveforms of simulation of single input-single output boost converter with R load

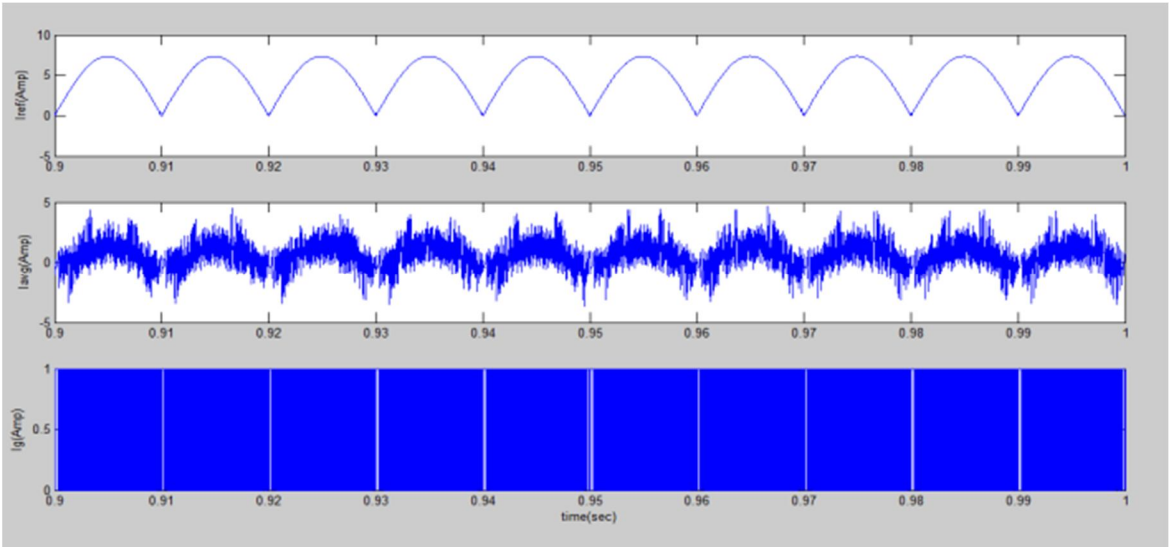

Fig5: Simulation results of PI controller with average current mode control scheme

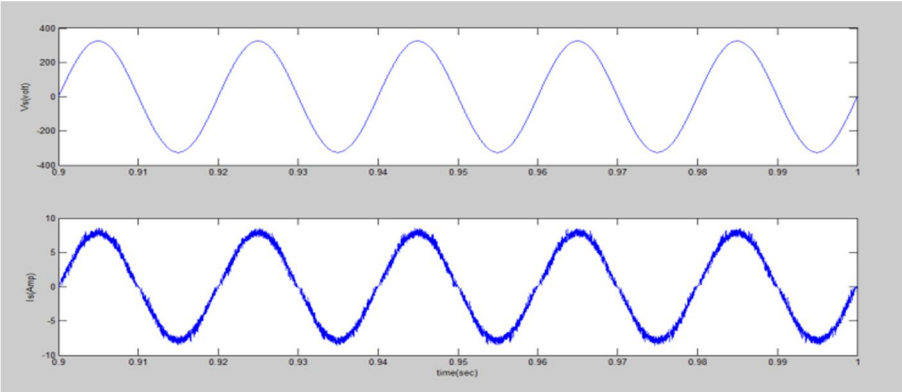

Fig6: Simulation results of input of single input single output boost converter

V. CONCLUSIONS

In this manuscript a energy trait better single input single output boost converter with abridged components is introduced. Mutually the converters having the single input .So, they are obsessed by on its own MOSFET switch. This energy caused corrected converter shown a better power factor of 0.96 and THD in source current is established to be not as much of as 5% consequently conflicting IEEE standards.

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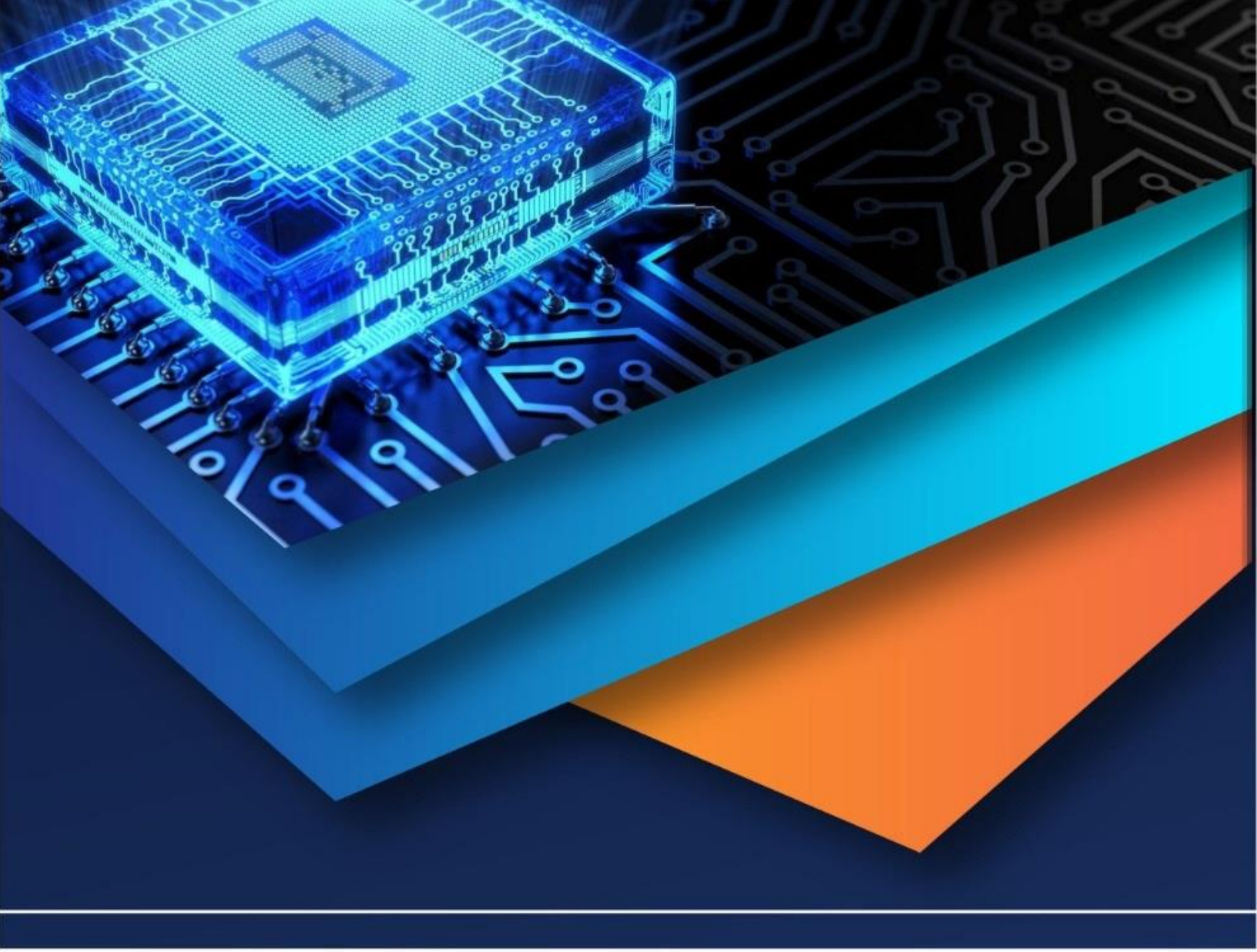

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