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Cascaded Switched Diode Capacitor Voltage Accumulated Multi-Level Inverter

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Abstract: ***Multilevel inverters are the one which converts DC voltage into several levels of AC output voltage. It includes an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages. As the output voltage level increases, the output harmonic content of such inverters decreases, allowing the use of smaller output filters. Here cascaded SDCVA multi-level inverter is proposed. It will generate boosted output voltage, by switching the capacitors in series and in parallel. Also the number of levels can be increased by cascading the SDCVA cells. Level shifted Sinusoidal Pulse Width Modulation (SPWM) technique is used to generate the switching pulses. Simulations are carried out in MATLAB 17/Simulink software. For an input voltage of 80V DC 230V RMS is obtained. The THD of the inverter is found to be 13.93%. Control strategy is implemented using Arduino 2560. Driver circuit for switches are fabricated in PCB. The prototype of proposed inverter is implemented and output is verified. The inverter can be extended for Hybrid Renewable Energy Generation System application.***
Keywords: Nine level inverter, SDCVA, SPWM, cascaded inverter, PD-PWM

I. INTRODUCTION

Over the last four decades multilevel technology has received a great deal of attention and popularity among both researchers and industry for their inherent property of increasing the voltage level and improving power quality. Multilevel inverters (MLIs) are power electronic converters that consist of several input DC sources or capacitors and switching elements such as active switches, power diodes and drivers which achieves proper output voltage with appropriate quality by a suitable switching pattern [10]. The quality of output voltage waveform depends on the number of inverters voltage levels; as the number of output voltage level increases it become more close to sine wave and thus reduces THD. Multi-level inverter offers several advantages over two level inverter: it improves the output voltage waveform, reduced (dv/dt) voltage stress on the load and also reduces electromagnetic interference problems. But it has some disadvantages when the number of voltage levels increases such as; complex PWM controlling method, voltage balancing problems are introduced and higher number of semiconductor switches are required [3]. There may be a single DC voltage source or multiple sources can be used depending on the inverter configuration. For single-phase multilevel inverters(MLIs), the most common topologies are the diode clamped MLI, flying capacitor MLI(FCMLI) and the cascaded multilevel inverter(CMLI) which includes symmetric and asymmetric types depending on the value of input DC supplies. In symmetrical method all the DC sources voltage have unique value and it ensures good modularity. Different rating of switches are required in asymmetrical method due to different DC sources voltage magnitude, this may generate high number of output voltage with minimum DC source. But multilevel inverter modularity may reduce. CMLI synthesises the staircase AC voltage waveform from several DC sources with reduced harmonic content . Therefore the CMLI configuration is more attractive than other two configurations. Overall, the above mentioned multilevel topologies only can realize the voltage step-down inversion, i.e., the AC voltage amplitude cannot exceed the input DC voltage. A transformerless architecture is competent since it reduces the system cost and weight and realizes the voltage step up inversion [5]. The step up converter can be realised in many ways by using diode capacitor cell and coupled inductors or with simple boost converters etc. Here a cascaded structure consisting of switched diode capacitor voltage accumulator(SDCVA) is used. This ensures the output voltage greater than input voltage. The modulation methods used in multilevel inverters can be classified according to switching frequency, they are fundamental switching frequency and high switching frequency PWM. Space Vector Control and Selective Harmonic Elimination are coming under fundamental switching frequency and Space Vector PWM and Sinusoidal PWM are under high switching frequency PWM. This nine level inverter make use of level-shift multicarrier based pulse width modulation method which is one among the Sinusoidal PWM techniques and is classified into three types In Phase Disposition (IPD), Phase Opposition Disposition (POD), Alternate Phase Opposition Disposition (APOD) [2].

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In order to overcome the difficulties of the classical multilevel inverters and to ensure voltage step-up inversion a cascaded SDCVA nine level inverter is proposed. It makes use of a switch-diode-capacitor cell. Compared to the conventional cascaded topologies it uses reduced number of power switches, diodes and DC sources. The following table shows the comparison of existing nine level topologies with the proposed one.

TABLE I COMPARISON

Inverter Type	DC Source	Capacitor	Active Switch
CHB	4	0	16
NPC without voltage control	7	0	16
Reversing voltage topology[3]	4	0	12
Extended topology[7]	2	4	16
Proposed Topology	2	4	10

II. CASCADED SDCVA NINE LEVEL INVERTER

The inverter topology proposed here make use of two SDCVA units cascaded with two separate voltage sources which gives nine level output voltage. It generates boosted output by switching the capacitors in series and parallel. One of the significant advantages of this multilevel configuration is that it can be extended to any number of levels by cascading the SDCVA cells. As the number of voltage levels increases, there is more decrease in harmonic content of the output voltage waveform.

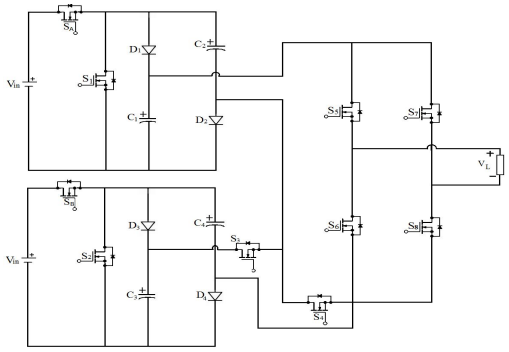


Fig. 1.Proposed Nine-Level Inverter

III.MODES OF OPERATION

There are mainly 10 modes of operation for this nine level inverter. Five are for positive half cycle and remaining five are for negative half cycle. Depending on the ON and OFF position of switch S_1 and S_2 capacitors C_1, C_2, C_3 and C_4 will be connected either in series or in parallel. When switch S_1 is turned on, diodes D_1 and D_2 are reverse biased, capacitors C_1 and C_2 will discharge in series. When switch S_1 is turned OFF, diodes D_1 and D_2 are turned on, capacitors C_1 and C_2 get charged in parallel. The same will be done if switch S_2 is turned ON and OFF. Switches S_3 and S_4 are used to switch between upper and lower SDCVA cells. Operating modes are shown in Fig. 2.

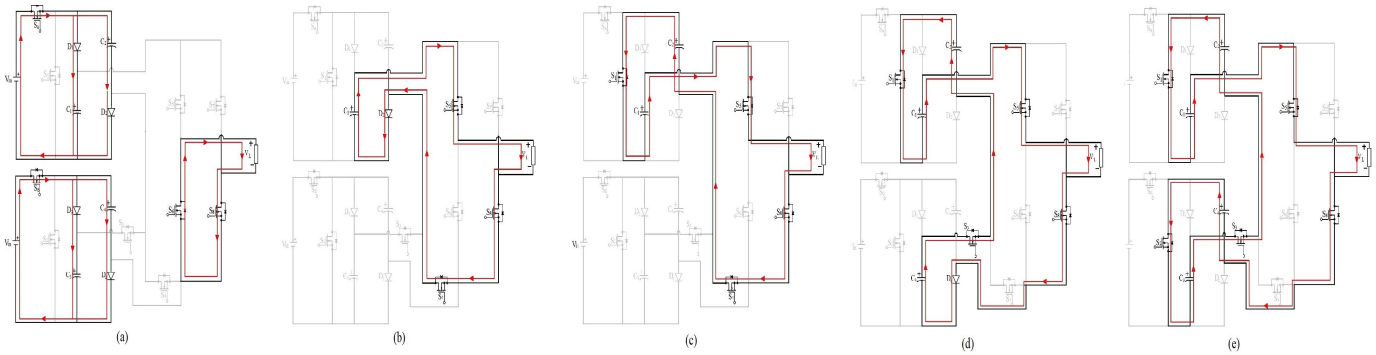


Fig. 2.Modes of Operation (a) Mode 1 (b) Mode 2 (c) Mode 3 (d) Mode 4 (e) Mode 5

IV. MODULATION TECHNIQUE

The modulation technique employed in this system is Phase Disposition PWM(PD-PWM) which is shown in Fig. 3. The PD-PWM method is one of the carrier-based PWM methods and implementation is based on a comparison of a reference waveform with vertically shifted carrier waveforms. In phase disposition method all the carriers are in phase with each other and all carrier signals are having same amplitude and frequency. This method uses N-1 carrier signals to generate the N-level inverter output voltage. Here eight carriers each of frequency 15kHz and modulating signal of frequency 50Hz is used. Switching pulses are generated by using relational operators and logical operators.

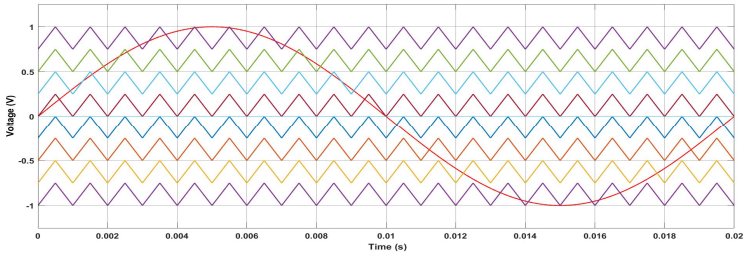


Fig. 3. PD PWM

V. SIMULATION STUDIES

The simulation study of proposed multi-level inverter is performed in MATLAB R2017a software. For an output of 230V rms, two DC voltage sources of 80V each is used. The switching frequency is 15kHZ and modulating signal frequency is 50Hz. Capacitors are selected according to the allowable ripples of 5 percentages in the capacitor voltage and it is selected as 2200 µF.

A. Simulink Model and Results

The detailed MATLAB/Simulink model for cascaded SDCVA multi-level inverter is shown in Fig. 4. The four switches(S_5-S_8) in H bridge work at high frequency while the remaining switches work at low frequency (50 Hz), which helps to reduce the switching losses. S_3 and S_4 are used to switch between upper and lower SDCVA cells. The switching pulses are generated by using relational and logical operators along with repeating sequence stair block in MATLAB.

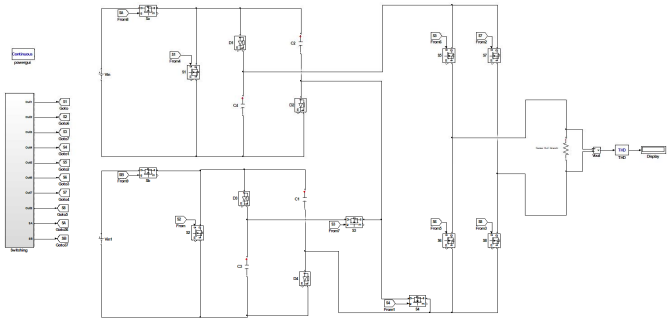
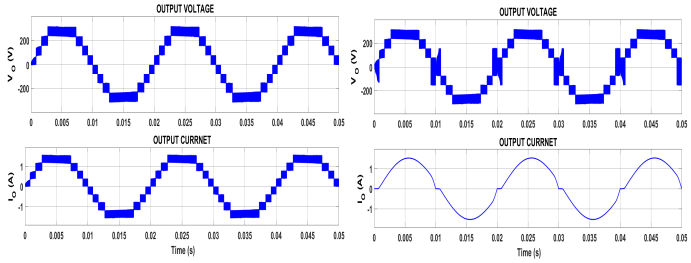


Fig. 4. Matlab model of Cascaded SDCVA Multi Level Inverter

All the four capacitors C_1, C_2, C_3 and C_4 are equally charged to supply voltage. There is no unbalancing problems in the capacitor voltage. The output voltage and current waveforms for R and RL load are shown in the Fig. 5. With RL load of power factor 0.96(R=200Ω, L=130mH) small spikes are appearing in the voltage waveform, due to the presence of inductance.



(a) (b)

Fig. 5. Output Voltage and Current (a) R Load (b) RL Load

B. Simulation Analysis

PD-PWM technique has been employed in the cascaded SDCVA multi-level inverter. A THD of 13.93% obtained for the inverter. The FFT analysis is shown in the Fig. 6. From the analysis 3rd, 5th and 7th order harmonics are predominant in the output voltage waveform.

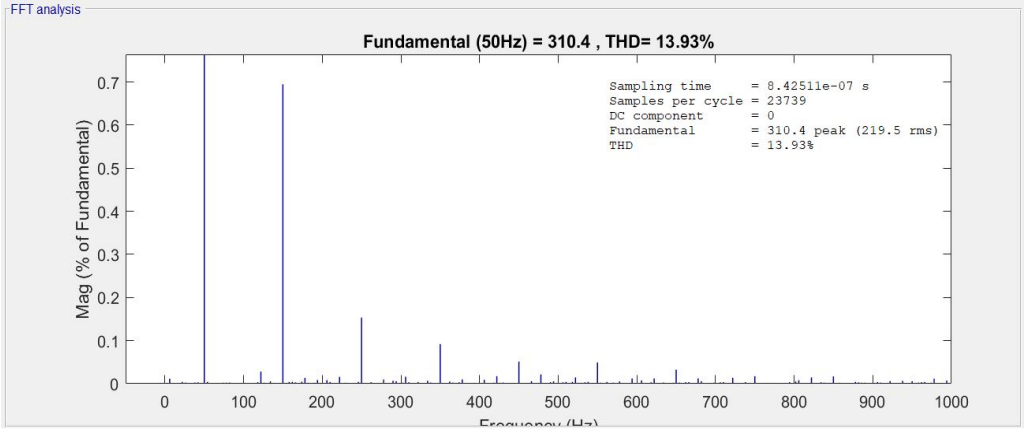


Fig. 6.FFT Analysis

The variation of efficiency with load resistance is shown in the Fig. 7. Efficiency increases to a value of 95.24% and then shows a decreasing trend and become constant near 900Ω.

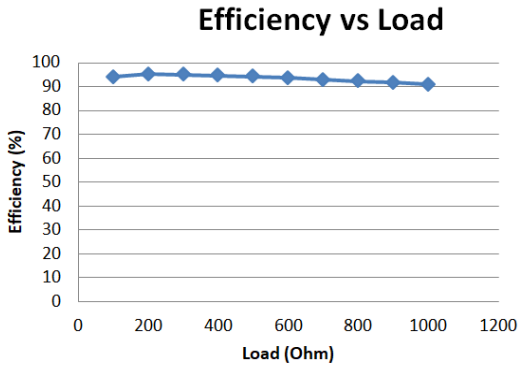


Fig. 7.Efficiency vs Load

The variation of THD load resistance are shown in Fig. 8. Change in the load resistance can affect the THD of output. From the analysis it can be seen that by using resistance higher than 100Ω is used the THD became constant and independent of load resistance.

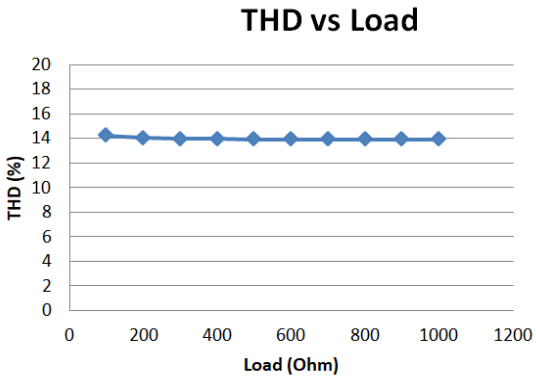


Fig. 8.THD vs Load

VI. HARDWARE IMPLEMENTATION

For validating the simulation results the hardware implementation of the proposed inverter is done. The prototype of proposed inverter is done with an input voltage of 18V to each SDCVA cells. The figure shows the experimental setup of the inverter. The cascaded nine level inverter consist of two isolated sources, 8 capacitors and ten MOSFET switches IRF 540. The control pulses are generated using Aurduino mega 2560 micro controller and are given to appropriate switches. Isolation between driver and power circuit are provided by opto-coupler TLP 250.

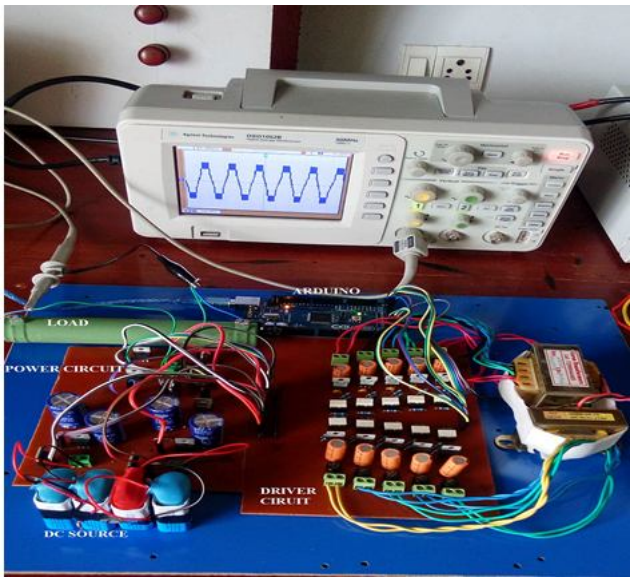


Fig. 9.Experimental Setup

The output obtained from DSO is shown in Fig. 10. From the experimental setup we can assure the hardware is working properly. Due to the switching losses the output voltage is 62.4V instead of 72V.

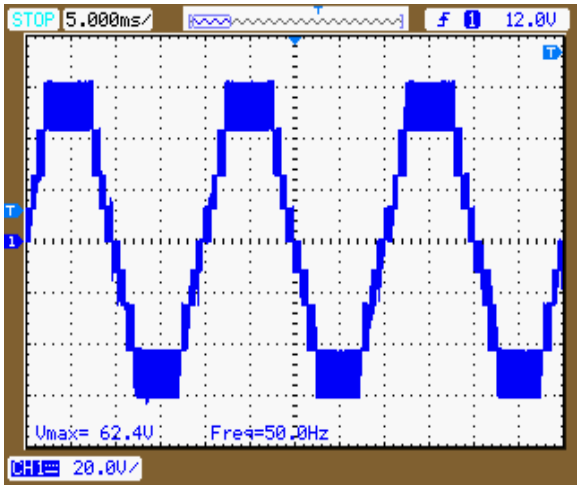


Fig. 10. Experimental Output

VII. CONCLUSIONS

In this work cascaded switched diode capacitor voltage accumulated (SDCVA) multi-level inverter is proposed. Various simulation studies are performed and hardware implementation validates the simulation results. Compared to the existing cascaded topologies the component count is less for the proposed inverter. The minimum THD obtained is 13.93% with PD-PWM technique. The maximum simulation efficiency obtained is 95.24% and maximum output voltage obtained is four times the input voltage of a single cell. The SDCVA cells can be cascaded for higher number of output levels. For an input voltage of 18V to each SDCVA cell output voltage of 62.4V is obtained. N number of cells will give 4N+1 number of levels in output. The inverter is suitable for hybrid renewable energy system applications which make use multiple input sources.

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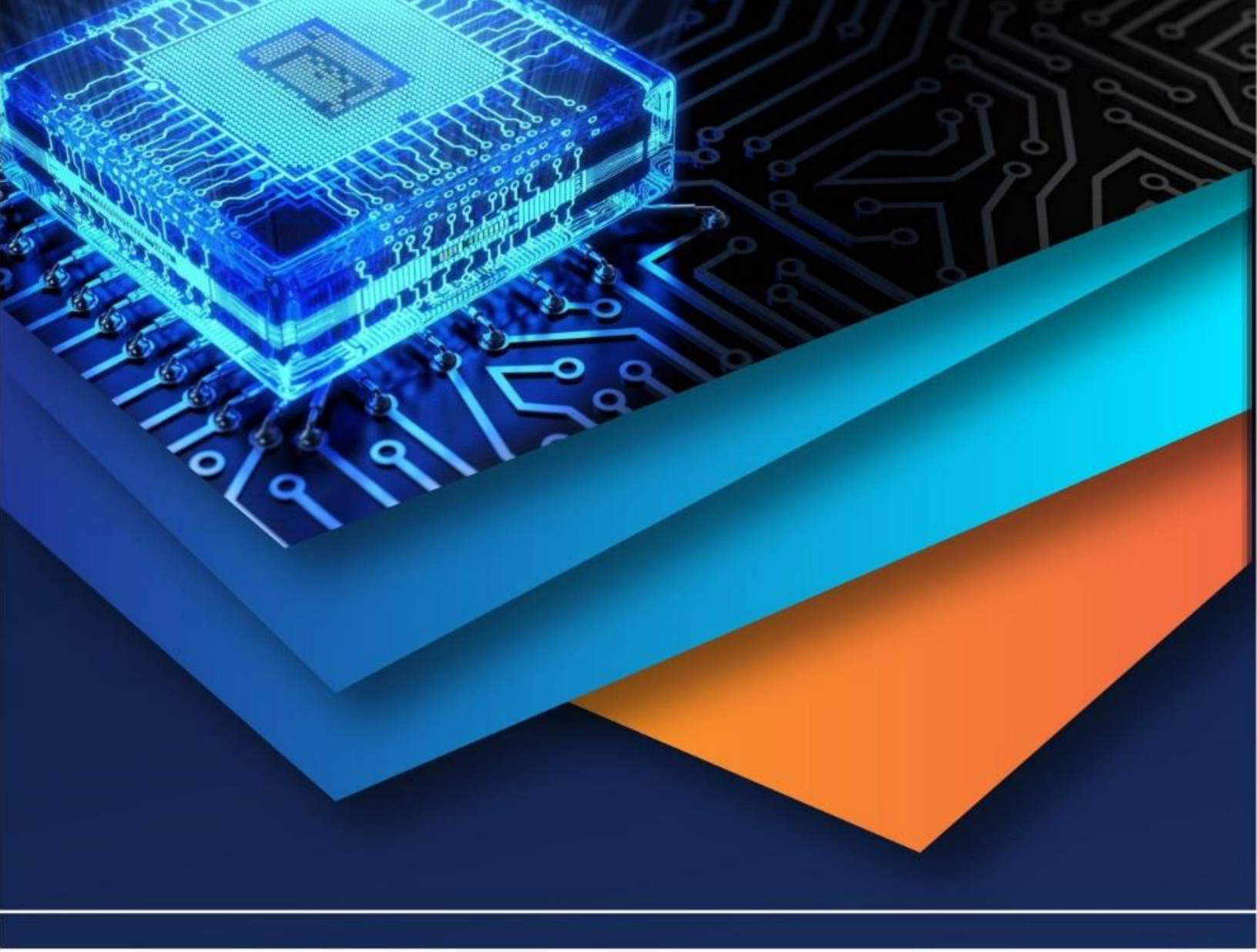

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