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A Novel Dual-Input Asymmetrical 17-Level Inverter

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Abstract: ***Multilevel inverters are the new structures of power electronic circuits that are used in high voltage DC-AC conversion systems. These kinds of inverters create more output voltage levels which reduce the harmonic components. This paper presents a new dual-input asymmetrical single phase multilevel inverter topology capable of producing seventeen level output voltage with reduced number of devices. In order to obtain the desired output voltage, capacitors are connected in all the combination of addition and subtraction through different switches. Inherent creation of the negative voltage levels without any additional circuit, such as H-bridge circuit is one of the main advantage of proposed module. In addition, the module has inherent self-balancing property. Comparison between the existing topologies shows that the proposed topology requires less number of components. Proposed topology is modeled and simulated using MATLAB/Simulink 2017 software in order to verify the feasibility and performance of the module. A phase disposition sinusoidal pulse-width modulation strategy is used in this inverter. The results show that the proposed topology is capable to produce a seventeen-level output voltage with less number of component counts and acceptable harmonic distortion content. A prototype of proposed inverter is designed, analyzed and implemented using Arduino Mega 2560.***

Keywords: Multilevel inverter, asymmetrical, sinusoidal pulse-width modulation, Total Harmonic Distortion (THD), seventeen-level.

I. INTRODUCTION

Multilevel inverters (MLIs) have been innovated as necessary cost benefit devices with a wide range of applications. They have been in the focus for decades because of interesting features such as high quality output voltage, operation in high voltage/power, low harmonic components, low stress on switches, high efficiency, modularity, scalability etc. Multilevel converters have a wide range of applications which has rapidly developed the area of power electronics with good potential for further technology. MLIs with salient features become attractive converters for medium/high power applications in comparison with two levels inverters at the applications of PV farms, wind turbine, active power filer, drives systems and electrical vehicle . Multilevel converters are different arrangements of semiconductor switches with DC links to create n-level output waveform. The concept is to produce higher voltage output in small voltage steps by utilizing more dc sources and switches. As the number of voltage steps increase the output waveform of the inverter approaches near to sinusoidal waveform.

The Cascaded H-bridge (CHB), Neutral Point Clamped (NPC), and Flying Capacitor (FC) are the basic multilevel inverter topologies [1]. In 1981, NPC was introduced as the first multilevel converter which can be used in medium voltage applications. The main disadvantage of NPC topology is that the required number of clamping diodes is quite high and for higher number of voltage levels this topology will be impractical due to this fact. Voltage balancing is another problem of this topology, which can be solved by adding an additional balancing circuit. Early 1990s, FC was presented and in 1996, CHB was reintroduced. Flying Capacitor (FC) topologies require a number of additional floating capacitors in each phase, which are used to generate multi-level outputs from a single DC link. Researchers have a tendency on CHB type due to some drawbacks of NPC and FC including huge capacitors, unbalanced DC links and high stress on switches. Asymmetric multilevel inverters which have unequal DC links become interesting in order to increase the quality of output waveform by minimizing the number of components. Modules are designed based on optimal using of DC links by reduced switches. The papers [2-7] investigated conventional and vanguard topologies for last decade as a reviewing study.

Researchers presented different types of modular multilevel inverters. A cascade multilevel inverter has been presented in [2] which tends to reduce the number of switches. In this topology each level is created by two switches and one source. These levels are connected in series together to achieve positive voltage levels and an auxiliary H-bridge circuit is used to create alternative voltage. Note that, H-bridge switches tolerate more voltages than other switches. This problem has been mitigated in the two other

successive topologies [3, 4]. The symmetric and asymmetric extended cascade multilevel inverter has been presented in [3] which reduces the number of DC voltage sources. Stress of H-bridge switches is divided between each sub-module in [3]. Two capacitors are added for each DC source to reach more voltage levels with the penalty of using more components. Other innovative topology of multilevel converter has been presented in [4], which reduces the number of switches considerably without using high voltage switches. In [5] a packed U cells converter has been presented. Each U cell consists of an arrangement of two power switches and one capacitor. Other MLI topologies are proposed in [6-10]. An E-type asymmetric multilevel inverter is discussed in [6]. In this topology, a combination of ten switches and four unequal DC sources (two $2V_{dc}$, two $1V_{dc}$) are used to produce 13 level output. The aim of the proposed topology is increase the output voltage levels with minimum DC sources, which helps to make the topology more compact.

This paper proposes a new asymmetric multilevel module based on cascade category which offers maximum voltage levels from DC sources. Also, it makes 17 levels by reduced switches. In spite of other topologies, this module does not need any additional circuit to create negative voltage levels. The next section describes the working of the circuit in detail and its comparison with other competitive topologies. The following section gives an idea about the control strategy used in the proposed topology. The performance of the module is verified by simulation and experimental results. Simulation results are recorded, under different load condition, to analyse the performance of the module.

II. NOVEL DUAL-INPUT ASYMMETRICAL 17-LEVEL INVERTER

A. Circuit Description

A novel asymmetric multilevel inverter with smart arrangement of semiconductor devices are shown in Fig. 1. The idea is to arrange the available switches and DC sources in a fashion such that the maximum combination of addition and subtraction of the capacitor voltages can achieve. The proposed topology consists of 12 switches, 12 diodes, 4 capacitors and 2 unequal DC sources. Asymmetrical DC sources are independent of each other and are in ratio of 1:3. These DC voltage sources are equally divided by using 2 capacitors of same value. Using this idea for multilevel inverters (a different ratio of DC sources) generates different number of output voltage levels by fewer DC sources. Surrounding switches (S_1-S_6) are unidirectional switches and middle switches (S_7-S_9) are bidirectional switches. Thus, diodes and bidirectional switches avoid the problem of short circuiting. This arrangement of sources produces 17 levels (8 positive levels, 8 negative levels and zero level). There are symmetric paths for all levels, it makes the output balanced. So the module has self-balancing, inherently. This feature makes easier to control the module.

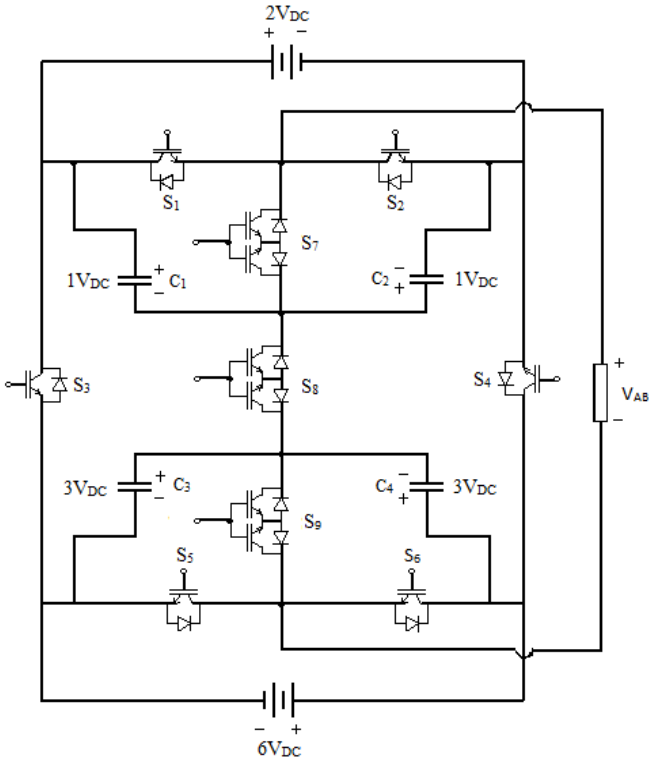

Fig. 1. Dual-input asymmetrical multilevel inverter

B. Modes of Operation

The main concept of this circuit is to create different paths from different sides of a capacitor to be connected to other capacitor to achieve negative levels in order to remove H-bridge. The switching paths does not provide any closed loop for DC sources. Switching states of the switches and the magnitude of the output voltage in per unit for each mode is tabulated in Table I.

TABLE I
SWITCHING TABLE: SWITCHING SEQUENCE AND OUTPUT VOLTAGE

Modes		Switching Sequence									Output Voltage
		S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	
Positive Levels	I	1	0	0	0	0	0	0	1	1	$1V_{dc}$
	II	0	1	0	0	1	0	0	1	0	$2V_{dc}$
	III	0	0	0	0	1	0	1	1	0	$3V_{dc}$
	IV	1	0	0	0	1	0	0	1	0	$4V_{dc}$
	V	1	0	0	1	0	0	0	0	1	$5V_{dc}$
	VI	0	1	0	1	1	0	0	0	0	$6V_{dc}$
	VII	0	0	0	1	1	0	1	0	0	$7V_{dc}$
	VIII	1	0	0	1	1	0	0	0	0	$8V_{dc}$
Zero Level		0	0	0	0	0	0	1	1	1	$0V_{dc}$
Negative Levels	I	0	1	0	0	0	0	0	1	1	$-1V_{dc}$
	II	1	0	0	0	0	1	0	1	0	$-2V_{dc}$
	III	0	0	0	0	0	1	1	1	0	$-3V_{dc}$
	IV	0	1	0	0	0	1	0	1	0	$-4V_{dc}$
	V	0	1	1	0	0	0	0	0	1	$-5V_{dc}$
	VI	1	0	1	0	0	1	0	0	0	$-6V_{dc}$
	VII	0	0	1	0	0	1	1	0	0	$-7V_{dc}$
	VIII	0	1	1	0	0	1	0	0	0	$-8V_{dc}$

Fig. 3 shows different modes of operation in the positive half cycle of the proposed topology. The path followed by the current for different modes are indicated with the red line. For one complete cycle, the circuit will be operated in seventeen different modes i.e. eight for positive half cycle, eight for negative half cycle and one mode for zero level. Modes I(A)-VIII(a), positive cycle modes which produces positive output levels. Negative modes are exactly the mirror images of the positive modes.

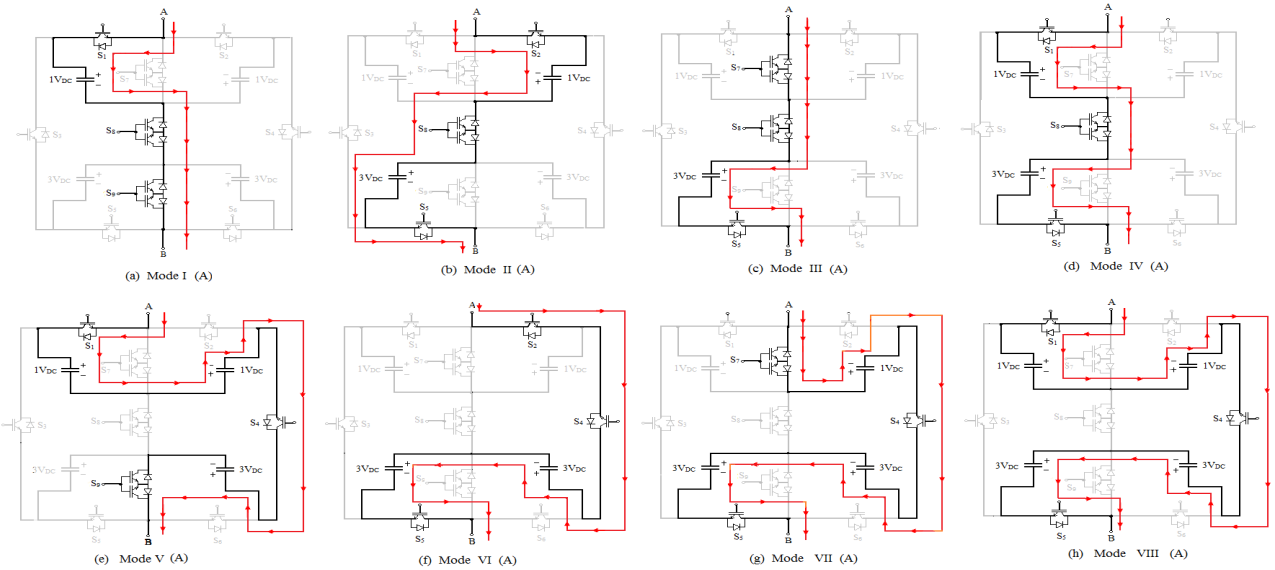

Fig. 2. Different Switching state of the proposed inverter topology during positive half cycle

C. Comparison with Other Topologies

Comparative study, based on the number of switches, diodes, dc sources and total component count, of the proposed topology with other existing topologies for seventeen-level output is carried out and the results are tabulated in Table II. The topologies taken for comparison are cascaded H-bridge (CHB), Neutral Point Capacitor (NPC), Fly-Capacitor (FC) [1], Multilevel DC Links (MLDCL) [2], two capacitor links H-bridge (2CLHB) [3], crossing switch MLI (CSMLI) [4], U-Cell [5].

TABLE III
COMPARATIVE STUDY

	Switch Count	Diode Count	DC Link Count	Negative Level
NPC	32	18	8	With at least Two arms
FC	32	32	15	With at least Two arms
CHB	32	32	8	With H-Bridge
MLDCL [2]	20	20	8	With H-Bridge
2CLHB [3]	18	18	8	With H-Bridge
CSMLI [4]	18	18	8	With H-Bridge
U-Cell [5]	18	18	8	With H-Bridge
Proposed Topology	12	12	2	Inherent

The proposed topology can generate 17 levels with lower components. This ability along with achieving negative voltage levels without any additional circuit confirms that the proposed inverter can perform well in comparison with other existing ones. As the number of device count increases, reliability decreases and the cost, losses as well as complexity in the circuit increases. Therefore, the proposed inverter depicts better performance than other topologies.

III.SIMULATION OF DUAL-INPUT ASYMMETRICAL MULTILEVEL INVERTER

A. Simulation Parameters

To verify the performance of the topology, simulation model based on Fig. 1 is developed in MATLAB/Simulink software. Circuit is simulated at a fundamental frequency of 50Hz. In order to obtain maximum output of 400V, the value of the DC sources is taken as V_1 =100V and V_2=300V. The inverter is operated in open loop mode with 150Ω resistive load.

B. Control Stratergy

Many control techniques are available in literature [9]. Phase disposition sinusoidal pulse width modulation (PS-SPWM) scheme are used to generate gate signals shown in Fig. 3. In this scheme of modulation, gate signals are obtained by comparing sinusoidal reference or modulating signal at fundamental frequency (50Hz) with triangular carrier signal which are at higher frequency. Here switching frequency is selected as 10kHz for better performance. 16 carriers are required to generate 17 level. The magnitude of sine wave is represented as V_{sin} and magnitude of triangular carrier is represented as V_{tir}. The magnitude of carrier is compared with modulating signal to obtain switching pulses.

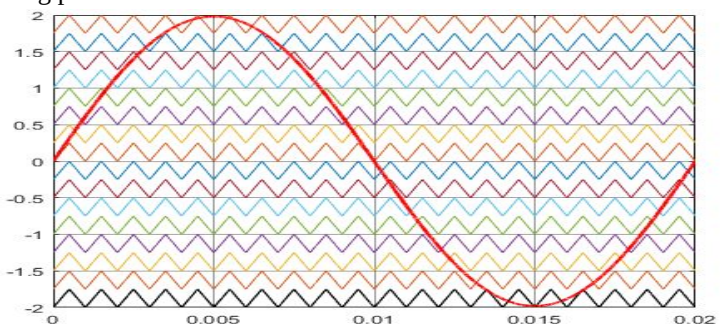

Fig. 4. Phase disposition sinusoidal pulse width modulation

C. Output Voltage and Current

Fig. 5 shows the 17 level output voltage and output current for R-load using PS-SPWM technique. Here, simulation is carried out with 150Ω resistive load. The output voltage for an input of 100V and 300V is 400V.

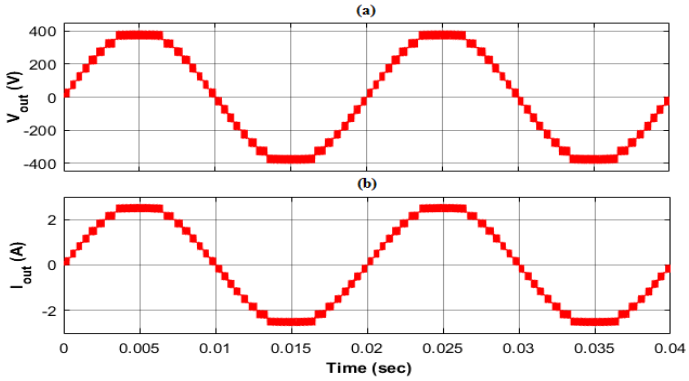

Fig. 5. (a) Output voltage, (b) Output current

Fig. 6 shows the FFT spectrum of output current measured using the FFT block of Simulink. Here %THD is 7.12 by considering 20 cycles of output current with a fundamental frequency of 50Hz.

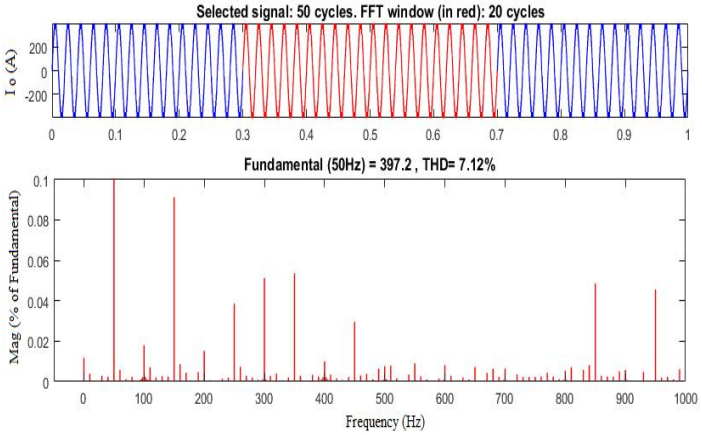

Fig. 6. FFT Analysis

D. R Load

The variation of efficiency and %THD with R-load are shown in Fig. 7 and Fig. 8. The graph clearly shows that variation of R loads up to 250Ω does not significantly affect the efficiency and %THD. The maximum efficiency of the proposed topology is 99%. The %THD is almost constant at 7.02.

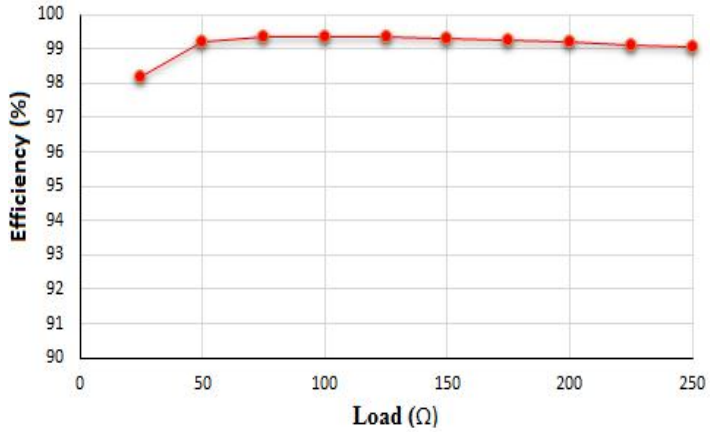

Fig. 7. Efficiency Vs Load

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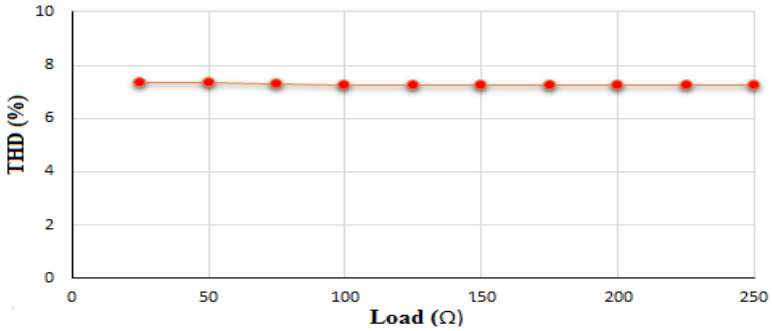

Fig. 8. THD Vs Load

E. RL Load

Fig. 9 shows that the load variation is slightly dependent on the efficiency. The inductance is varying from 100mH to 1000mH and resistance as 150Ω. When the power factor is varying from 0.5 to 1, the %THD maintains a constant value of 7.02 from Fig. 10.

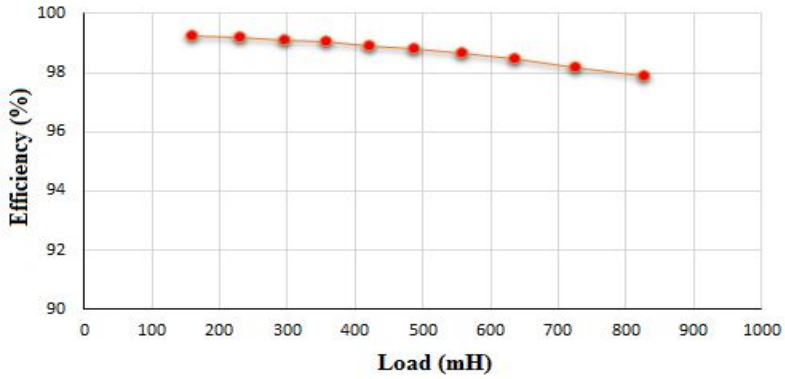

Fig. 9. Efficiency Vs Load

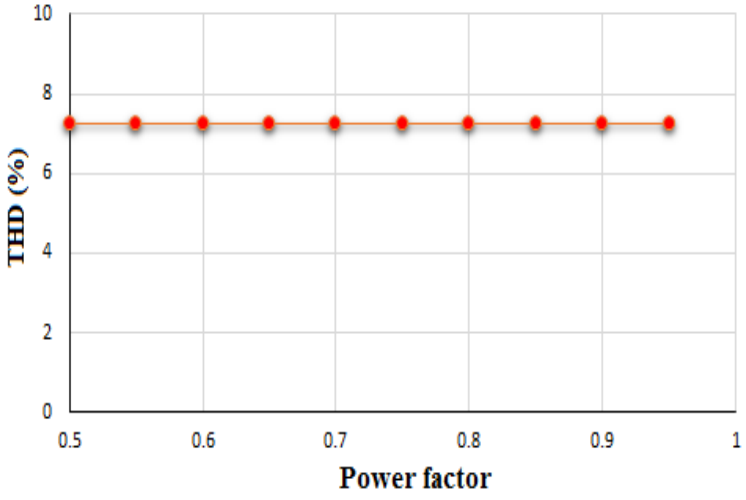

Fig. 10. THD Vs Power factor

IV. HARDWARE IMPLEMENTATION

The implementation of the prototype of dual-switch asymmetrical multilevel inverter requires to two main step, first is the software implementation. Once the programming is done accurately for generating gate switching for switching devices, the hardware implementation of the circuit can be carried out. Software programming is done in Arduino mega 2560 micro controller. The switches used are MOSFET IRF540 along with its driver TLP250 which is an optocoupler used to isolate and protect microcontroller from any damage, and also to provide the required gating to turn on switches.

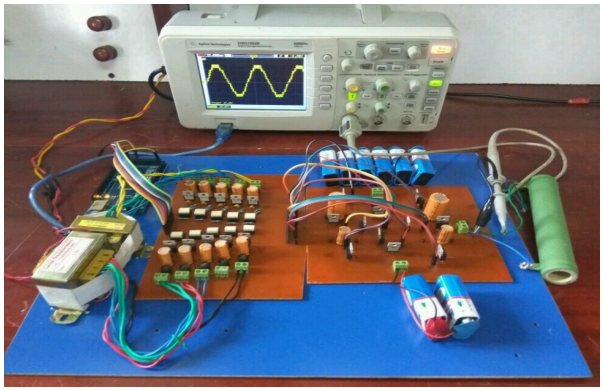

Fig. 11. Hardware setup

For the hardware prototype, 1000µF capacitor and 150Ω, 5W load resistor is used. Since the capacitor charged to half of the supply voltages, output is 50Hz staircase waveform having maximum output voltage of eight times of the supply voltage.

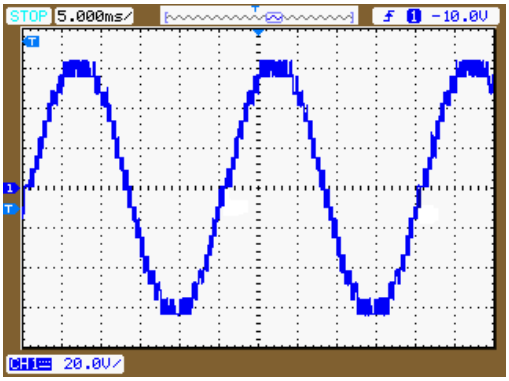

Fig. 12. Seventeen level output voltage

V. CONCLUSIONS

In this work, novel dual-input asymmetrical multilevel inverter is proposed. It can be used in high voltage/power applications with unequal DC sources as input. Proposed topology is capable of producing seventeen-level output voltage with reduce device counts. Different modes of operation are discussed in detail. Comparative study shows that, for seventeen level output, the proposed topology requires lesser component counts than the conventional and other topologies. The performance of the module is verified by simulation and experimental results. Detailed simulation analysis is carried out. From the performance analysis of the inverter, the efficiency of the inverter is found to be 99% and the THD is 7.02%. The variation of THD with different control methods, modulation index, different loads etc. is analysed. Also module is tested under different resistive inductive loads which results good performance. One of the main advantage is that the THD is independent of loads. The prototype of dual-input asymmetrical inverter fabricated in PCB and the control pulses obtained using Arduino Mega 2560. The circuit is tested for an input voltage of 18V, 54V and output voltage waveform is obtained with peak of 62V.

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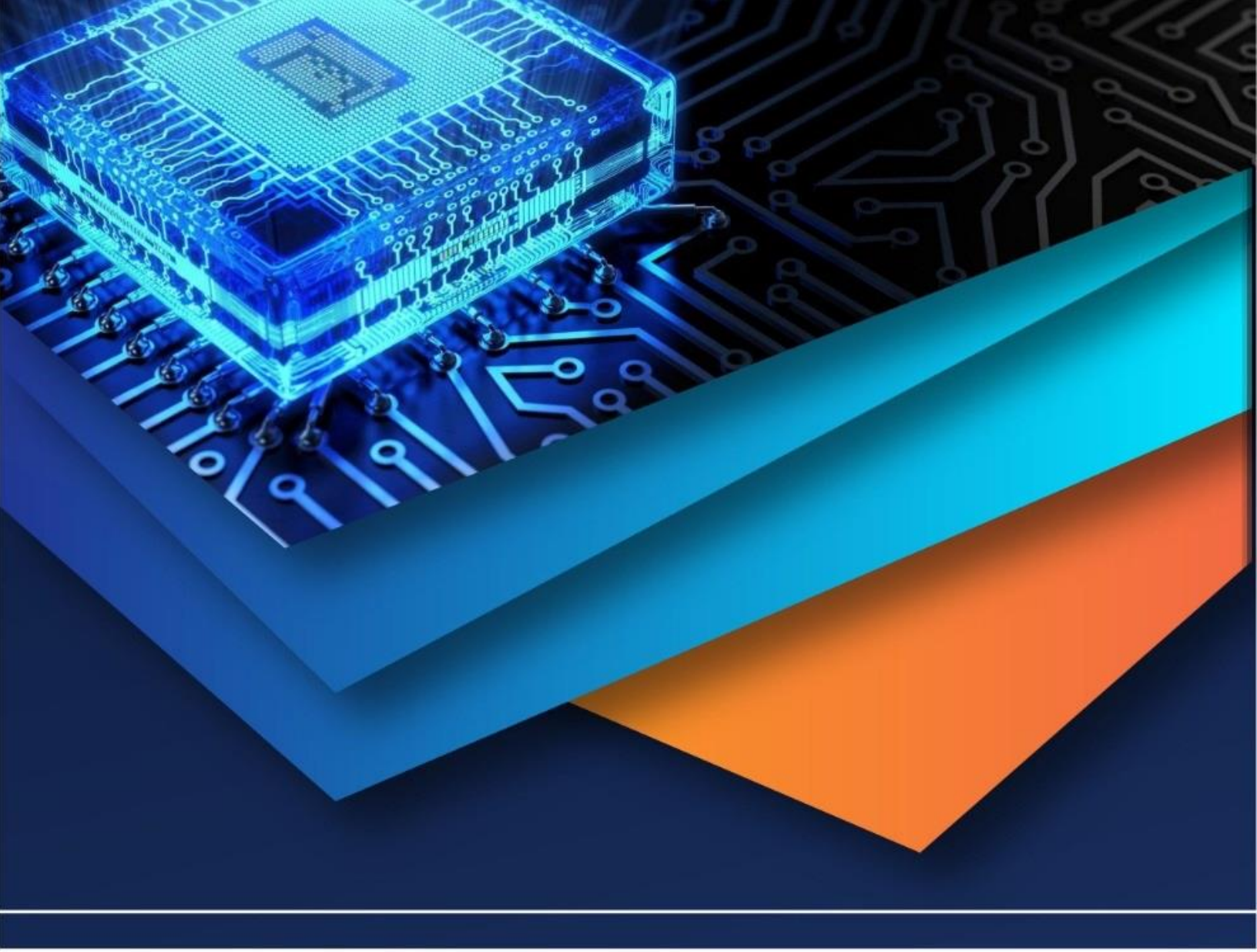

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