iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 6 **Issue:** VI **Month of publication:** June 2018

DOI: http://doi.org/10.22214/ijraset.2018.6246

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International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 6.887
Volume 6 Issue VI, June 2018- Available at www.ijraset.com

A Review on Design and Analysis of Low Power PLL for Digital Applications

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Abstract: This paper discusses the challenges and outcomes in designing the low power PLL for digital applications. PLL being an important block for providing clocking scheme in many electronic circuits raises the requirement of decreasing the power with the growing CMOS technology. The state of art designs adopted is critically reviewed and improvements are suggested.
Keywords: PLL, CMOS, Clocking, Power, Digital Applications

I. INTRODUCTION

The PLL is the predominant and constructing a part of Digital electronics, communication (wireless and wire-line) and excessive-speed (Low propagation delay) digital methods. A PLL designed by means of built-in CMOS has executed the fine importance within the last few many years considering the fact that of the high performance system design within the digital and communication area. It is in actual fact utilized in many methods for frequency synthesis, clock/data restoration, clock de-skewing, and many others. For an IC, the important element to be regarded for its designing is its low power consumption (because of smaller chip dimension) and increased operating speed. Right here enhancement of speed isn't the major obstacle; here the focus is more commonly on reduction of power consumption via PLL as a lot as viable. There are basic components present inside PLL whose circuitry might be modified to obtain the desired outcomes, without effecting different fundamental phenomenon.

II. PAGE LAYOUT

The rest of the paper is organized as follows. A brief description of the PLL is described in section III. Section IV contains the architecture adopted so far for low power PLL design. And conclusions are drawn in section V.

III.GENERAL DESCRIPTION OF PLL

PLL can be seen as a circuit which synchronizes an output signal (generated by an oscillator) with a reference or provided input signal in phase as well as frequency [1].

In the synchronizing state, which is also referred to as “the locked state”, the phase error which occurs between the output signal and the input or reference signal remains either constant or is zero However, if in the process due to some discrepancy a phase error have some value rather than zero or constant, a control mechanism gets triggered, which acts upon oscillator to counter-balance the obtained resulted phase error in such a way that it will reduced to minimum until it will matched. As, the control system locks (matches) the phase of the output signal to the phase of the reference signal. Hence it is named, “Phase-locked loop”.

The important feature to note here is that, the PLL not only responsible to set a fixed relationship between its output clock phase and the input or reference clock phase but it also keep track on the subsequent phase that changes within its bandwidth.

Due to its characteristics features, the PLL has been used for communication network systems and other circuits which require a data synchronization, clock recovery and frequency multiplier.

It ensures the system and circuit engineers with a high extent of freedom to generate well-timed on-chip clocks in great performance digital systems. PLL constitute of PFD (Phase Frequency Detector), Charge pump, Loop filter and VCO (Voltage Control Oscillator), these are the basic building blocks of the PLL.

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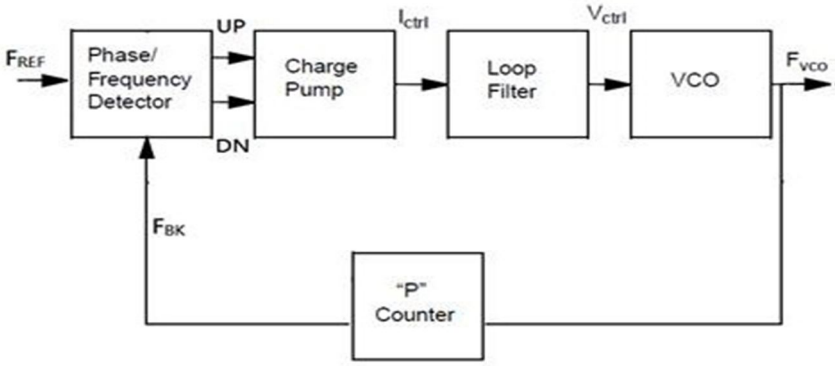

Fig. 1 Basic Building Block diagram of PLL

A. PFD (Phase Frequency Detector)

It is basically used to compare the phase of feedback signal from VCO with the phase of input or reference signal and generate outputs (UP or DOWN) as per the Phase difference also known as phase error. UP signal will be HIGH, when phase of input or reference signal leads towards VCO output signal else DOWN signal will be HIGH.

B. Charge pump (CP)

It mainly used for conversion of the digital output of PFD into the current signal, such that a stable controllable signal has been generated for oscillator to control the oscillation frequency. Charge pump stores the charge in the capacitor of Loop Filter and charges or discharges the capacitor of the Low pass filter as per the provided UP or DOWN signal of the PFD..

C. Loop Filter

The loop filter is the heart of PLL. It is very important to choose the loop filter values appropriately, as any random values may either lead to the long oscillation of loop without reaching the locked state or it may happen that for once it is locked, but for small variations in the input data may cause the loop to unlock. It is used to stabilize the system and achieve the desired response.

D. VCO

The voltage controlled oscillators is the very important device component of this feedback system that helps to produce the essential frequency output (Fref) in the PLL. Depending upon control voltage of the low pass filter, the VCO generates a reference signal that matches the frequency. An oscillator is an independent system which gives a periodic output without any input signal. A voltage controlled oscillator is an electronic oscillator designed such that its input voltage controls its oscillation frequency, in PLL it increases or decreases output frequency as per the control voltage produced by the charge pump. The basic block diagram of the PLL is shown in the Fig. 1.

IV. ARCHITECTURE ADOPTED FOR LOW POWER PLL DESIGN

Zafer Ozgiir Gursoy et.al (2003) have given paper in which it is designed, verified, system integrated and physically realized a high-speed monolithic phase locked loop (PLL) based high performance clock and data recovery (CDR) circuit(as shown in Fig. 2) using conventional 0.13-pm digital CMOS Technology which operates up to 3.2 GHz of sampling frequency and can achieve the robust phase alignment with overall power consumption of 18.6mW having silicon area of the CDR is approximately 0.3 mm2 with its internal loop filter capacitors. [1].

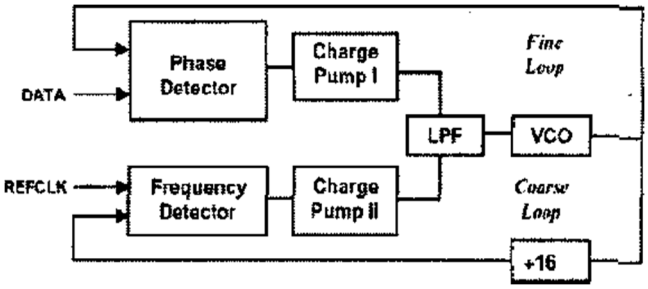

Fig.2 Architecture proposed by Z.O. Gursoy et.al of two loop CDR block

Ashish mishra et.al (2014) has analyzed that by using 5-stage CSVCO(Current starved VCO) as shown in Fig. 3, lock range from 357MHz-900MHz has increased with large VCO gain, lock time has reduced and got improved around (54ns) with oscillation frequency range 431.683 MHz-1.7966 GHz because of more number of inverter stages with PLL power dissipation of 7.08mW. Also the phase noise performance for the 5-stage VCO has improved. [2]

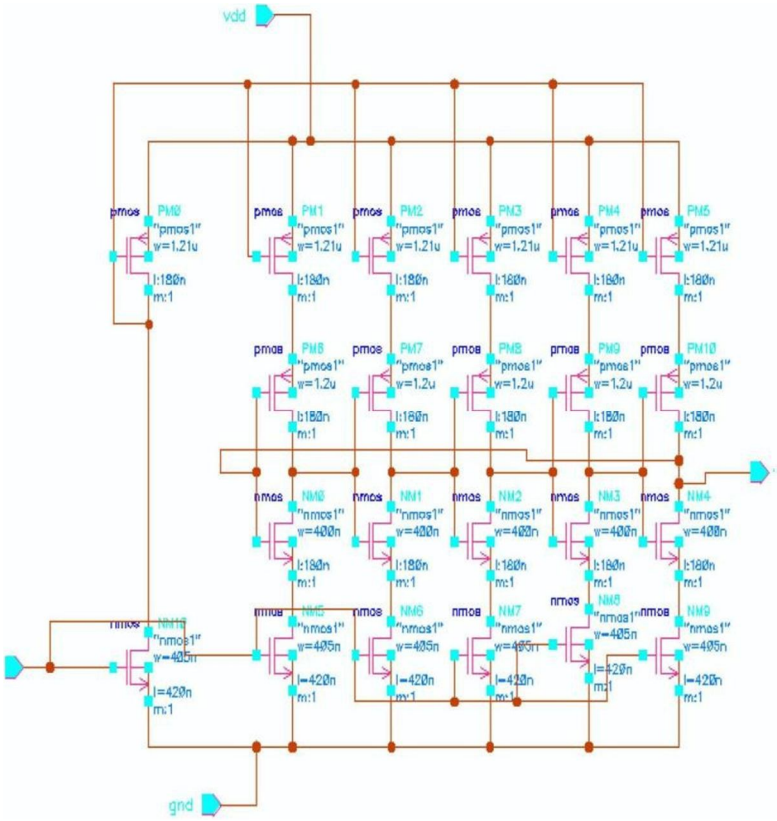

Fig. 3 Architecture proposed by Ashish Mishra et.al of 5 stage CS-VCO

S. Moorthi et.al (2013) has focused to design a 1GHz range PLL with low power consumption and low jitter. A telescopic OTA based ICO (current controlled oscillator) is designed as shown in Fig. 4 to make the PLL operate at high frequency and improve the lock-in range. The problems of current mismatch between the charging and discharging current, charge sharing and jitter due to the delay have minimized and a conventional charge pump has designed. Due to this jitter performance has reduced and passive loop filters and a D-latch based PFD have used to minimize the overall power consumption and to enhance the system stability. The major power consuming block in the proposed system was VCO. The system is simulated in CADENCE UMC180nm technology and the results obtained showed maximum jitter is 27.1ps and that the lock-in range is 1GHz with 0.34mW power consumption. [3]

Jussi Ryynanen et.al (2009) Has presented a 2.4-GHz all-digital phase locked loop (ADPLL) frequency synthesizer for wireless applications. Around a digitally controlled LC oscillator The ADPLL has been built, and with fine frequency resolution it covers the target frequency range. A high-speed topology has employed in the feedback path for the variable phase accumulator to count full cycles of the RF output. A short delay line based on a simple technique in the reference signal path effectively reduces power consumption of the time-to-digital converter (TDC) and lowers in-band spurs of the output spectrum. It has been fabricated in a 65-nm CMOS. The ADPLL has provided an active area of about 0.24 mm2. Output frequency range is from 2.29 to 2.92 GHz has measured. The worst case phase noise is -120dBc at the frequency range 1MHz, when power is lowered to 8mW, the PLL consumed 12mW from a 1.2-V supply. The far-off spurs below -57dBc and inband spurs are below - 61dBc. [4]

Chung-Ting Lu et.al (2010) has given a circuit topology of the quadrature voltage-controlled oscillator (QVCO) has presented in this paper for low-power and low-voltage applications. Quadrature output phases can be generated at minimum power consumption, with the antiphase coupling provided by the MOSFETs in a passive mode, while maintaining desirable circuit performance in terms of phase noise and phase error. An integer-N phase-locked loop (PLL) is implemented in a standard 0.18- m CMOS process Based on the proposed QVCO circuit (as shown in Fig. 5). As the building blocks are optimized for low-power and low-voltage operations,

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Volume 6 Issue VI, June 2018- Available at www.ijraset.com

the fabricated PLL has frequency range of 2.4-GHz consumes a dc power of 14.4mW from a 0.6-V supply. By applying a reference frequency of 20 MHz, the phase noise and measured spur rejection at 1-MHz offset are 104.69dBc/Hz and 39.83 dB, respectively has produced quadrature output waveforms, the phase error is 2.21. [5]

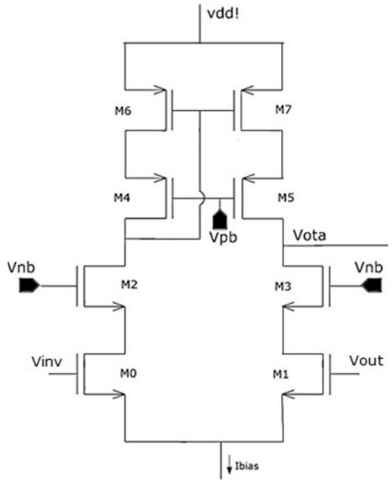

Fig. 4 Architecture proposed by S.Moorthy et.al of telescopic OTA

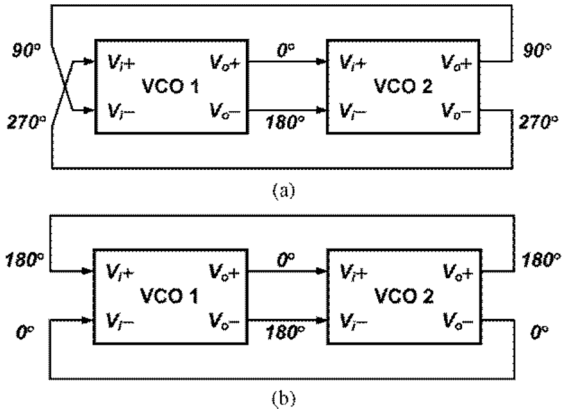

Fig. 5 Architecture proposed by chung-ting lu et.al. Fig (a)Antiphase (b)inphase coupling structures

Jogi ganesh et.al (2016) have proposed ADPLL in which functionality of the design has confirmed by utilizing Incisive Unified Simulator .The performance issues like area, timing analysis and power consumption are analyzed at a typical libraries of TSMC 45nm technology by using Verilog-HDL and by using Encounter RTL Compiler the designs are exclusively synthesized. A low power All Digital phase locked loop (ADPLL) yield better testability, programmability, stability and portability over different processes also it has better noise immunity. It has wide applications in signal processing and communication systems like SerDes. The lock range is less than 11 cycles and total power dissipation is 1127nW. [6] Anshul agrawal et.al (2015) has performed and designed the PLL in which PFD has designed in such a way that the PLL became free in dead zone, VCO is giving larger tuning range (167MHz- 1.711GHz), high gain 2.21GHz/V or 13.875*109radians/s*V, pull-in range 950MHz(50MHz – 1GHz) with max jitter 9.8ps with pull-in time is 265ns at 1GHz. power consumption has reduced to 277.2µW. here also, 180nm CMOS technology have used with suppl of 1.8V and simulated by using CADENCE spectre simulator. [7] Abdul Majeed K.K. et.al (2013) have presented two phase frequency detectors PFD1 and PFD2 have designed by using 15 and 8 transistors respectively with a supply voltage 1.8V. In this work power consumption has reduced by 80.3% and 99.2%, area reduced up to 64.9% and 81.4% as comparison with conventional PFDs, phase noise has reduced to -161.8dBc/Hz and - 142.1dBc/Hz for PFD1 and PFD2 respectively, also frequency range has enhanced 3-5times higher as compared to conventional PFD. To speed up acquisition process and to eliminate blind zone the reset process has removed completely, by implementation of 180nm technology using GPDK090 library in CADENCE virtuoso environment. [8].

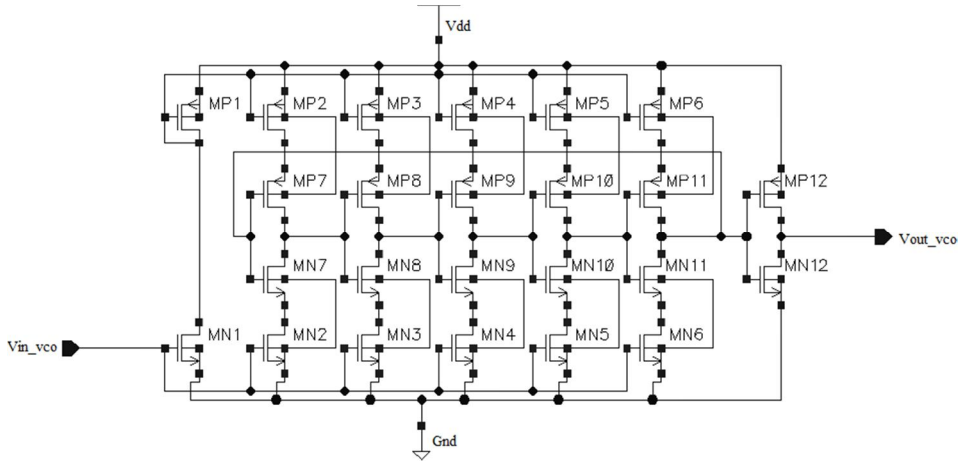

Fig. 6 Architecture proposed by anshul agrawal et.al CS-VCO

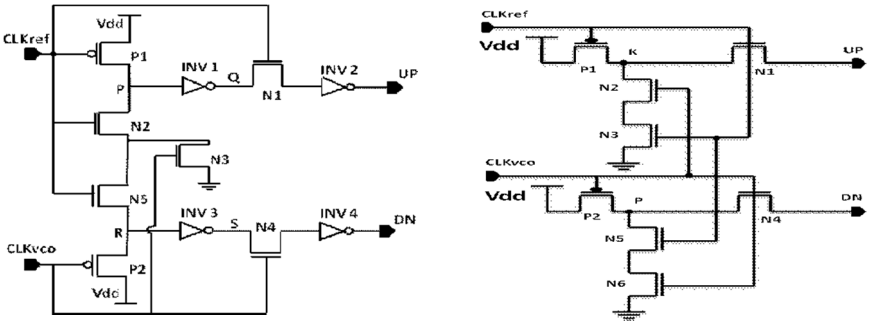

Fig. 7 Architecture proposed by Abdul Majeed K.K et.al of PFD1 and PFD2

Sreedhar Vineel R. Kaipu et.al (2016) have designed third order, fully integrated low power phase-locked loop (PLL) with a wide range of 1.7GHz to 2.5GHz using UMC 180nm CMOS technology. In this paper they have designed integer-N PLL based on frequency synthesizer with some modifications in VCO. This resulted into the jitter of around 35.26ps which has settled down at frequency of 2GHz at 14.1µs. the overall power consumed here is 274.34µW at 1.4/1.8V. the design has taken an area of0.11862mm2 which could be used for Zigbee applications. [9]

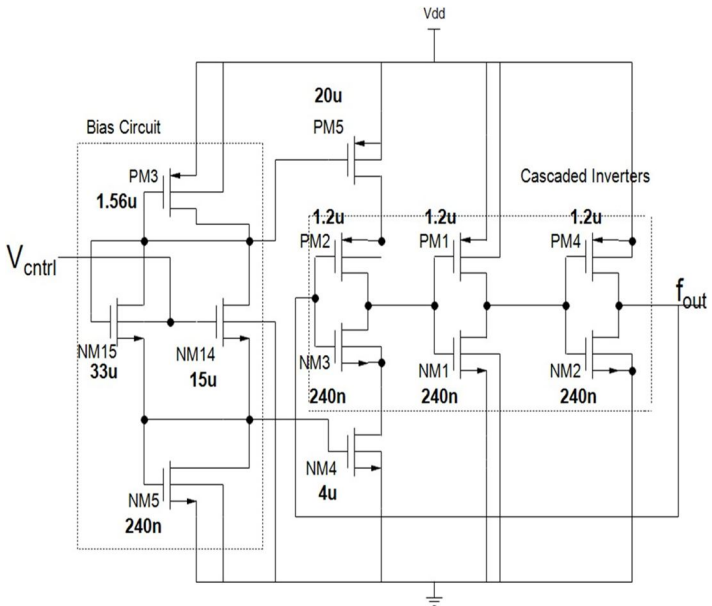

Fig. 8 Architecture proposed by S.V.R Kaipu et.al of VCO along with transistor widths

Kanika Garg et.al (2013) have presented third order PLL by focusing on reduction of power consumption to get wide applications on low power. They have tried to reduce power consumption to 37% with minimum 12mW and maximum 31mW with RMS value equals to 1.7V and average value 1.3V with power supply of 3V at 350nm technology node by using SPICE model. The proposed design has been similar to conventional PLL but instead of VCO, a fully differential ring oscillator based VCO has taken. Also, second order passive loop filter, 7-bit digital frequency divider using 350nm, 180nm and 130nm technology nodes at 350MHz have used [10] Swati Kasht et.al (2012) designed and simulated low power PLL and fast locking using 180nm CMOS technology of TANNER tool and National Clock Design tool has used to analyze jitter and phase noise. To achieve these specific properties of PLL few modifications has been done into its internal components as they have designed PFD using edge triggered D flip flop for reduction of static phase error and area, charge pump of current mirrored structure to decrease the current mismatch with enhanced output voltage and self bias differential ring oscillator VCO to obtain low jitter. Hence the paper presented its result with less locking time of 554ns, with consumed power as 0.38mW, phase noise of -98.14dBc/Hz at 100kHz and having RMS jitter of 159.5ps [11]

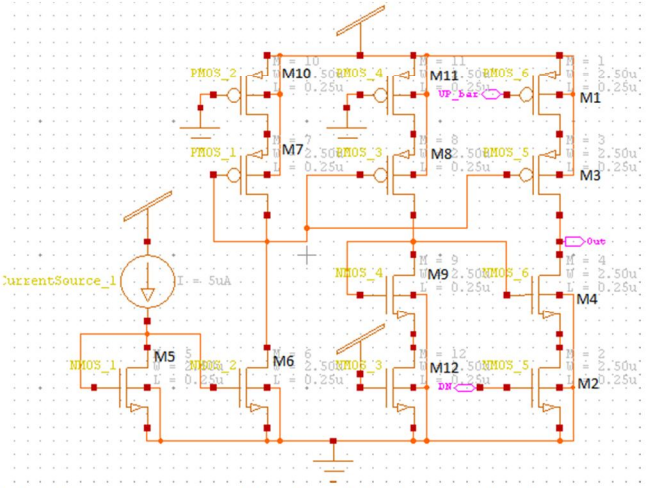

Fig. 9 Architecture proposed by Swati Kasht et.al for charge pump

K. N. Minhad et.al (2014) proposed work has focused on power supply, power consumption, layout area, dead zone size and wide input frequency range while considering mainly on characteristics of PFD, it should be preserved by using 18 transistors operated at 1.2V supply. It has been designed by using Mentor Graphics environment and 180nm CMOS process. The active layout area comprised is 101µm2, total power consumption is 59pW when input frequency clock operates at 50MHz while feedback input frequency clock operated at 4GHz and peak-to-peak spikes has lowered to 76mV. [12]

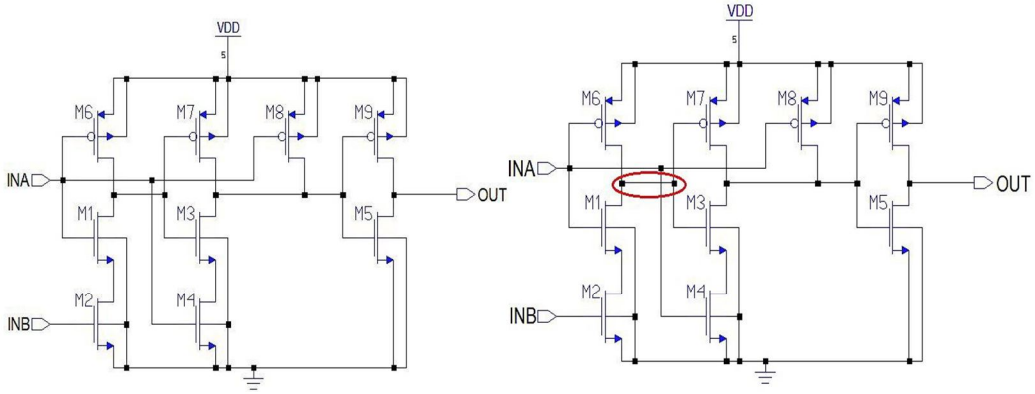

Fig. 10 Architecture proposed by K.N Minhad et.al

Kruti P. Thakore et.al (2011) presented three types of PFDs- traditional, modified and high speed, on comparing these with each other in respect of low power and low jitter it has detected that high speed PFD has achieved it. High speed PFD has operated at input frequency of 1GHz with 1.8V supply voltage, total power consumed is 0.39nW and resulted only 2ps of jitter. It has been

simulated with 350nm CMOS technology [13]

Jeng-Han Tsai et.al (2015) Designed and fabricated an X-band 9.75/10.6GHz fully-integrated low power PLL on 180nm CMOS process. Nearly 24mW power has consumed, with output frequency of 9.75GHz and 10.6GHz which has successfully synthesized with a reference source of 12.5MHz, through band control circuit of VCO and modulus frequency divider. At an offset frequency of 10MHz the closed loop phase noise of PLL measured is –116.24dBc/Hz and -122.64dBc/Hz with center at 9.75GHz and 10.6GHz respectively. The PLL having low power consumption, better phase noise and high level integration which has been suitable for X-band and found many applications in low noise block(LNB) converter of satellite television [14]

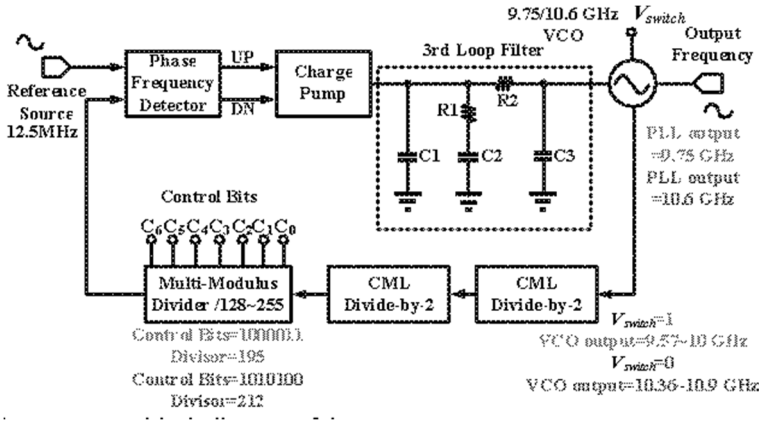

Fig. 21 Architecture proposed by Jeng-Han Tsai et.al.

Shao-Wei Huang et.al (2014) designed and integrated a 5.5GHz full integrated low power PLL on standard 180nm CMOS process. Here 9.23mW power consumption has achieved by the utilization of transformer feedback VCO and high speed true single phase clock (TSPC) divider. Also, to give full voltage swing for TSPC input a rail-to-rail buffer amplifier is incorporated between the VCO and TSPC divider chain. The phase noise measured at 1MHz and 10MHz of offsets frequency are -85dBc/Hz and -116.6dBc/Hz respectively. [15].

V. CONCLUSIONS

The low power PLL design circuits discussed in this paper mainly describes the modification on design of VCO and PFD. However since loop filter plays major role in PLL design, the charging and discharging of loop filter's capacitor must be controlled in a way so that power dissipation can be further reduced. Future work will be based on modification of loop filter design for power reduction

VI. ACKNOWLEDGMENT

The authors would like to thank all the researchers who have already contributed in this field of PLL for low power consumption, their work and experiments will be beneficial and also they have provided us a leading way for our future implementations. The authors hope this acknowledgment of some contributors will let readers know that the field they are working in or are about to venture is one of the most demanding field around the globe. Individuals, too numerous to mention, have also played a role in contributing towards this article. The authors would like to take this opportunity to also thank them for their contributionsAlso a very special thanks to our college committee for motivating us and for providing us a golden opportunity to work on this area.

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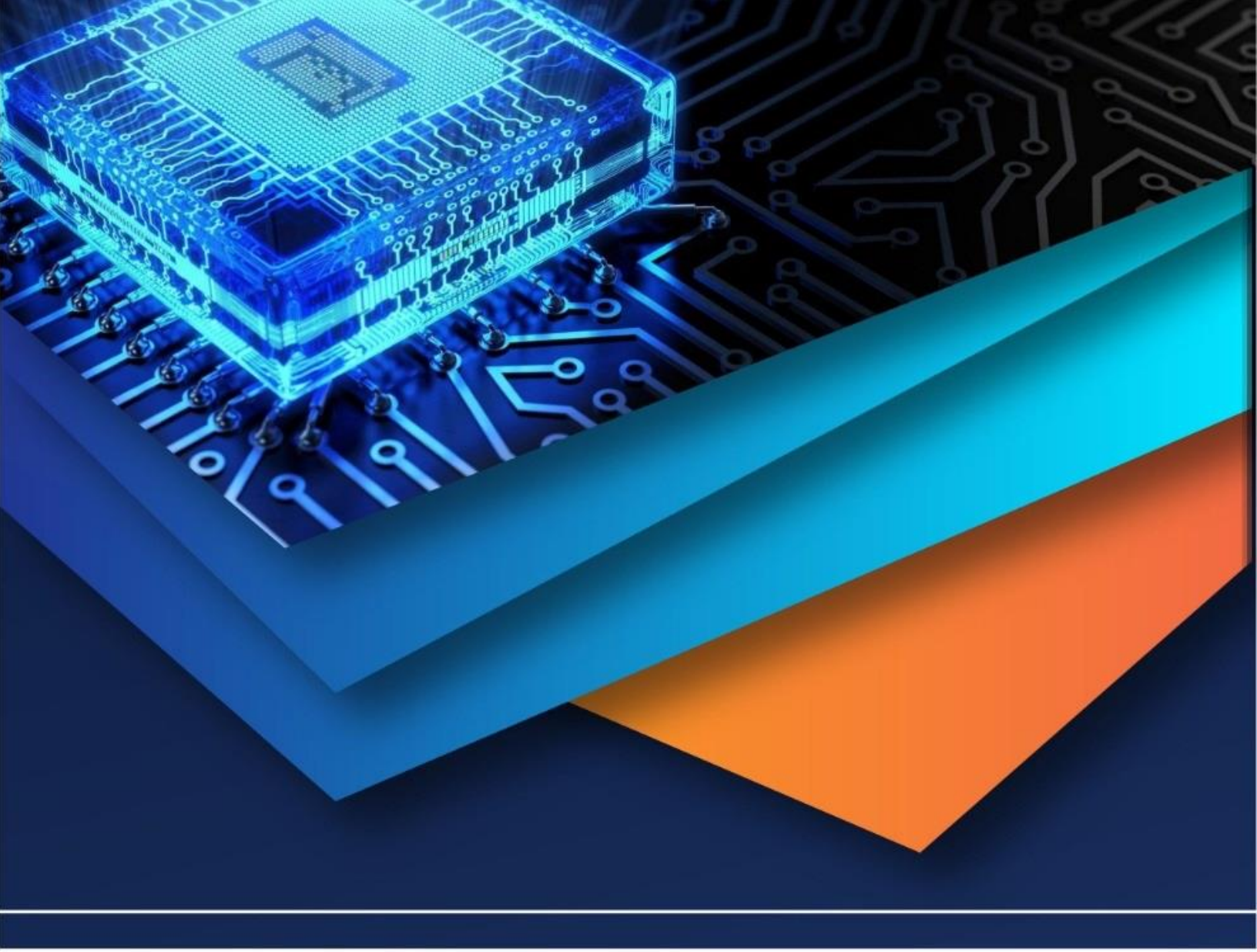

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