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Generation of Pulse Width Modulation for Controlling BLDC Motor Implementation using FPGA

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Abstract: ***Pulse width modulation (PWM) has been widely used in speed control of BLDC motor drive application. Pulse Width Modulation (PWM) signal is applied to the gate terminal of the power electronic switches IGBT, MOSFET and etc., in the electric drives to control the average voltage delivered to the motor which control the speed of the motor. This PWM pulses generated using Field Programmable Gate Array Xilinx Spartan -3board simulation is done using isim software .output waveforms are obtained and validated with register transfer level (RTL) schematic.***
Keywords: PWM, VHDL, Register Transfer Level (RTL), Field Programmable Gate Array (FPGA).

I. INTRODUCTION

In the recent years, the Pulse width modulation (PWM) techniques are most popularly used to controlling the electric drives application. PWM Signal is used to triggering the power electronics switches In power converters it is used for firing of power electronic devices like Metal Oxide Semiconductor Field Effect Transistors (MOSFET), , Insulated Gate Bipolar Transistors (IGBTS) and etc.[1]-[3]. Recently the concept of digital signal processing (DSP) used in the electrical drives applications that make a cost effective and energy efficient control system design. The performance of DSP architecture allows an intelligent approach to reduce the complete system cost. Although these devices are indeed very powerful, they do not have the total flexibility of programmable logic devices (PLDs). Most preferred PLD technology is represented by field programmable gate arrays (FPGAs), which offers the possibility of defining efficient custom hardware and powerful processing capabilities due to the inherent parallelism in FPGA architecture. They can perform complex computations faster than DSPs[4].Sixstep Inverter fed three phase Brushless DC motor drives has wide area of domestic/industrial application which has the smooth operation ,longlife, good weight to torque ratio, high effiency. The Pulse Width Modulation (PWM) makes that convert three phase fixed DC volage DC voltage by controlling the duty cycle of the PWM pulses. Duty cycle (D) means that, as ratio of ON time (Ton) over to total Time period(TP) .

Duty cycle $D = Ton/TP$ (1

The two decade before, PWM signal are generated using the analogy circuit which has many drawbacks like less flexibility , more complexity, to overcome the above issues, pwm signals are generated using digital circuits [6]-[7].In the paper proposes the generation a PWM signal for control the BLDC Motor drive using Hardware Description Language. Xilinx FPGA Spartan 3 A board and Integrated system Environment (ISE) is used

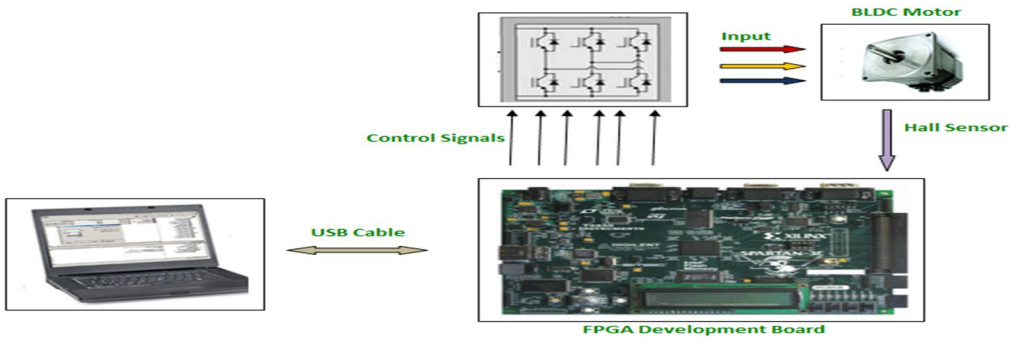


Fig 1. Block diagram for BLDC Motor Drive

II. STRATEGY FOR GENERATING PWM SIGNALS IN FPGA USING VHDL

The Counter based PWM generator has N bit digital input which will desired PWM duty cycle value. The N-bit comparator compares the N bit counter output and N bit register output When both input of the comparator become equal, the output of the comparator is reset the RS latch . When the input of the comparator is not equal, the output of comparator is set the R/S latch output which produces the PWM signal. Next PWM signal is generated when the counter overflows [8] Each PWM signal is generated using one counter. For generation of six PWM pulse, total number of six counter is required. A clock and a reset is taken common for all counters.For an N-bit resolution, provides a 2^N values of different duty cycle , the clock frequency, f_{clock}, is correlated to the PWM signal frequency, f_{PWM}, as follows:

$$fPWM = fclock/ 2N$$

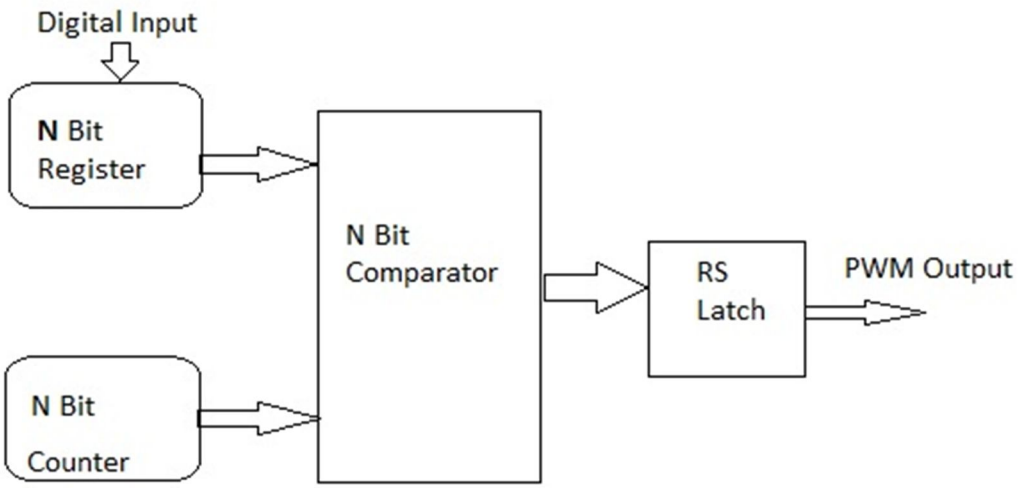


Fig 2. Counter based PWM Generator

III. IMPLEMENTATION OF VHDL CODES IN XILINX

the codes are written in Xilinx ISE then code is synthesized by using synthesizer and then can get Pulse Width Modulation output waveforms on Xilinx iSim simulator as well as the RTL schematic is generated (Fig.3) which provides a whole information about the function of our proposed PWM generator

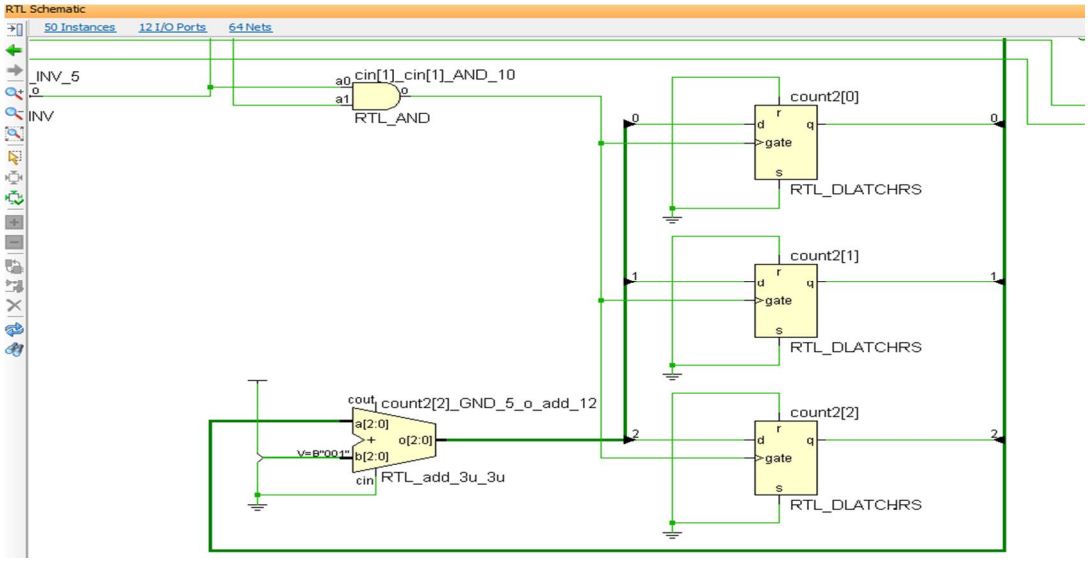


Fig 3. RTL schematic of proposed PWM generator

A VHDL language was used to develop a software program and program was synthesized by using Xilinx ISE 14.5. Behavioural simulation is verified using Xilinx isim simulator as shown in Fig 3. If clock speed is increased the PWM resolution is reduced, reduction of delay depends on the counter internal logic. Observation of the output show that PWM frequencies up to 3.985 MHz can be produced using the proposed design techniques which is adequate for a motor control, renewable energy systems control, etc.

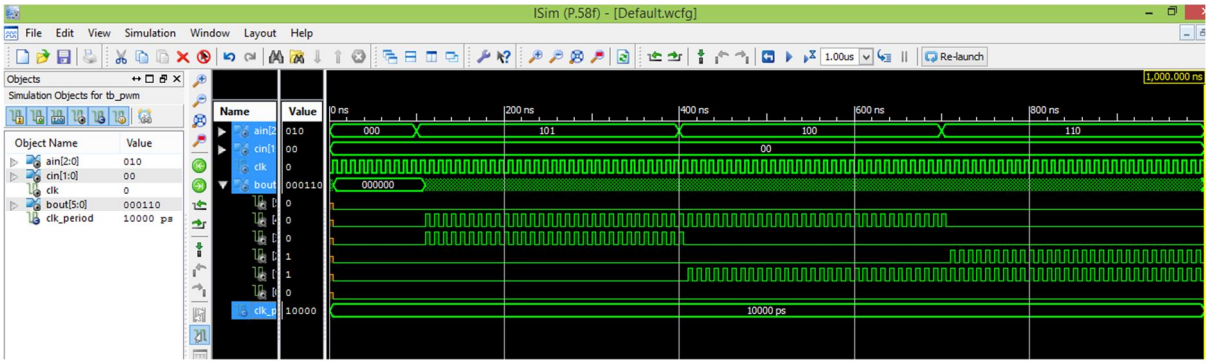


Fig 4.PWM waveform generation using FPGAThe FPGA Xilinx Spartan 3E xcs500 board reads from the Hall Effect sensor which is placed the BLDC Motor. Electronic commutation is required in order to motor rotates. Based on the commutation sequence the FPGA board generate a Pulse Width Modulation (PWM) and commutation signal shown in Fig.4. Synthesis report shows that less number of FPGA resources (Fig 5.) are needed to implement for the proposed PWM generator. In this study FPGA Spartan 3E board is used and specification follows

Device	-XC3S100e
Purpose	-General Purpose
Package	- tq144
Speed grade	-4

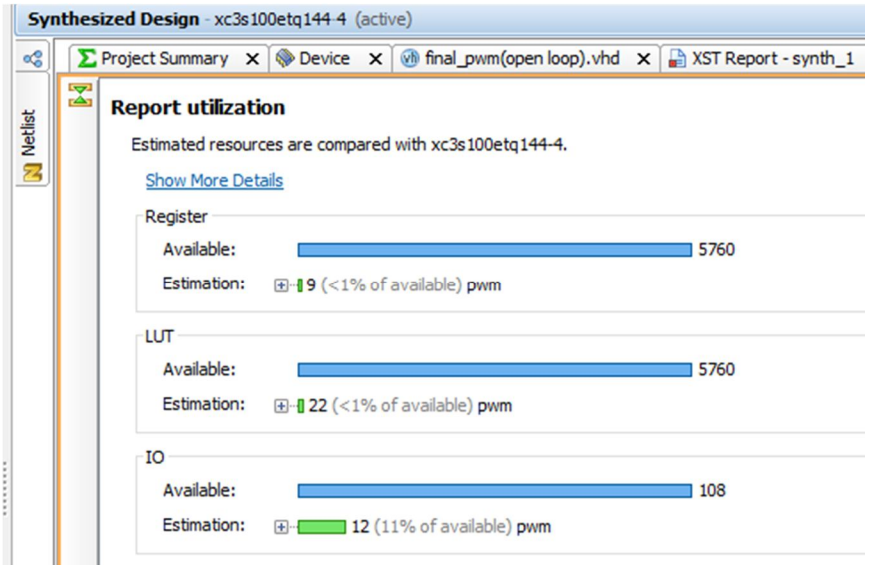


Fig. 5.Synthesis result of generation of PWM for area utilization

IV. CONCLUSION

In this paper the generation of Pulse Width Modulation signal for controlling the speed of the three phases BLDC Motor using Hardware Description Language is investigated. A code is written for the PWM generation of fixed frequency in the VHDL which is implemented on FPGA and validates by using RTL schematic. FPGA are faster, flexible and suitable than traditional DSPs. The simulation results validated that an efficient PWM generator was developed

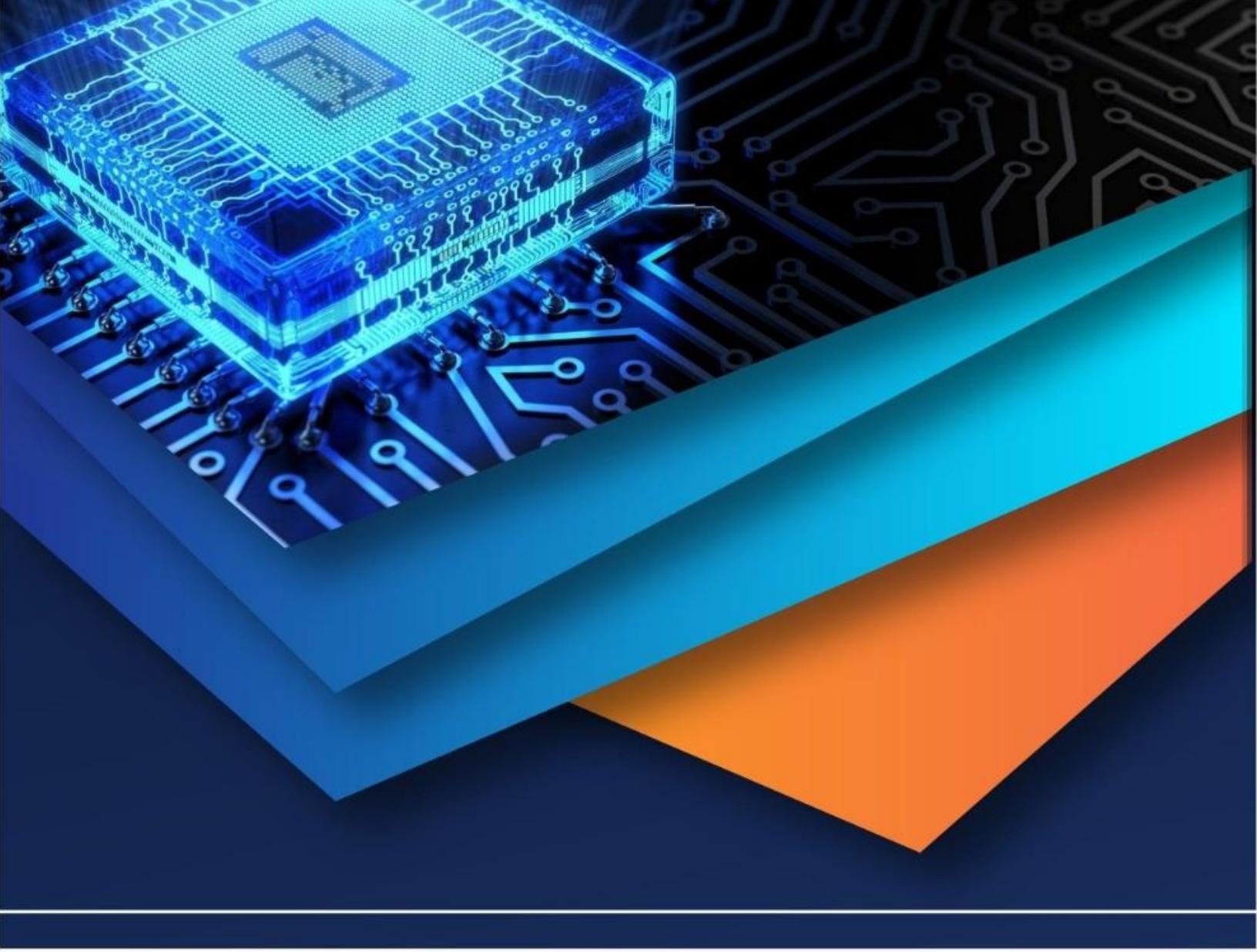
REFERENCES

[1] R.Krishnan, "Electric Motor Drives Modeling, Analysis, and Control, Prentice-Hall International Inc.,New Jersey, 2001
[2] S.Raja, Dr. M.Rathinakumar, A. S. Viswanathan, Performance Analysis of Digital Controller for BLDC Motor Drive System, International Journal of Innovative Research in Science, Engineering and Technology, Vol. 6, Issue 6, June 201
[3] Jakirhusen I. Tamboli, Prof. Satyawan R. Jagtap, Amol R. Sutar Pulse Width Modulation Implementation using FPGA and CPLD ICs, International Journal of Scientific & Engineering Research Volume 3, Issue 8, August-2012 1 ISSN 2229-551
[4] R.M. Jalanekar & K.S. Jog, "Pulse –Width-Modulation Techniques: A Review," IETE journal of research, Vol. 46, No. 3, May-June 2000.
[5] Brian von Herzen, "Signal processing at 250 MHz using high performance FPGA s," IEEE Transactions on VLSI Systems 6, 1998, pp. 238–246.
[6] M.M. Islam, D. Allee, S. Konasani, A. Rodriguez, "A low-cost digital controller for a switching DC converter with improved voltage regulation," IEEE Power Electronics Letters 2, 2004, pp. 121–124.
[7] R. Ramos, D. Biel, E. Fossas, F. Guinjoan, "A fixed-frequency quasisliding control algorithm: application to power inverters design by means of FPGA implementation," IEEE Transactions on Power Electronics 18, 2003, pp. 344–355.
[8] .M. Omar, N. Rahim, S. Mekhilef, "Three-phase syn-chronous PWM for flyback converter with power-factor correction using FPGA ASIC design," IEEE Transactions on Industrial Electronics 51, 2004 pp. 96106.
[9] Koutroulis, Eftichios, Apostolos Dollas, and Kostas Kalaitzakis. "High frequency pulse width modulation implementation using FPGA and CPLD ICs." Journal of Systems Architecture 52.6, 2006, pp. 332-344.

BIOGRAPHY

S.Raja received the B.E degree in Instrumentation and Control Engineering from Anna University-Chennai, through Arulmigu Meenakshi College of Engineering, Kanchipuram, Tamil Nadu, India in 2006, the M.Tech in Embedded Systems and Technology from SRM University, Chennai, Tamil Nadu, India in 2012. He is currently pursuing his Ph.D degree in the Department of Electrical and Electronics Engineering, SCSVMV University, Kanchipuram, Tamil Nadu, India. He is having more than 10 years of teaching experience in the Department of Electrical and Electronics Engineering, SCSVMV University, Kanchipuram, Tamil Nadu, India. His research interest includes BLDC Motor Drives, FPGA based design, and Low power VLSI design.

Dr.M.Rathinakumar, born in Madurai, Tamilnadu, India, on July 19, 1969. He graduated from Thiyagarajar College of Engineering, affiliated to Madurai Kamaraj University under Electrical and Electronics Engineering in the year 1993. He obtained his post graduation in Power Systems from the same University in the year 1995. He obtained his Ph.D from SCSVMV University, Enathur, Kanchipuram, Tamilnadu, India in the year 2010. He has put around 25 years of experience in teaching Electrical Engineering. His areas of interest are Power systems, Power Quality, Power System Operation and Control. Presently he is working as Professor in the Department of Electrical and Electronics Engineering, SCSVMV University, Enathur, Kanchipuram, Tamilnadu, India.



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