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Design of high speed low power Content Addressable Memory (CAM) using parity bit and gated power matchline sensing

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Abstract— Content Addressable Memory (CAM) offers high speed search function in single clock cycle. Due to its parallel matchline comparison, Content Addressable Memory power is hungry. In general CAM has three operation modes read, write, comparison. The comparison operation to perform n-input search data register into content addressable memory. The recent developments in the design of large capacity of content addressable memory. Thus robust design, high speed and low power Match-Line Sense Amplifiers are highly sought-after in CAM designs. In proposed system are introduced address search in memory location for sensing line, and matchline. A parity bit that reduces to sensing delay reduction. An effective gated power technique to reduce the peak and average power consumption. A feedback loop is employed to auto-turn off the matchline into power supply VDD. The gated power transistor px is controlled by a feedback loop denoted as power control which will automatically turn off once the voltage on the matchline reaches a certain voltage.
Index Terms— CMOS, content addressable memory (CAM), match-line.

I. INTRODUCTION

Content addressable memory (CAM) is a type of solid-state memory. In general, a CAM has three operation modes: READ, WRITE, and COMPARE [4].The comparison operation is performing to n-input search word into the search data register CAM [1]. Due to its parallel match-line comparison, CAM is power-hungry. The recent developments in the design of large-capacity content-addressable memory (CAM). A CAM is a memory that implements the lookup-table function in a single clock cycle using dedicated comparison circuitry. CAMs are especially popular in network routers for packet forwarding and packet classification, but they are also beneficial in a variety of other applications that require high-speed table lookup. However, the speed of a CAM comes at the cost of increased silicon area and power consumption, two design parameters that designers strive to reduce. As CAM applications grow, demanding larger CAM sizes, the power problem is further exacerbated. Reducing power consumption, without sacrificing speed or area, is the main thread of recent research in large-capacity CAMs.

The developments in the CAM area at two levels: circuits and architectures. First briefly introduce the operation of CAM and also describe the CAM application of packet forwarding. The input to the system is the search word that is broadcast onto the search lines to the table of stored data. The number of bits in a CAM word is usually large, with existing implementations ranging from 36 to 144 bits [1]. A typical CAM employs a table size ranging between a few hundred entries to 32K entries, corresponding to an address space ranging from 7 bits to 15 bits. Each stored word has a matchline that indicates whether the search word and stored word are identical (the match case) or are different (a mismatch case, or miss).

The match lines are fed to an encoder that generates a binary match location corresponding to the matchline that is in the match state. An encoder is used in systems where only a single match is expected. The operation of a CAM is like that of the tag portion of a fully associative cache. Many circuits are common to both CAMs and caches; however, we focus on large capacity CAMs rather than on fully associative caches, which target smaller capacity and higher speed.

Today's largest commercially available single-chip CAMs are 18 Mbit implementations, although the largest CAMs reported in the literature are 9 Mbit in size [1]. As a rule of thumb, the largest available CAM chip is usually about half the size of the largest available SRAM chip. This rule of thumb comes from the fact that a typical CAM cell consists of two SRAM cells, as we will see shortly. Chips versus time from 1985 to 2004, revealing an exponential growth rate typical of semiconductor memory circuits and the factor-of-two relationship between SRAM and CAM.

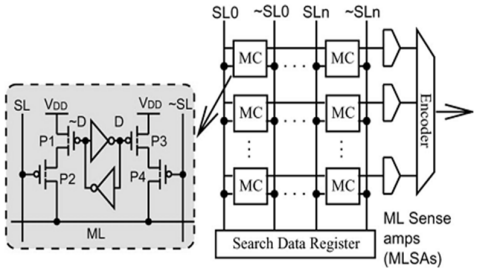


Fig 1: Block diagram of conventional CAM

The simplified block diagram of a CAM core with an incorporated search data register and an output encoder is shown in fig 1. It starts a compare operation by loading an -bit input search word into the search data register. The search data are then broadcast into the memory banks through pairs of complementary search-lines SLs and directly compared with every bit of the stored words using comparison circuits. Each stored word has a ML that is shared between its bits to convey the comparison result. Location of the matched word will be identified by an output encode. During a pre-charge stage, the ML are held at ground voltage level while both SL and ~SL are at V_{DD} .During evaluation stage, complementary search data is broadcast to the SL and ~SL. When mismatch occurs in any CAM cell (for example at the first cell of the row D= “1”; ~D “0”;SL “1”; ~SL “0”), transistor P3 and P4 will be turned on, charging up the ML to a higher voltage level.

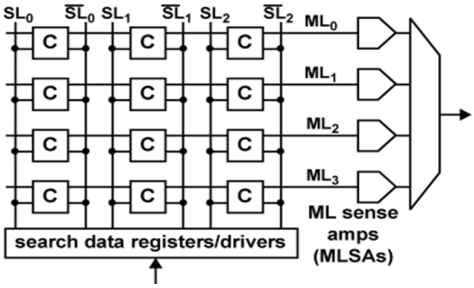


Fig 2: CAM Architecture

It consist of core cells. search line ,match line, MLSA and an encoder. Search data register is used to get the input from user, and will be compared with the memory bank through search line. Matchline sensing amplifiers are used to sense the voltage variations from the matchline. Encoder is used to identify the location of the output [1]. CAM search operation begins with pre-charging all match lines high, putting them all temporarily in the match state. The match lines are inputs to an encoder that generates the address corresponding to the match location. The content addressable memory is the modification of random access memory. Random Access Memory consist of read, write operation, Content Addressable Memory consist of read, write, and comparison operation.

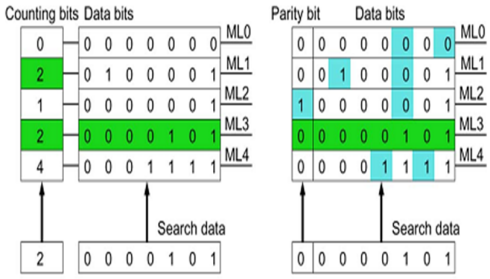


Fig 3: Preconventional CAM and Proposed Parity bit

Pre-Computation CAM Design: The pre-computation CAM uses additional bits to filter some mismatched CAM words before the actual comparison. These extra bits are derived from the data bits and are used as the first comparison stage. For example, in Fig. 3 number of “1” in the stored words are counted and kept in the Counting bits segment. When a search operation starts, number of “1”s in the search word is counted and stored to the segment on the left of Fig. 3. These extra information are compared first and only those that have the same number of “1”s (e.g., the second and the fourth) are turned on in the second

sensing stage for further comparison. This scheme reduces a significant amount of power required for data comparison, statistically. The main design idea is to use additional silicon area and search delay to reduce energy consumption.

The above mentioned pre-computation and all other existing designs shares one similar property. The ML sense amplifier essentially has to distinguish between the matched ML and the 1-mismatch ML. This makes CAM designs sooner or latter face challenges since the driving strength of the single turned-on path is getting weaker after each process generation while the leakage is getting stronger. Thus, we propose a new auxiliary bit that can concurrently boost the sensing speed of the ML and at the same time improve the performance of the CAM by two times. Parity Bit Based CAM: The parity bit based CAM design is shown in Fig. 3 consisting of the original data segment and an extra one-bit segment, derived from the actual data bits. We only obtain the parity bit, i.e., odd or even number of "1"s. The obtained parity bit is placed directly to the corresponding word and matchline. Thus the new architecture has the same interface as the conventional CAM with one extra bit. During the search operation, there is only one single stage as in conventional CAM. Hence, the use of this parity bits does not improve the power performance.

A parity-bit is search speed of the Content Addressable Memory.The parity bit based CAM sensing delay reduction.A power-gated sense amplifier is to improve the performance of the power.A feedback loop is employed to auto-turn off the power supply. The V_{DD}ML independently controlled by a power transistor (P_X) and a feedback loop that can auto turn-off the ML current to save power. The gated-power transistor P_X is controlled by a feedback loop, denoted as "Power Control" which will automatically turn off once the voltage on the ML reaches a certain threshold.

II. PROPOSED CAM STRUCTURE

Each CAM cell is powered by two power rails V_{DDML} for the compare transistors, V_{DD} for the SRAM transistors. The rail V_{DDML} of a row is connected to the power network V_{DDC} via a p-MOS device P_x which is used to limit the transient current. All the cells of a row will share the limited current offered by the transistor P_x, despite whatever number of mismatches.

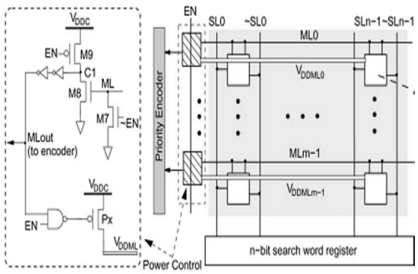


Fig 4: Proposed CAM Structure

At the beginning of each cycle, the ML is first initialized by a global control signal EN. At this time signal EN is set to low and the power transistor Px is turned OFF. CAM can be used to accelerate any applications ranging from local-area networks, database management, file-storage management, pattern recognition, artificial intelligence, fully associative and processor-specific cache memories, and disk cache memories. This will make the signal ML a C1 initialized to ground and V_{DD}, respectively. After that, signal EN turns HIGH and initiates the COMPARE phase. If one or more mismatches happened the CAM cells, the ML will be charged up. After a certain but very minor delay, the NAND2 gate will be toggled and thus the power transistor (P_X) is turned off again. As a result, the ML is not fully charged to V_{DD} but limited to some voltage slightly above the threshold voltage of M8.

III. GATED POWER ML SENSE AMPLIFIER DESIGN

Power gating technique is used to integrated circuits to reduce power consumption .By shutting of the current to blocks that are not in use. Power gating parameters are power gate size, gate control slew rate, simultaneous switching capacitance, power gate leakage. The power gating methods are four catagories , fine grain power method, coarse grain power gating method, isolation cells, retention registers.

The power gate must be selected to handle amount of switching current at any given time both p-MOS and n-MOS. Enable this is the control signal used to enable both write and read operation. All CAM operations are synchronous to the rising edge of the clock input. Encoder typically provides multiple bit of output. The matchline for all N rows couple to encoder. Search word input to the location in system search word.

A. *OPERATING PRINCIPLE*

The proposed CAM architecture is depicted in Fig. 4. The CAM cells are organized into rows (word) and columns (bit). Each cell has the same number of transistors as the conventional P-type NORCAM (shown in Fig. 1) and use a similar ML structure. However, the "COMPARISON" unit, i.e., transistors *M1-M4* , and the "SRAM" unit, i.e., the cross-coupled inverters, are powered by two separate metal rails, namely *VDDML* and the *VDD*, respectively. The VDDML is independently controlled by a power transistor (*Px*) and a feedback loop that can auto turn-off the current to save power. The purpose of having two separate power rails of (*VDDML* and *VDD*) is to completely isolate the SRAM cell from any possibility of power disturbances during COMPARE cycle. As shown in Fig. 4, the gated-power transistor *Px*, is controlled by a feedback loop, denoted as "Power Control" which will automatically *Px* turn off ML once the voltage on the reaches a certain threshold.

B. *CAM Cell Layout*

Fig. 5 shows the layout of the CAM cell using 65-nm CMOS process. Since the new CAM cell has a similar topology of that of the conventional design (except the routing of *VDDML*), their layouts are also similar. These two cell layouts have the same length but different heights. In the new architecture, *VDDML* cannot be shared between two adjacent rows, resulting in a taller cell layout, which incurs about 11% area overhead.

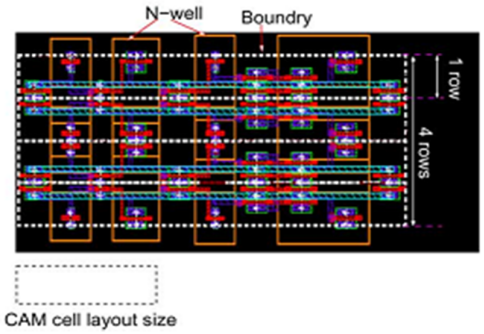
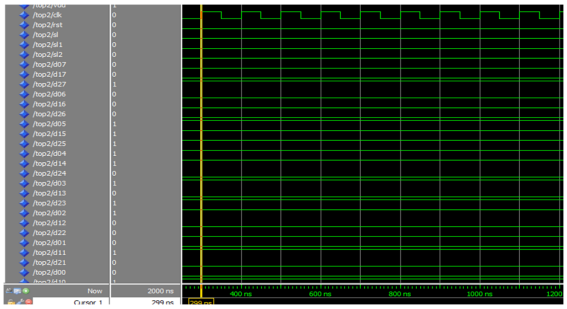
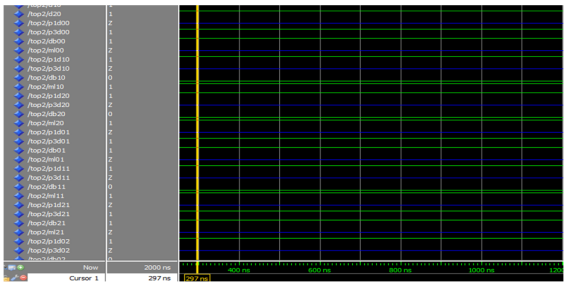


Fig 5: CAM Cell layout

IV. SIMULATION RESULTS AND ANALYSIS





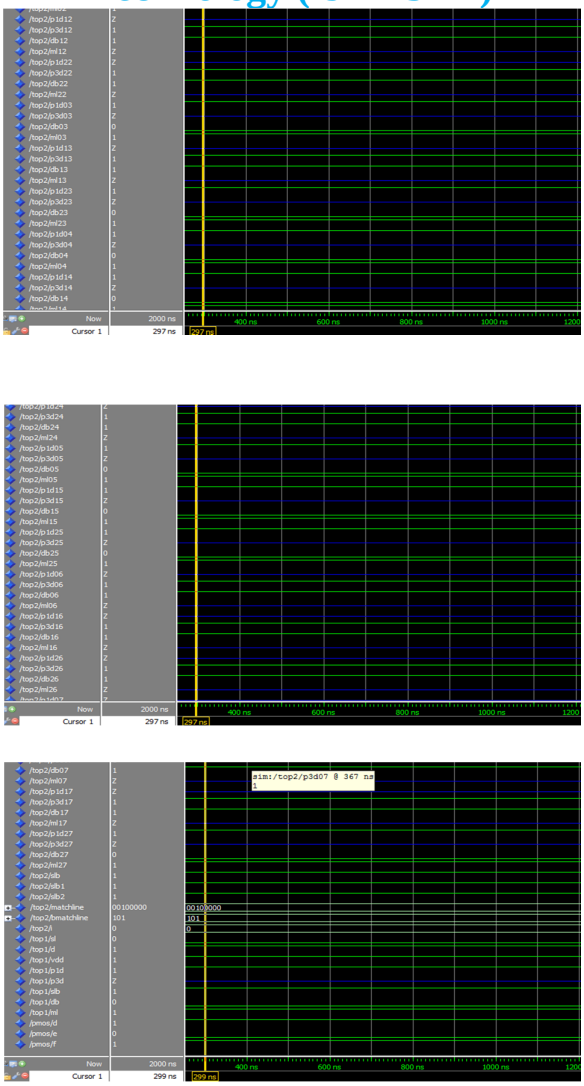


Fig 6: CAM Output waveforms

Snapshot is nothing but every moment of the application while running. It gives the clear elaborated of application. It will be useful for the new user to understand for the future step. The address space between the content addressable memory eight, and sixteen bits simulation in modelsim. In this simulation of content addressable memory sensing line sand match line operation eight bit. A Content Addressable Memory implement the three ways of operation one cell structure of CAM, matrix model of the CAM, and p-MOS using Content addressable memory in each line has 128 lines. The address space between the content addressable memory eight, and sixteen bits simulation in modelsim. In this simulation of content addressable memory sensing line sand match line operation eight bit. A Content Addressable Memory implement the three ways of operation one cell structure of CAM, matrix model of the CAM, and p-MOS using Content addressable memory in each line has 128 lines. Core matrix cells input are given by vdd—supply,clk—clock,rst—reset,sl,sl1,sl2 sensing line, sl=0,sl1=0,sl2=0,clk=0,rst=1,The invert sensing line ~sl=1,~sl1=1,~sl2=1.

The input values are given in sl, d, vdd.sl—sensing line, d—not gate value, vdd—supply.sl=1, d=0, vdd=1.The outputs are p1d, p3d—transistors,slb—invert of sensing line, db—invert of not gate, ml—matchline. ~slb=0,~db=1 .According to that sense line d, vdd, values both transistors p1d,p3d, values get changed. Inputs: d,e, Outputs : f when '0' | 'L' => f <= d - If f=0,the value of f=d when '1' | 'H' => f <= 'Z'- If f=1,the value of f=z(high impedence) when others => f <= '0' - otherwise the value 'f' become zero. It will be represented by either signal green or blue (high impedance).

The matchline value (7 down to 0),b matchline value (2 down to 0). When "00100000" =>b matchline<= "101" - when the match line value is "00100000" then the b matchline value is "101" . when others => ~b matchline<= "XXX" - when other

matchline values, the b matchline value does not exist. In this case clock input '1' and reset value will be '0' then changing the searchline and matchline 7 down to 0, ~b matchline 2 down to 0.

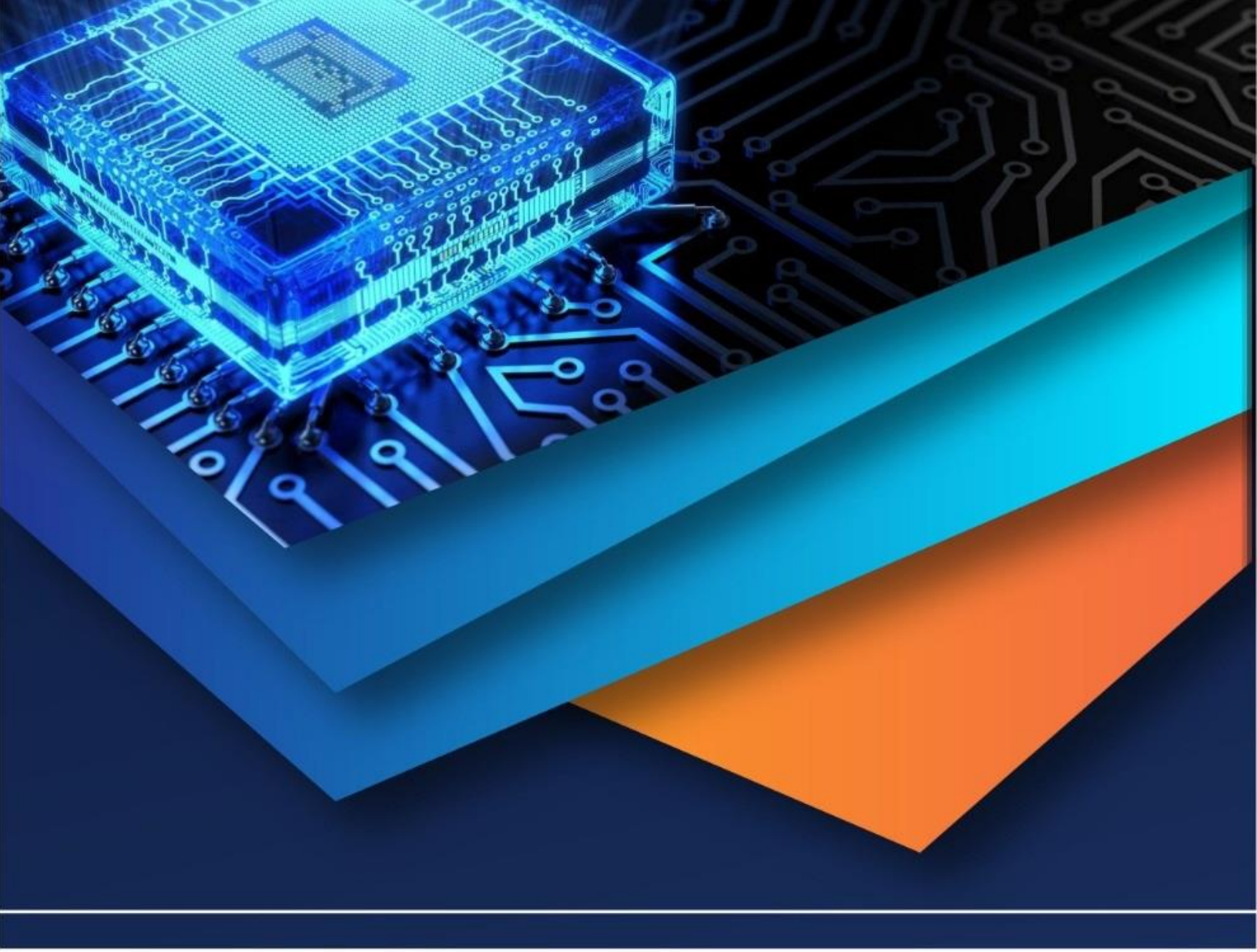
Matchline = 00100000
~b matchline = 101

V. CONCLUSION

The proposed an effective gated-power technique and a parity-bit based architecture that offer several major advantages, namely reducedpeak current (and thus IR drop), average power consumption, boosted search speed and improved process variation tolerance. It is much more stable than recently published designs while maintain their low-power consumption property. When compared to the conventional design, of Content Addressable Memory only at extremely low supply voltages. At 1 V operating condition, both designs are equally stable with no sensing errors. It is therefore the most suitable design for implementing high capacity parallel CAM in sub-65-nm CMOS technologies. In future we can develop match line in 16 bits. Now, we are giving sensing line input. But, in future we will call the value. If the match lines are correct, it will permit otherwise denied. It just like IP address checking or ATM applications.

REFERENCES

[1] K. Pagiamtzis and A. Sheikholeslami, "Content-addressable memory(CAM) circuits and architectures: A tutorial and survey,"IEEE J. SolidState Circuits, vol. 41, no. 3, pp. 712–727, Mar. 2006.
[2] A. T. Do, S. S. Chen, Z. H. Kong, and K. S. Yeo, "A low-power CAMwith efficient power and delay trade-off," inProc. IEEE Int. Symp. Circuits Syst. (ISCAS), 2011, pp. 2573–2576.
[3] I. Arsovski and A. Sheikholeslami, "A mismatch-dependent power allocation technique for match-line sensing in content-addressable memories,"IEEE J. Solid-State Circuits, vol. 38, no. 11, pp. 1958–1966,Nov. 2003.
[4] N. Mohan and M. Sachdev, "Low-leakage storage cells for ternary content addressable memories,"IEEE Trans. Very Large Scale Integr.(VLSI) Syst., vol. 17, no. 5, pp. 604–612, May 2009.
[5] O. Tyshchenko and A. Sheikholeslami, "Match sensing using matchline stability in content addressable memorys (CAM),"IEEE J. SolidState Circuits, vol. 43, no. 9, pp. 1972–1981, Sep. 2008.
[6] N. Mohan, W. Fung, D. Wright, and M. Sachdev, "A low-power ternary CAM with positive-feedback match-line sense amplifiers,"
IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 56, no. 3, pp. 566–573,Mar. 2009.
[7] S. Baeg, "Low-power ternary content-addressable memory design using a segmented match line,"IEEE Trans. Circuits Syst. I, Reg.
Papers, vol. 55, no. 6, pp. 1485–1494, Jul. 2008.
[8] K. Pagiamtzis and A. Sheikholeslami, "A low-power content-addressable memory (CAM) using pipelined hierarchical search scheme,"IEEE J. Solid-State Circuits, vol. 39, no. 9, pp. 1512–1519, Sep. 2004.



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