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3-D Field Programmable Gate

Interconnect Faults by Testing and Diagnosis

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Abstract - The emerging three-dimensional (3D) integration technology is one of the promising solutions to overcome the barriers in interconnect scaling, thereby offering an opportunity to continue performance improvements using CMOS technology. As the fabrication of 3D integrated circuits has become viable, developing CAD tools and architectural techniques are imperative for the successful adoption of 3D integration technology.
A brief introduction on the 3D integration technology has been proposed, and then reviewed the EDA challenges and solutions that can enable the adoption of 3D ICs, and finally presented the design and architectural techniques on the application of 3D ICs, including a survey of various approaches to design future 3D ICs, leveraging the benefits of fast latency, higher bandwidth, and heterogeneous integration capability that are offered by 3D technology.
Keywords- 3D integrated circuits, interconnect scaling, architectural techniques, 3D technology

I. INTRODUCTION

FPGA's are used to implement the logic functions. They have both analog as well as digital features. FPGA's contain components called logic block and the hierarchy of interconnects which connects the blocks together. These logic blocks are configured.
To perform combinatorial as well as memory elements. FPGA's have the advantage of re-program in the field to fix bugs. FPGA's have many programmable logic blocks which provides the basic computation and storage elements used in digital systems. Apart from basic logic block, modern FPGA's contains different blocks, which can only be used for specific functions. These devices are based around a matrix of Configurable Logic Blocks (CLBs) connected through Programmable Interconnects.
Time to market factor is shorter and lower non-recurring engineering costs. Some FPGAs can be reconfigured partially that lets one portion of the device be reprogrammed while other portions continue running. FPGAs use dedicated hardware for processing logic and do not have an operating system. Since the operations are carried out parallel, the performance of one part of the application is not affected when additional processing is added. Multiple control loops can run on a single FPGA device at different rates.

II. FPGA ARCHITECTURE

The generic architecture of FPGA consists of resources like configurable logic blocks, input/output blocks or pads, interconnection wires/switch matrix. Modern FPGAs contain up to hundreds of thousands of CLBs. The basic FPGA architecture has 2 Dimensional arrays of logic blocks with a means for the user to configure the interconnection between the logic blocks and the function of each logic block.
A configurable logic block contains digital logic, inputs. It implements user logic. Interconnects provides routing between the logic blocks to implements the user logic. Switch matrix provides switching between interconnects depending on the logic. Input / output pads used for outside world to communicate in applications. SRAM-based island-style FPGA architecture has been used.

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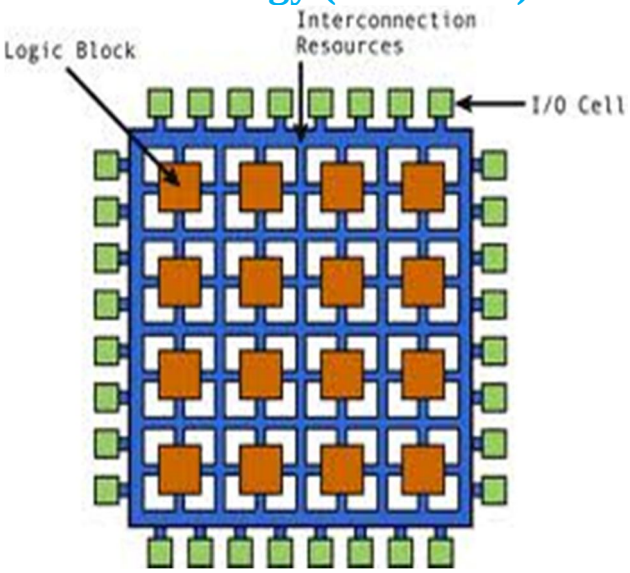

Fig.1. 3-D FPGA architecture

3D FPGA is having CLB configuration which is based on anti fuse. These anti fuses will have the connectivity of configuration.
3D FPGA'S has a technology of two layers that can be a relaxed lithography used for programming transistors. The novel technologies will be interconnected in between the device layers at the particular featured size. They are easily integrated with lower and higher terrains.
The high density of the uninterrupted is having a very high voltage programming devices in the 3D FPGA's. They have maximum programming element density approaching the maximum size density.

III. FAULT MODELS

Fault models are used for identifying the targets which are mostly occurred for testing and they have a limited scope for the test pattern generation in which they creates the tests for the modeled faults only.
We have different fault models like single stuck-at fault models, memory faults, delay faults and analog faults. And also we will test the different testing's for the 3-D FPGA's by fault diagnosis and test set generations for the detecting stuck-at faults at particular testing circuits.

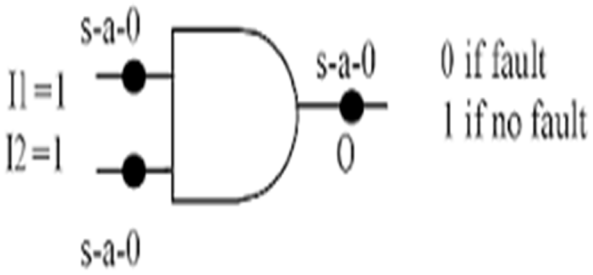

Fig.2. Single Stuck-at Fault Model

A. Line Stuck-at Fault(LSA) Injection and Collapsing Fault model

Generally the FPGA's will inject the LSA inputs and outputs at particular LUTs. By this the LSAs will know the exact inputs that are active in LUTs. And also they can detect the possible number of the faults in the terms of 2,4,6,8 and 10 for each LUTs in accordingly with the inputs like 0, 1, 2,3 and 4.

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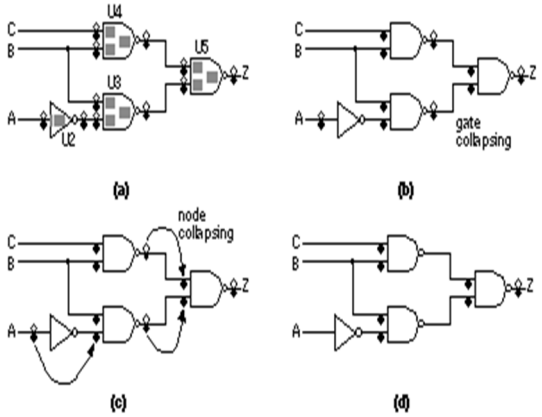

Fig.3. Line Stuck-at Fault (LSA) Injection and Collapsing Fault model

B. Combination Stuck-At(CSA) Fault model

The fault simulation will be done for evaluating the fault coverage matrices and the test qualities, every LUT nodes will be having a detection of LSA faults and the fault universe.

IV. TESTING OF 3-D FPGA

During the normal operation of the circuit, the testing will be performed by using the scheme of BIST .Generally BIST is a technique used for the capability of performance at the speed testing in high fault coverage and they reliance on external equipment.

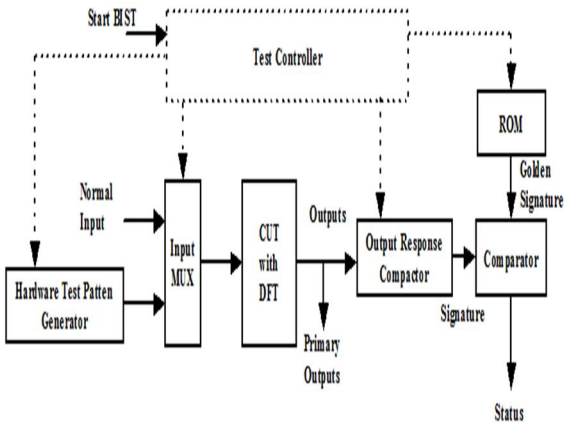

Fig.4. BIST Circuit

During the normal operation of the circuit there are certain modes like No test mode and Real time error detection. In online-BIST the normal functional operation occurs simultaneously. And non concurrent will carry out when it is idle state because interruptible will be realized out by the executing the software routines.

And the other type of BIST is Offline BIST, which deals with the testing of a system when it is not carrying out the normal functional operations in the circuit. And there are two types of the modes i.e., Test mode and Non real –time error detection mode.

V. FAULT DIAGNOSIS METHODS

We have different fault models in under the different patterns in which they behave like single and multiple fault diagnosis. We

have the primary inputs pseudo primary inputs and the outputs will refer the primary outputs and pseudo primary outputs

A. *Fault Element Graphs*

Fault element Graphs (FEGs) are used for constructing the combined effects of multiple fault effects. And can be identified by the by using FEG in keeping the track of multiple fault elements in the particular faults.

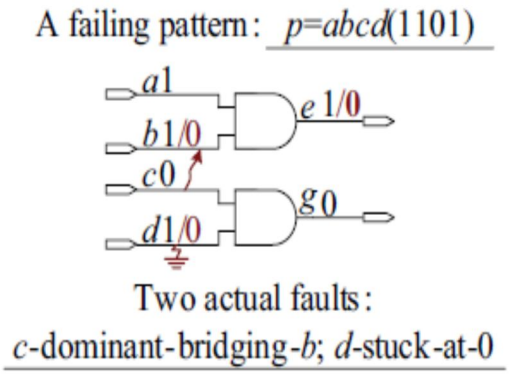

Fig.5. Example of Fault Elements

By the consideration of one fault for identifying the multiple fault effects so that the candidate locations can be iteratively identified by the by their fault elements by using FEGs.
So that the fault locations will be identified by the fault elements and the FEGs will be reduced to null.

B. *Fault Diagnosis by using Multiple Faults*

Multiple fault diagnosis is one of the faults masking and reinforcing effects for detection in which fault masking will be occurred when the propagation path will be blocked by the other faults because of the fault effect that has been propagated by the other values blocking the changed values in the fault effects.

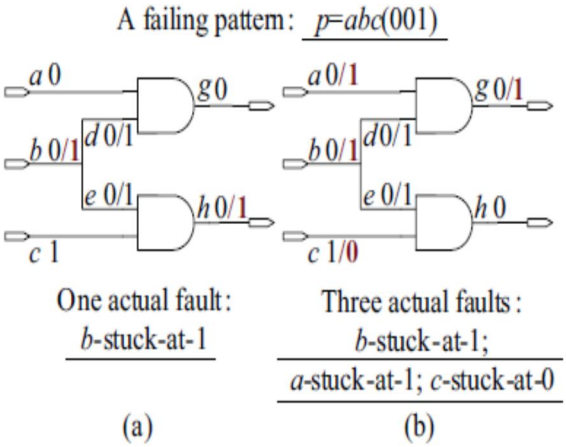

Fig.6. Example of Multiple Fault Effects (a) Single fault, (b) multiple faults with masking and reinforcing effects.

Under the Fig. 6(a) only one fault element will exist as 1/p and one failing output as p. And Fig. 6(b) illustrates the two elements as existing a/1/p and c/0/p and b/1/p will under masking by c/0/p and a/1/p will be reinforcing. And then the output will be changing

from h to g.

C. *Fault Insertion*

Fault Insertion requires the insertion of the faults by the test generation vector and fault testing which copies the into the circuit and compares the output with the working of the circuit. Checkpoints are defined as the consistence of the primary inputs and fan out branches which occur in the circuit.

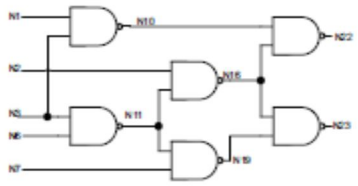

Fig.7. C17 Schematic Diagram

In the Fig.7 we are using C17 by the reference of ISCAS bench mark suite. The wire will appear once will be stored in another vector, whenever the fault is detected. When the parent column is containing the same node more than once, then the node is detected as fan out and it's a NULL parent node and this node is considered as primary node.

At every check point we will insert a multiplexer having one input to the original gate input so that the second input will be considered as either stuck-at 1 or 0.

We will select the mux-select as a signal in between the fault data and correct data.

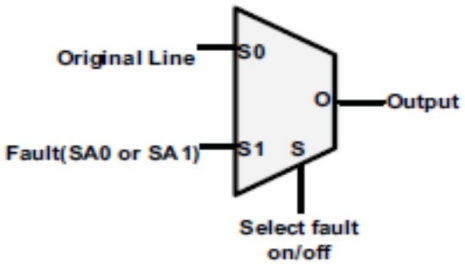

Fig.8. Fault insertion multiplexer

In Fig.8 the multiplexer will be added for the identification of the nodes so that the identified nodes will be the primary inputs. Finally the multiplexer output will be as original signal output defined as '0'. The process will be repeated with the multiplexer and at each fan out node and checkpoints at each node in the circuit.

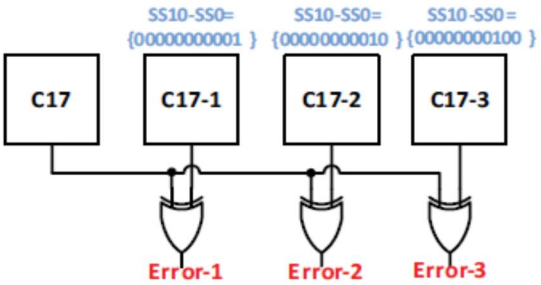

Fig.9. Fault free C17 will be activated by SS10 and SS0

The Fig. 9 illustrates the C17 circuit with three instantiations by using different multiplexer signals. As per the circuit, C17-1 has the select lines of SS10-SS0. Similarly, the multiplexer lines will be associated with the SS1 SS2 lines in the terms of C17-2 and C17-3 too.

As shown in the figure, the fault free circuit will be compared with the fault output by using XOR-gate.

VI. CONCLUSION

We have described about the introduction 3-D FPGA's. In, the architecture of 3-D FPGA's we have described the CLB configuration, and the technology used for the 3-D FPGA's. Then with proposed concept of Testing and fault diagnosis, we have briefly described about what exactly is a fault. How a fault does occurs in 3-D FPGA's.

Fault models have different types of faults, which are involved and used for the fault detection in FPGA's. We are implementing fault models like Line Stuck-at Fault (LSA) Injection and Collapsing Fault model, Combination Stuck-at (CSA) Fault model, and we implemented Testing in FPGAs so that by using BIST we can detect the faults in the circuit.

We are implementing different types of fault diagnosis methods for 3D technology these methods may help in the detection of faults in the circuits like Fault element graphs, fault diagnosis by using multiple faults, and fault insertion.

In this paper, we are implementing different methods for finding out the faults and that can be detected easily so that the performance will be high and also they will have highest SDFC nearly 90%, and stability will also gets increases.

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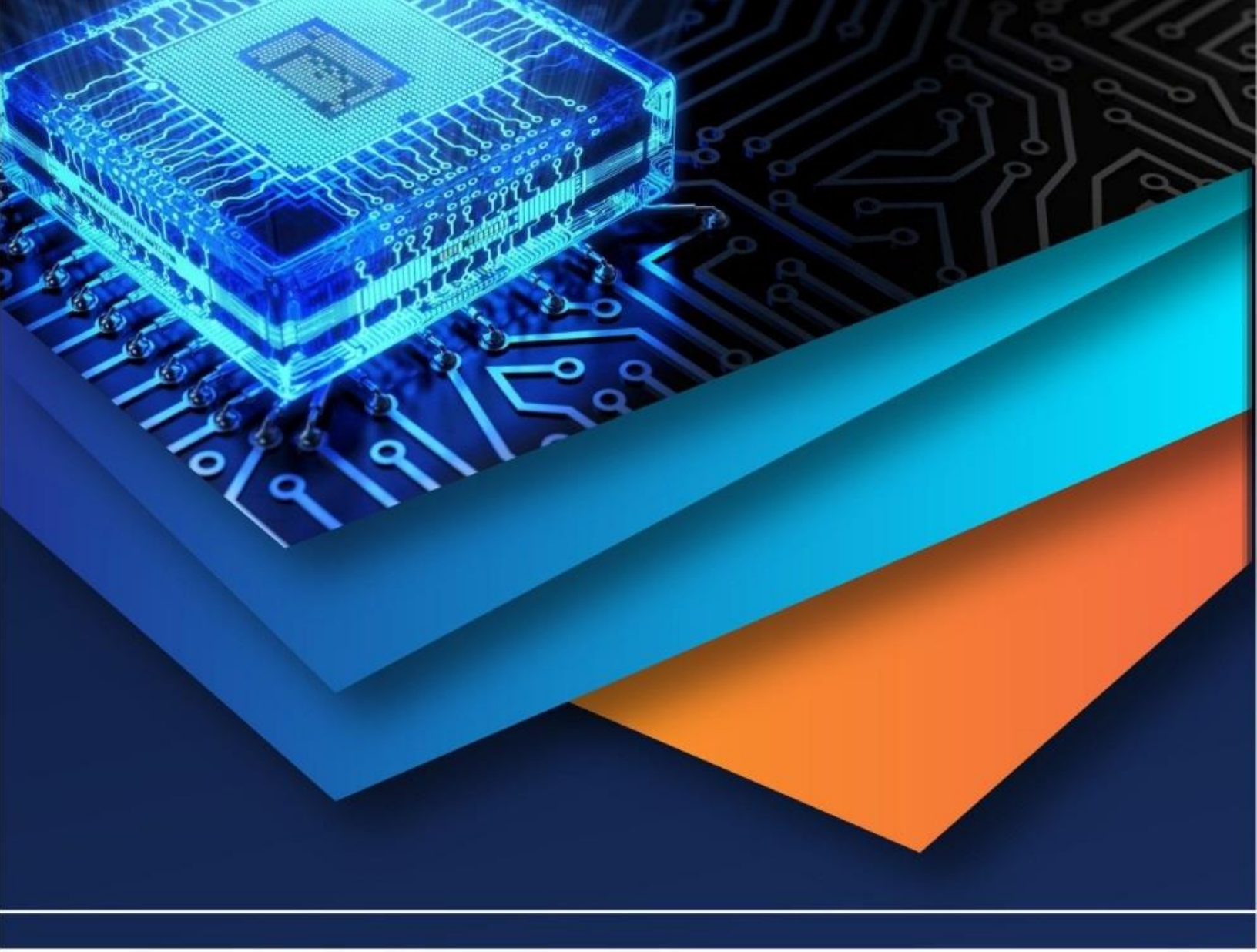

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