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A Substrate Biased Full Adder Circuit

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Abstract— With the recent advances in the VLSI design and technology, the challenge in the design complexity of IC has grown. One of the major challenges is to design logic with power minimization. This is due to two reasons; one is the long battery backup for mobile and portable devices and second is due to increase in number of transistors packed in a single chip which will lead to reliability problems. As addition is one of the indispensible operations in digital system we selected the basic full adder and the substrate biased full adder. The design criterion of a full adder is usually multi – fold. In this paper we did a comparative study based on the number of transistor used. The circuits are simulated in a famous EDA tool ORCAD. The results show that there is a considerable reduction in transistor count with respect to substrate biasing. In future these adders can be developed into an enhanced ALU with added features.
Keywords— CMOS adder, ORCAD, Substrate biased adder, transistor count, XOR Gate.

I. INTRODUCTION

Low speed and high performance are the design trade off in the field of VLSI design. In recent days the performance of a chip can be considered as an analogy for speed. The extensive development in the field of portable systems and cellular networks has intensified the research efforts in low power microelectronics. The low-power design has become a major design consideration. The design criterion of a full adder cell is usually multi-fold. Transistor count is, of course, a primary concern which largely affects the design complexity of many function units such as multiplier and algorithmic logic unit (ALU). This paper makes an effort to design some basic digital circuits with an improved CMOS transistor model [1], supported by mathematical and logical equations. In this paper the basic analysis of CMOS model is described and then used this model to design Full adder circuit. Then it describes the substrate biased CMOS model and using this model the Full adder circuit is designed. Then it concludes the improvement in number of transistor used.

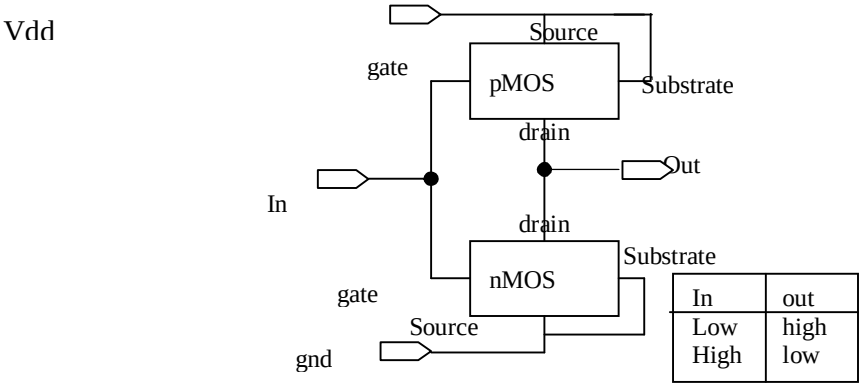
II. CMOS TRANSISTOR MODEL

A. CMOS Transistor

A Complementary MOS transistor consists of both nMOS and pMOS devices. The gate terminal of an nMOS transistor controls the flow of current between the source and drain. When the gate is low, the nMOS transistor is OFF and almost zero current flows from source to drain. A pMOS transistor is just the opposite, being ON when the gate is low and OFF when the gate is high.

B. CMOS Inverter

A basic CMOS inverter is given in Fig.1 along with its truth table. It should be noted that the substrate is connected to source in conventional CMOS inverter.



In	out
Low	high
High	low

Figure1. The circuit of a CMOS inverter with its truth table

C. Substrate Biased CMOS Inverter

The pMOS substrate is biased to the supply voltage Vdd, so that additional positive charge carriers are supplied to the n – type substrate. In this case unlike a conventional circuit, the source is not shorted to the substrate. Moreover this is not forward body biasing, but it is again a reverse biased p – n junction between source to substrate, with an increased strength of reverse supply.

This reverse biasing will help to make available positive charge carriers at the inversion region formed beneath the gate, at required gate voltage[2]. This will help the formation of the p – type channel, irrespective of the source potential and help in conduction as assumed by the model given in Fig. 2. So biasing the pMOS substrate to the supply voltage and nMOS substrate to the ground will help the given model to work as desired. The Boolean equation for this can be given as below

$$Out = (in1.(in2)')+(in2.in3) \quad (1)$$

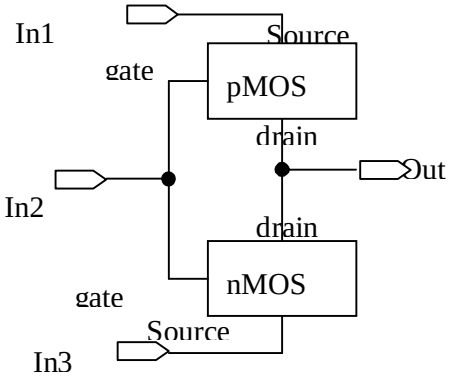


Figure2. CMOS Transistor Model for

III.SUBSTRATE BIASED CMOS

A. Implementation Of Gates

The CMOS model developed in the previous section helps in defining a new and efficient concept of designing the logic circuits and devices. To design a AND gate with A and B as inputs and Out as output, the logic equation should be

$$Out = A.B \quad (2)$$

Hence from equation (1) to get the AND gate output, we should make in1 as zero.

$$Out = (0.(in2)')+(in2.in3) \quad (3)$$

$$Out = (in2.in3) \quad (4)$$

In conventional AND gates 3 CMOS gates are required, but now it uses only 1 CMOS. Thus the number of transistors is reduced as we expected. The simulation of 2 input substrate biased AND gate and its output waveform is shown in Fig. 3a and Fig. 3b respectively. Similarly to design a OR gate, in3 is made as high, which reduces the equation (1) as

$$Out = (in1.(in2)')+(in2.1) \quad (5)$$

$$Out = in1+ in2 \quad (6)$$

To design a XOR gate, in3 is made as equal to inversion of in1, which reduces the equation (1) as

$$Out = (in1.(in2)')+(in2.(in1)') \quad (7)$$

$$Out = in1 \ominus in2 \quad (8)$$

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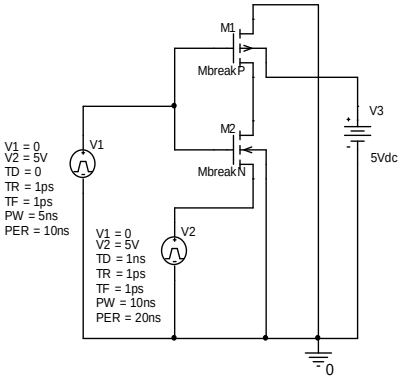

Figure3a. Circuit Diagram of AND gate

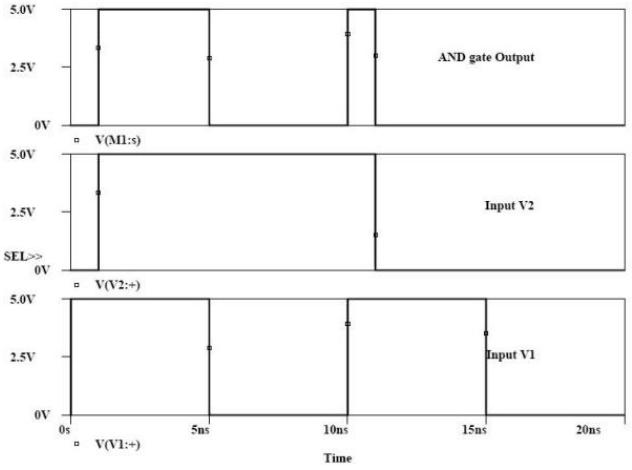

Figure3b. Output Waveform of AND gate

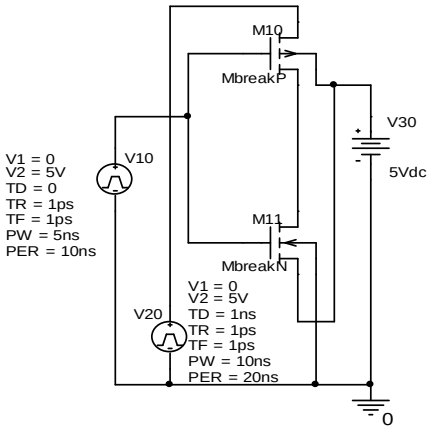

Figure 4a. Circuit diagram of OR gate

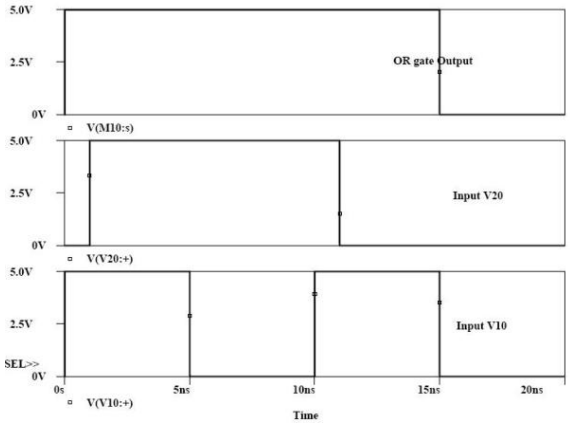

Figure 4b Output waveform of OR gate

The simulation of 2 input substrate biased XOR gate and its output waveform is shown in Fig. 5a and 5b

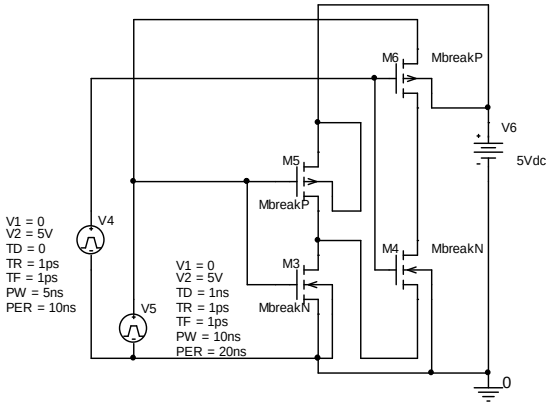

Figure 5a The Circuit diagram of XOR gate

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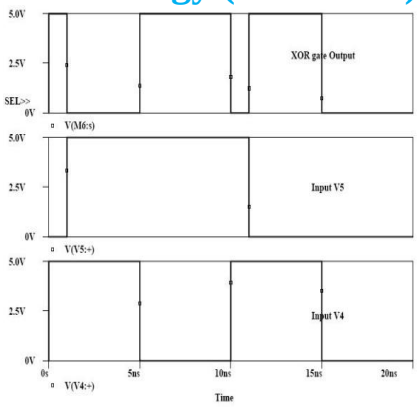


Figure 5b. The Output waveform of XOR gate

B. Design Of Full Adder

A combinational circuit consists of logic gates whose outputs at any time are determined directly from the present combination of input without regard to previous inputs. Arithmetic circuits fall under the category of combinational circuit. Adders form an basic component in applications like DSP architectures , microprocessor etc. The binary adders are used to add two binary numbers. Apart from basic addition the arithmetic operations that can be computed in electronic component are Shift/extension operation, equality and Magnitude comparison, increment/decrement, Complement, Sum, Multiplication, division, square root, trigonometric functions [3]. Hence we started out work with the basic adders. The full adder accepts three inputs – two input bits and the input carry, and generate sum output and carry output. The logic equations can be given as

$$Sum = A \oplus B \oplus C \quad (9)$$

$$Carry = (A.B) + (B.C) + (C.A) \quad (10)$$

The logic diagram for the full adder is shown below in Figure 6.

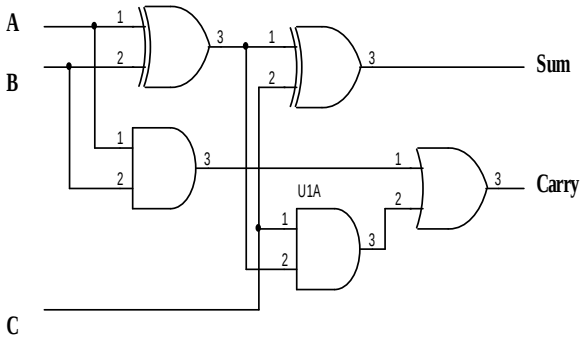


Figure 6. The Circuit diagram of Full adder

The Table 1 shows the truth table of a full adder which includes all the possible combinations of inputs.

Table1. Truth table of a Full Adder

Inputs			Outputs	
A	**B**	**C**	**Sum**	**Carry**
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The logic diagram of a full adder consists of two numbers of XOR gates, two numbers of AND gates and one number of OR

gate. So to implement a full adder a sum of 10 CMOS devices are needed as summarized in Table2

Table 2 Details of CMOS required for Full Adder

Gates for FA	No of CMOS	No of gates	No of transistors
XOR	4	2	16
AND	3	2	12
OR	3	1	6
Total	10	5	34

But if substrate biased gates are used then it requires only 5 CMOS devices as summarized in Table3.

Table 3 Details of CMOS required for Substrate biased Full Adder

Gates for FA	No of CMOS	No of gates	No of transistors
XOR	2	2	8
AND	1	2	4
OR	1	1	2
Total	4	5	14

Hence the substrate biased full adder is simulated with PSPICE schematic Entry. The number of transistors used is 14 instead of 34 as in the case of conventional CMOS Full adder.

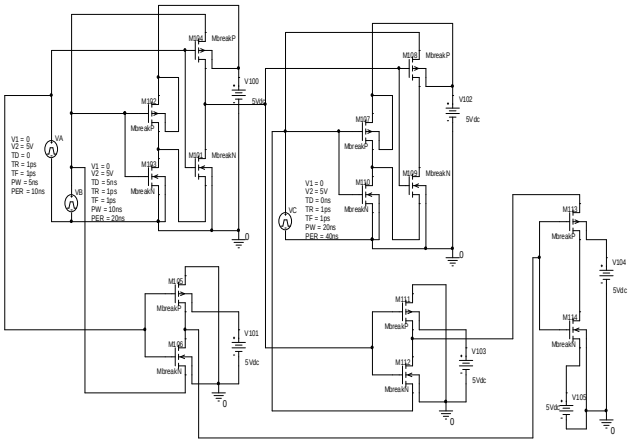
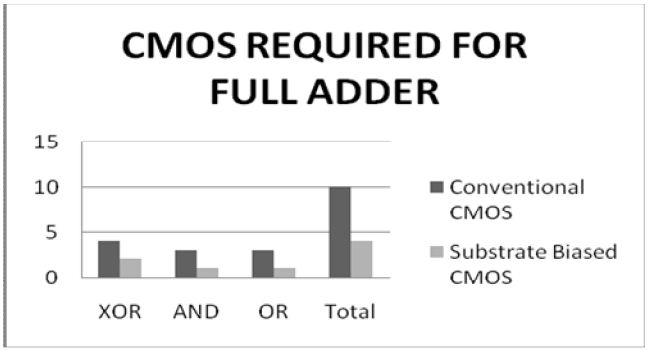


Figure7. Substrate biased Full adder circuit

The following Figure compares the number of CMOS required for implementation of Full adders with respect to conventional CMOS and Substrate biased CMOS.



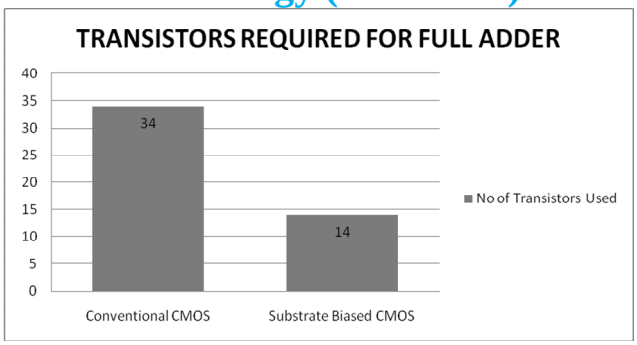


Figure 8. Comparison of Substrate biased and Conventional CMOS devices

IV. CONCLUSIONS

From the results it can be observed that the number of transistors required to implement a Full adder is reduced considerably from 34 to 14. Thus we get the expected output. If this technique is implemented for other architectures the transistor count will be reduced. Even this full adder architecture can be enhanced by using multiplexer instead of gates which will further reduce the transistor count through which the power consumption is reduced.

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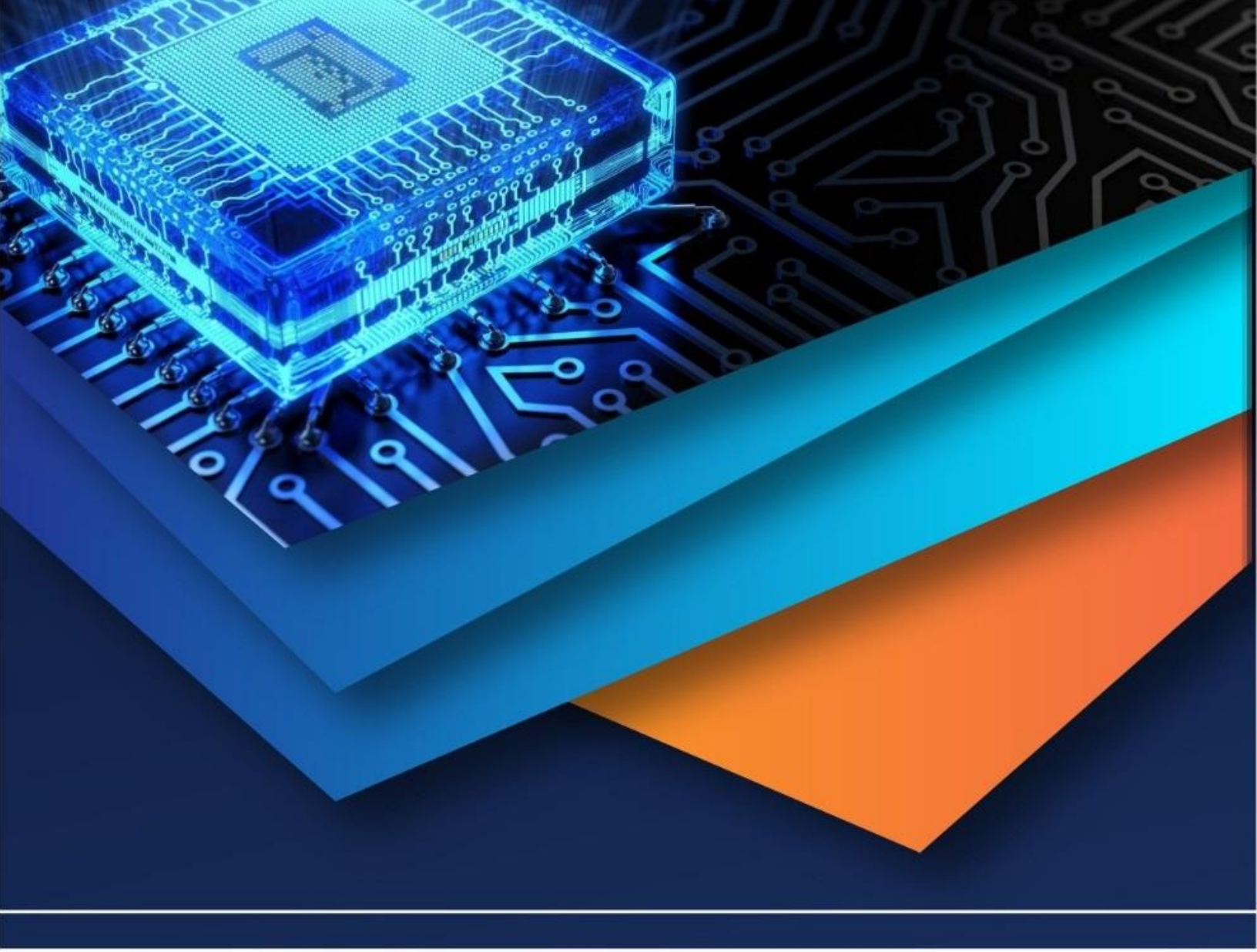

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