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# Electronic Design Automation Tool: a Comparative Study

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***Abstract:*** ***Teaching and evaluation of questions related to computer programming, circuit designing, mathematical problems is a critical part in engineering courses. Lot of efforts and time needs to be put by the faculties to teach and evaluate such domains. The questions in this domain are considered to be logical and hence can be solved in multiple ways. In this scenario, evaluation becomes significantly more complex and hence more time consuming and tricky. After conducting an exam of 2 hours, faculty at times need to spend more than 5 to 6 hours to evaluate the submission properly. This takes huge efforts as well as lot of time is consumed to intimate the result. Circuit design is a one of the most common subject in engineering courses. Creation of physical circuits using hardware and testing their validity is expensive and time consuming for students as well as faculties. Alternative teaching method for creation of circuit is virtualization of hardware activities into software solutions. One such solution is EDA tool. An Electronic Design Automation (EDA) tool serves as a learning, experimentation and evaluation tool in teaching-learning environment. These modern electronic design methods help faculties and students to draw and simulate circuit designs effortlessly. Once a circuit has been designed, it can be saved and tested multiple times, with different inputs to check its validity. In this research paper, we have done comparative study of three most widely used EDA tools namely QUCS, LT Spice and e-Sim.***
***Keywords: EDA, Rectifier, QUCS, LTspice IV, OSCAD***

## I. INTRODUCTION TO EDA (ELECTRONIC DESIGN AUTOMATION) TOOLS

Electronic chip designing is one of the complex tasks for chip designers. A prototype chip created using hardware involves high cost and at times high failure rates too. Today it is possible to simulate the design of a chip using computer and proper software tools. Electronic Design Automation is an approach, where a software tool used to design and simulate the working of an electronic circuit[2]. An EDA tool allows creation of proper engineering electronic design. The circuit designs creates a designs, simulates it, corrects problem if needed and implement the design. It provides flexibility and reduces the work of designer. EDA tool thus has a huge potential usage in teaching of circuit design. It can be used by teacher and student for simulating and evaluating a circuit design. In this research paper, we have studied some existing EDA tools. By doing this, we hope that this work would help other researchers to identify the strengths and weakness of different EDA tools compared here. The comparison has been done by simulating a half wave rectifier circuit design in different EDA tools. The circuit that has been simulated in this paper is half wave rectifier. The half wave rectifier is used to convert AC voltage to DC voltage. As electronic devices work on the DC voltage supply only, rectifiers are used in all electronic devices. Half wave rectifier is used to rectify only half cycle of the waveform. In the simulation scenario, AC input is given to the rectifier circuit. These inputs are for positive and negative cycles. The half wave rectifier works only on positive half cycle. It omits negative cycle. Fig. 1 shows the half wave rectifier circuit design.

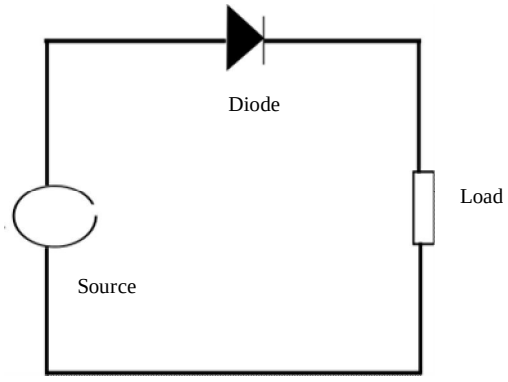


Fig. 1 Half wave rectifier

## II. CIRCUIT SIMULATION

Circuit simulation shows the behaviour of electronic devices or circuits. Traditionally, electronic circuits were modelled and simulated using special-purpose electronic circuit simulators. Although a number of such simulation tools have been made available over the years, the one tool that has been most successful in conquering the market is SPICE (Simulation Program with Integrated Circuit Emphasis) [1]. SPICE was released in 1972 by the University of California at Berkeley. It is a general-purpose circuit simulator. It can simulate broad range of circuit families, circuit sizes, and has many analysis options. Today over 10,000 copies of the program are in use world-wide, making it without doubt the most successful single program for electronic circuit design ever developed. SPICE simulator describes device models and circuit data in text format called netlist.

## III. SIMULATION OF HALF WAVE RECTIFIER USING EXISTING EDA TOOLS

EDA tools like KiCAD, Logisim, ORCAD, PSPICE, NGSPICE and many more are widely used in academic environment. Each EDA tool has its own interface and working methodology. In this section we have discussed the characteristics, interface, input file format, output file format and simulation scenario of QUCS, LTspice IV and eSim EDA tools.

### *A. Quite Universal Circuit Simulator (QUCS)*

The Quite Universal Circuit Simulator (QUCS) [4] is an educational and open source software program. It helps to generate schematic diagrams and check their performance. It has vital component library which includes lumped components, sources, probes, transmission lines, nonlinear components, digital components, various simulations, file components, diagrams and paintings. It takes a netlist file, checks it for errors, performs the required simulation actions, and finally produces a dataset. Simulation data can be represented in various types of diagrams, including Smith-Chart, Cartesian, Tabular, Polar, Smith Polar combination, 3D-Cartesian, Locus Curve, Timing Diagram and Truth Table. It uses FreeHDL and Icarus Verilog for VHDL and Verilog digital simulation respectively. Qucsator simulation engine is used for simulation of circuit designs in QUCS. SPICE netlists can be read and simulated by QUCS using conversion program Qucsconv. Recent version Qucs-0.0.19/S is compatible with ngspice and Xyce. It has spice4qucs structure which helps to simulate spice netlist format circuits. ngspice and Xyce are an open source spice compatible analog circuit simulator. Fig. 2 shows transient simulation of half wave rectifier. Fig. 3 shows half wave rectifier simulation using QUCS. In the Fig. 3 blue coloured signal is input while red coloured signal is output. In this diagram AC Voltage source with 5v and frequency=100Hz has been applied. Ideal diode and a load register with 100ohm are used. Labels "IN" and "OUT" are used for the input and output sides of the circuits. To simulate circuit transient analysis is used. In transient analysis, dataset contains voltage or current information over time. The start time of the transient simulation is set to 0 and the stop time to 100ms which will include 100 periods of the input signal. Fig. 3 shows peak output voltage 4.2 V due to the voltage drop 0.8V at diode while Fig. 4 shows same in .csv format. This .csv file can be used for evaluation of circuit design. Fig. 5 show the netlist file of half wave circuit design using QUCS. This file includes list of components which are taken in circuit design and interconnection information of components. QUCS cannot directly simulate standard SPICE circuit netlists but requires them to be converted to their QUCS equivalent prior to simulation.

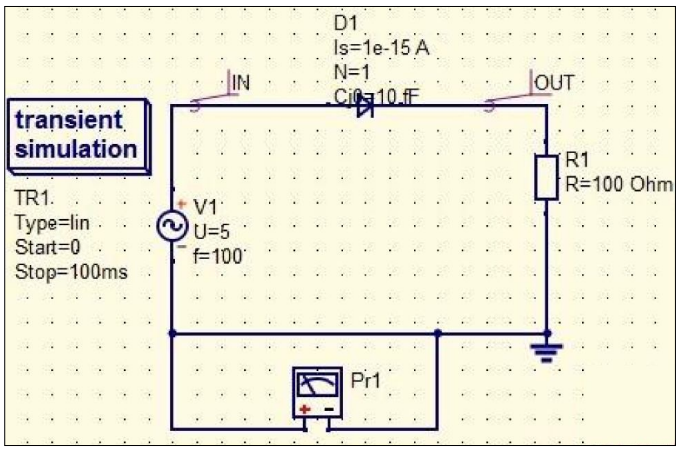


Fig. 2 Half wave rectifier schematic design using QUCS

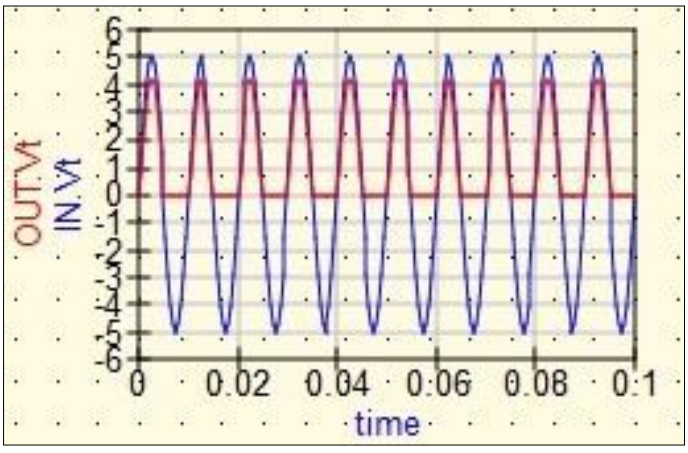


Fig. 3 Half wave rectifier simulation using QUCS

| time | r Pr1.Vt |
|---|---|
| 0 | 0 |
| 0.0005 | 0.835416 |
| 0.001 | 2.20418 |
| 0.0015 | 3.2999 |
| 0.002 | 4.00509 |
| 0.0025 | 4.24829 |
| 0.003 | 4.00509 |
| 0.0035 | 3.2999 |
| 0.004 | 2.20418 |
| 0.0045 | 0.835416 |
| 0.005 | -3.46247e-08 |
| 0.0055 | -1.33394e-08 |
| 0.006 | -7.84562e-09 |
| 0.0065 | -1.04155e-08 |
| 0.007 | -1.51261e-10 |
| 0.0075 | -3.32697e-09 |
| 0.008 | 6.80256e-09 |
| 0.0085 | 3.76425e-09 |
| 0.009 | 1.44696e-08 |
| 0.0095 | 1.33442e-08 |
| 0.01 | 3.44543e-08 |

Fig. 4 .csv file of simulated data of half wave circuit design using QUCS

```
# Qucs 0.0.18  C:/Users/poonam/.qucs/half_wwave_paper.sch

R:R1 gnd OUT R="100 Ohm" Temp="26.85" Tc1="0.0" Tc2="0.0" Tnom="26.85"

Diode:D1 OUT IN Is="1e-15 A" N="1" Cj0="10 fF" M="0.5" Vj="0.7 V" Fc="0.5"
Cp="0.0 fF" Isr="0.0" Nr="2.0" Rs="0.0 Ohm" Tt="0.0 ps" Ikf="0" Kf="0.0"
Af="1.0" Ffe="1.0" Bv="0" Ibv="1 mA" Temp="26.85" Xti="3.0" Eg="1.11" Tbv="0.0"
 Trs="0.0" Ttt1="0.0" Ttt2="0.0" Tm1="0.0" Tm2="0.0" Tnom="26.85" Area="1.0"

VProbe:Pr1 gnd gnd

Vac:V1 IN gnd U="5" f="100" Phase="0" Theta="0"
.
TR:TR1 Type="lin" Start="0" Stop="100ms" Points="201" IntegrationMethod="Trapezoidal"
Order="2" InitialStep="1 ms" MinStep="1e-16" MaxIter="150" reltol="0.001" abstol="1 pA"
vntol="1 uV" Temp="26.85" LTEreltol="1e-3" LTEabstol="1e-6" LTEfactor="1" Solver="CroutLU"
relaxTSR="no" initialDC="yes" MaxStep="0"
```

Fig. 5 Netlist file of half wave circuit designed using QUCS

*B. LTspice IV*

LTspice IV [6] is freeware EDA tool. It is produced by semiconductor manufacturer Linear Technology. Its simulation is based on SPICE. It has schematic design area and waveform viewer. LTspice IV can import third party models. It allows different types of analysis such as transient, noise, AC and DC. Efficiency reports can also be generated. PCB layouts cannot be using created this tool. This tool can be good for analog circuit designs. It cannot be useful for complex digital circuit designs. Foreign models of components can be imported from web in this tool. Lossy cable simulation is also possible with this tool. Fig. 6 shows transient simulation of half wave rectifier using LT spice. We have used diode, register and AC voltage source. Configuration of components as given in the first circuit. Fig. 7 shows peak output voltage 4.2V due to the voltage drop 0.7V at diode while Fig. 8 shows same in .csv format. In the Fig. 7 green coloured signal is input while blue coloured signal is output. LTspice allows the user to look at the waveforms of different current and voltages. Fig. 9 shows its netlist format of the circuit. It follows the pattern of SPICE netlist file. The netlist file format is quite simple and easy to understand.

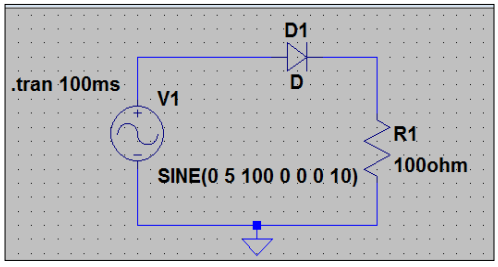

Fig. 6 Transient simulation of half wave rectifier using LTspice

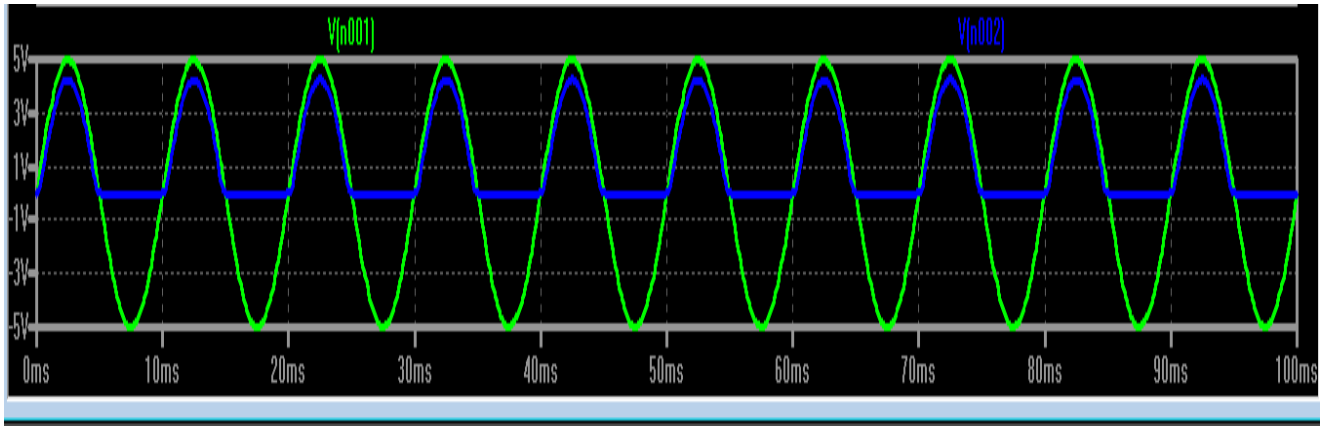


Fig. 7 Transient simulation of circuit design using LTspice

half_final.txt

| time | V(n001) | V(n002) |
|---|---|---|
| 0.000000000000000e+000 | 0.000000e+000 | 0.000000e+000 |
| 9.142857119773651e-006 | 2.872561e-002 | -5.662842e-008 |
| 1.828571423954730e-005 | 5.744555e-002 | -5.024345e-008 |
| 2.742857135932096e-005 | 8.615984e-002 | 1.915492e-008 |
| 3.657142847909461e-005 | 1.148685e-001 | 1.515667e-007 |
| 4.571428559886826e-005 | 1.435714e-001 | 3.469918e-007 |
| 5.485714271864191e-005 | 1.722687e-001 | 6.054303e-007 |
| 6.399999983841553e-005 | 2.009604e-001 | 9.268823e-007 |
| 1.279999996768311e-004 | 4.014211e-001 | 1.252213e-002 |
| 2.256562496768311e-004 | 7.058824e-001 | 1.124135e-001 |
| 3.233124996768311e-004 | 1.007795e+000 | 3.287423e-001 |
| 4.209687496768311e-004 | 1.305915e+000 | 6.057395e-001 |
| 6.162812496768311e-004 | 1.886306e+000 | 1.167900e+000 |
| 8.115937496768310e-004 | 2.438325e+000 | 1.709901e+000 |
| 1.006906249676831e-003 | 2.953670e+000 | 2.218458e+000 |
| 1.202218749676831e-003 | 3.424588e+000 | 2.684414e+000 |
| 1.397531249676831e-003 | 3.843997e+000 | 3.100082e+000 |
| 1.592843749676832e-003 | 4.205589e+000 | 3.458832e+000 |
| 1.788156249676832e-003 | 4.503926e+000 | 3.755036e+000 |
| 1.983468749676832e-003 | 4.734519e+000 | 3.984094e+000 |
| 2.178781249676832e-003 | 4.893900e+000 | 4.142465e+000 |
| 2.374093749676832e-003 | 4.979672e+000 | 4.227709e+000 |
| 2.569406249676832e-003 | 4.990546e+000 | 4.238516e+000 |
| 2.764718749676833e-003 | 4.926357e+000 | 4.174721e+000 |
| 2.960031249676833e-003 | 4.788072e+000 | 4.037302e+000 |
| 3.155343749676833e-003 | 4.577768e+000 | 3.828377e+000 |
| 3.350656249676833e-003 | 4.298612e+000 | 3.551170e+000 |
| 3.545968749676833e-003 | 3.954800e+000 | 3.209980e+000 |
| 3.741281249676833e-003 | 3.551504e+000 | 2.810141e+000 |
| 3.936593749676833e-003 | 3.094790e+000 | 2.357992e+000 |

Fig. 8 .txt file of simulated data of half wave circuit design using LTspice

SPICE Netlist: C:\Users\poonam\Desktop\phd assignments\phd paper\...

```
* C:\Users\poonam\Desktop\phd assignments\phd paper\half.asc
D1 N001 N002 D
R1 N002 0 100
V1 N001 0 SINE(0 5 100 0 0 0 10)
.model D D
.lib C:\Program Files (x86)\LTC\LTspiceIV\lib\cmp\standard.dio
.tran 100ms
.backanno
.end
```

Fig. 9 Netlist file of half wave circuit design

*C. eSim (OSCAD)*

eSim [7] is an open source EDA tool for circuit design, simulation, analysis and PCB design, developed by FOSSEE team under MHRD based at IIT Bombay. eSim is also known as OSCAD (Open Source Computer Aided Design). eSim tool is created using three open source softwares. Kicad, Ngspice and Scilab. Kicad [3] is used to design circuit, Ngspice [5] is used to simulate circuit and Scilab is used to show output design. Ngspice circuit simulator is based on Spice3f5, Ciderlb1 and Xspice. Fig. 10 shows half wave rectifier using eSim. We have used diode, register and AC voltage source. Configuration of components as given in the first circuit except load register. Register value has taken 1K. Labels "IN" and "OUT" are used for the input and output sides of the circuit. Fig. 11 shows transient simulation of half wave rectifier using eSim. It shows peak output voltage 4.3 V due to the voltage drop 0.7V at diode while Fig. 12 shows same in .txt format. Fig. 13 shows the netlist file format. eSim netlist file format follows SPICE standard. It is open source. Unique feature of eSim is to give a circuit equations for each simulation step.

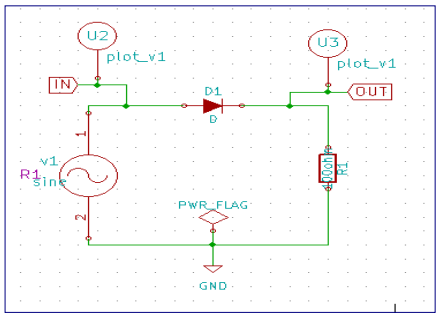

Fig. 10 Half wave rectifier schematic design using eSim

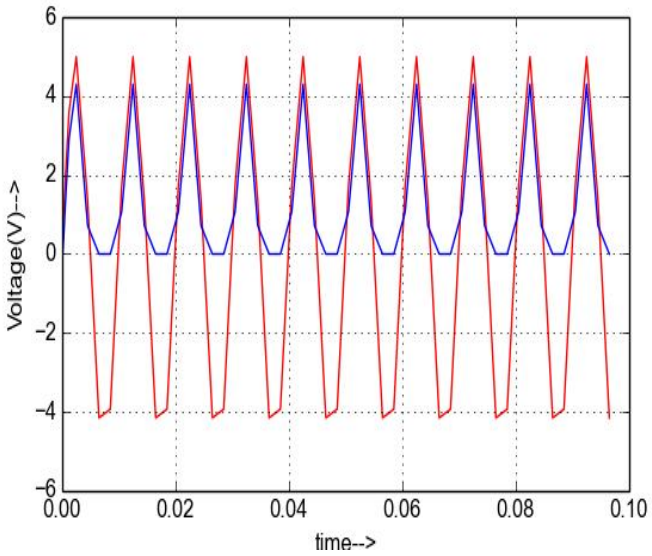


Fig. 11 Transient simulation of half wave rectifier using eSim

* /home/fossee/updatedexamples/halfwave_rectifier/halfwave_rectifier.cir
Transient Analysis Wed Mar 6 21:09:43 2019

| Index | time | in | out |
|---|---|---|---|
| 0 | 0.000000e+00 | 0.000000e+00 | -8.62853e-28 |
| 1 | 1.000000e-05 | 3.141572e-02 | 4.356214e-11 |
| 2 | 2.000000e-05 | 6.283020e-02 | 1.663322e-10 |
| 3 | 4.000000e-05 | 1.256505e-01 | 1.403427e-09 |
| 4 | 8.000000e-05 | 2.512216e-01 | 1.655683e-07 |
| 5 | 1.600000e-04 | 5.018086e-01 | 2.428117e-03 |
| 6 | 3.200000e-04 | 9.985499e-01 | 3.692175e-01 |
| 7 | 6.400000e-04 | 1.956868e+00 | 1.295028e+00 |
| 8 | 1.280000e-03 | 3.601545e+00 | 2.917719e+00 |
| 9 | 2.560000e-03 | 4.996447e+00 | 4.299656e+00 |
| 10 | 4.560000e-03 | 1.364760e+00 | 7.181923e-01 |
| 11 | 6.560000e-03 | -4.15298e+00 | -4.16298e-09 |
| 12 | 8.560000e-03 | -3.93144e+00 | -3.94144e-09 |
| 13 | 1.056000e-02 | 1.723215e+00 | 1.066075e+00 |
| 14 | 1.256000e-02 | 4.996447e+00 | 4.301902e+00 |
| 15 | 1.456000e-02 | 1.364760e+00 | 7.178597e-01 |
| 16 | 1.656000e-02 | -4.15298e+00 | -4.16298e-09 |
| 17 | 1.856000e-02 | -3.93144e+00 | -3.94144e-09 |
| 18 | 2.056000e-02 | 1.723215e+00 | 1.066075e+00 |
| 19 | 2.256000e-02 | 4.996447e+00 | 4.301902e+00 |
| 20 | 2.456000e-02 | 1.364760e+00 | 7.178597e-01 |

Fig. 12 .txt file of simulated data of half wave circuit using eSim

Halfwave_Rectifier.cir

```
* EESchema Netlist Version 1.1 (Spice format) creation date: Wednesday 06 March
2019 09:22:13 PM IST

* To exclude a component from the Spice Netlist add [Spice_Netlist_Enabled] user
FIELD set to: N
* To reorder the component spice node sequence add [Spice_Node_Sequence] user
FIELD and define sequence: 2,1,0

*Sheet Name:/
D1  IN OUT D
R1  OUT GND 100ohm
v1  IN GND sine
XU2  IN plot_v1
XU3  OUT plot_v1

.end
```

Fig. 13 Netlist file of half wave circuit design using eSim

## IV. COMPARISON OF EDA TOOLS

In this section, we present a comparison of an EDA Tools. We have done this comparison on the basis of various features discussed in each EDA tools in the above section. The comparison is based on general components, open source or proprietary platform support, analysis types and working of simulation engine.

TABLE I
COMPARISON OF EDA TOOLS

| Types of Components | QUCS | LTspice IV | eSim(OSCAD) |
|---|---|---|---|
| Passive Components (Register, Capacitor, Inductors, etc.) | Yes | Yes | Yes |
| Active Components (Diodes, Transistors, ICs) | Yes | Yes | Yes |
| Sources (Current and Volatge) | Yes | Yes | Yes |
| Digital Components | | | |
| AND, OR, XOR, NOT Gates | Yes | Yes | Yes |
| NAND, NOR, XNOR Gates | Yes | No | Yes |
| SR and D Flipflops | Yes | Yes | Yes |
| JK, T Flipflops | Yes | No | Yes |
| VHDL Files | Yes | No | No |
| Verilog Files | Yes | No | No |
| Analysis Types | | | |
| Transient | Yes | Yes | Yes |
| AC | Yes | Yes | Yes |
| DC | Yes | Yes | Yes |
| Digital | Yes (FreeHDL Packege Required) | Yes (not used for complex) | Yes |
| Harmonic balance | Yes | No | No |
| S-Parameter | Yes | Yes | No |
| Parameter Sweep | Yes | No | No |
| Noise | Yes | Yes | No |
| Optimization | Yes | No | No |
| Subcircuit Simulation | Yes | Yes | Yes |
| Others | | | |
| Runs on Windows? | Yes | Yes | No |
| Open Source tool | Yes | No | Yes |
| Other Platforms? | Linux, Solaris, Mac | For linux Wine required | Linux |
| Spice Netlist Format | No QUCS Netlist Format | Yes | Yes |
| PCB Creation | No | No | Yes |
| Web App | No | No | Yes |
| Circuit Equations for each simulation step | No | No | Yes |
| Check ERC | No | No | Yes |
| BOM (Bills of Materials) | No | Yes | Yes |
| Simulated data can be exported | Yes | Yes | Yes |

After comparing the tool we have following observations. QUCS and SPICE differ significantly in their representation of circuit netlist file formats. QUCS does not generate standard SPICE netlist file as an output. The QUCS netlist files generated are difficult to understand and cannot be directly simulated on other simulators. Further it cannot be used design PCB also. It also does not provide web view. Hence it is not integrated directly to web view. Additionally for performing digital simulation third party HDL packages are required. Erroneous connections cannot be directly identified by using ERC check rule.

LT spice is used more for analog circuit designs. It has very few digital components hence it is not used for complex circuit design. Also it cannot be extended by researchers as source code is not available although usage is free. It has a constraint of platform as it is majorly used as window operating system.

eSim supports few types of analysis like AC, DC and Transient. Hence exhaustive circuit analysis cannot be done. It supports webapp hence it can be integrated into a website for creation of a virtual lab.

## V. CONCLUSIONS

We have compared EDA tools using different parameters and a result is available in table 1. All the tools analyzed have proper GUI which can be easily understood and used by students as well as faculties for designing and testing analog circuits. From this paper we can conclude that it is a good option to use simulation techniques for the purpose of designing and testing new analog circuits. There is a still scope of new EDA tool that can perform more analysis as compared to the existing once.

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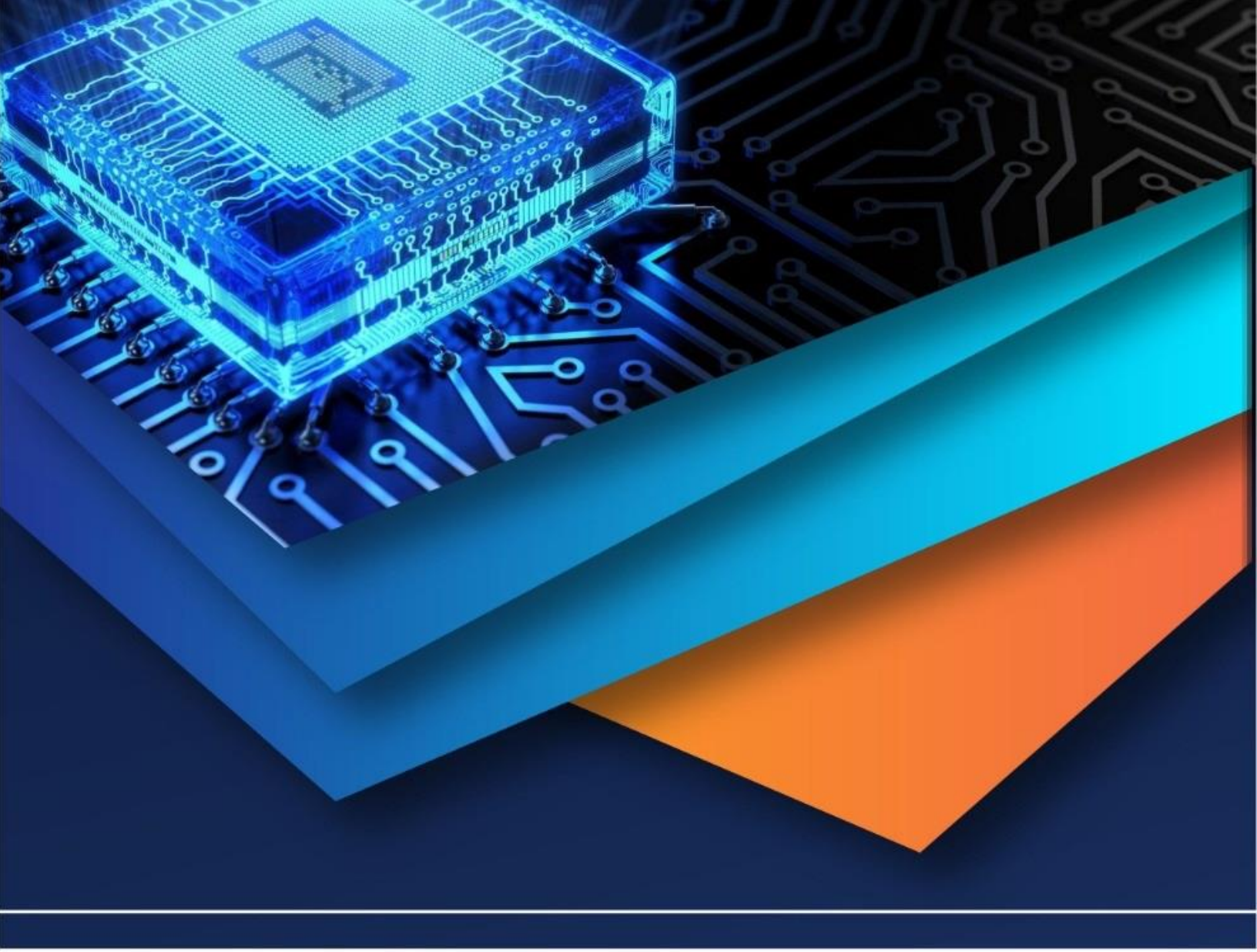

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