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Power Factor Improvement in ZETA Converter for BLDC Motor

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Abstract: ***In the recent years, usage of variable speed driving systems has been increasing in various applications like automobile industries, domestic applications etc., It leads to the development of permanent magnet brushless DC motor (PMBLDCM). For this motor diode bridge rectifier is generally used for AC to DC conversion to meet the demand of electrical machinery with the goal of providing continuous, harmonic less source of energy. In a conventional scheme of diode bridge rectifier with high value of dc-link capacitor fed BLDC motor drive, a high amount of harmonic current is drawn at AC mains. This combination draws peak current and leads to a very highly distorted supply current and very low power factor at AC mains. So, there is a need for improved power factor converters which are less expensive and reliable. For this purpose, ZETA converter is used. The speed of BLDC motor is controlled by varying dc-link voltage of the voltage source inverter (VSI) feeding BLDC motor. The ZETA converter is designed to operate in discontinuous inductor current mode. Thus, utilizing a voltage follower approach which requires a single voltage sensor for DC link voltage control and power factor correction operation. There by ZETA converter acts as inherent power factor corrector. The main objective of this paper is to improve the power factor and decrease harmonics at the input side, which is simulated using MATLAB/SIMULINK platform.***

Keywords: ZETA Converter, BLDC motor, Voltage Source Inverter (VSI), Diode Bridge Rectifier (DBR), Power factor improvement.

I. INTRODUCTION

Brushless DC (BLDC) motor is an ideal motor for low and medium power applications because of its high efficiency, high energy density, high torque/inertia ratio, low maintenance requirement and a wide range of speed control. It is a three-phase synchronous motor with three phase windings on the stator and permanent magnets on the rotor. It is also known as electronically commutated motor as there are no mechanical brushes and commutator assembly, rather an electronic commutation based on rotor position sensed by Hall-Effect position sensor is used. It finds applications in a wide range of household appliances, industrial tools, heating, ventilation and air conditioning and many others [1-6].

The requirement of improved power quality at ac mains is becoming essential and increasingly important. A limit on the allowable harmonic current drawn from ac mains is imposed by international power quality standards such as IEC 61000-3-2 which in-turn limits the total harmonic distortion (THD) of supply current and power factor (PF) at ac mains [7]. Hence, this recommends the use of improved power quality converters for achieving a unity PF (UPF) at ac mains with limited amount of harmonic distortion in the supply current [8-9].

In a conventional scheme of diode bridge rectifier (DBR) with high value of dc-link capacitor fed BLDC motor drive, a high amount of harmonics current is drawn at ac mains. This combination draws peaky current and leads to a very highly distorted supply current and very low PF at ac mains [10]. Fig. 1 shows the conventional DBR fed BLDC motor drive. A very high THD of supply current, that is, 65.9% and a very low PF, that is, 0.44 is achieved at ac mains, which is not under the acceptable limits of IEC-61000-3-2 [7].

Many single-phase power factor correction (PFC) converters are reported in the literature for feeding the BLDC motor drive [11-14]. Two-stage PFC converters have been in wide practice which use two different converters for PFC and dc-link voltage control. Generally, a boost converter is used of first stage for PFC followed by a second stage which depends on the type of application and voltage level required for that particular application [13, 14]. It requires higher number of components and thus has higher losses associated with it.

Moreover, two different controllers for PFC and dc–dc conversion stage are required, which increase the system cost and complexity. Single-stage PFC converters, as the name suggests, require a single converter for performing both tasks of voltage control as well as PFC operation.

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A. Conventional Diode Bridge Rectifier fed BLDC motor drive

The most conventional scheme of feeding the BLDC motor is by using a PFC boost converter [13, 14]. A constant dc-link voltage is maintained at the dc-link capacitor of the voltage source inverter (VSI) feeding the BLDC motor. The speed control is achieved by using the pulse width modulation (PWM)-based switching of VSI, which has high switching losses corresponding to the PWM switching frequency. This allows the operation of VSI in fundamental frequency switching for achieving an electronic commutation of BLDC motor. However, this scheme utilizes a higher number of sensors for controlling the stator current of the BLDC motor. Hence, this type of scheme finds application in higher end drives for precise speed control and is not suitable for low power, low cost household type appliances.

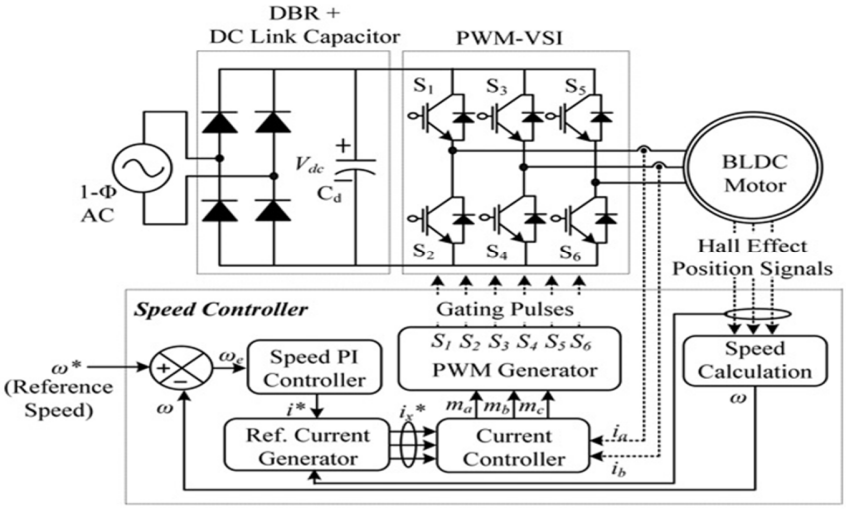

Fig.1 Conventional Diode Bridge Rectifier fed BLDC motor drive

Moreover, sensor reduction in a PFC-based BLDC motor drive is required for reducing the cost of complete drive. The PFC converter can be designed to operate in continuous inductor current mode (CICM) or discontinuous inductor current mode (DICM) operation. The PFC converter operating in CICM using a current multiplier approach requires sensing of dc-link voltage (V_{dc}), supply voltage (v_s) and input current (i_{in}). An inherent PFC is achieved in PFC converter operating in DICM using a voltage follower approach; and it requires sensing of dc-link voltage (V_{dc}), hence requiring a single voltage sensor.

Proper selection of a PFC converter is required for achieving a wide range of speed control of BLDC motor by varying the dc-link voltage. A widely used boost PFC converter is not suitable for this application because of its limitation of boosting the voltage higher than input voltage. Hence the operation of BLDC motor cannot be performed at lower speeds. A PFC-based zeta converter is used for this application because of its capability of bucking and boosting the voltage and its operation as an excellent PF corrector.

II. CONFIGURATION OF PROPOSED SYSTEM & OPERATION

The configuration of the proposed PFC-based zeta converter feeding a BLDC motor drive shown in Fig.2

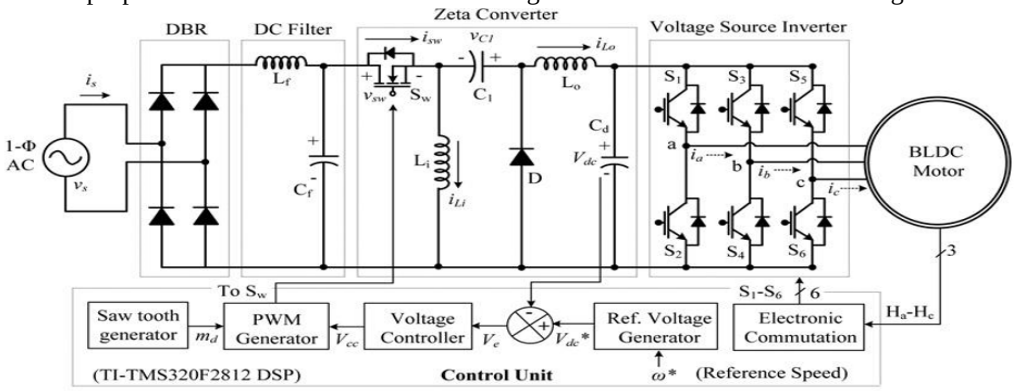

Fig. 2 Proposed PFC zeta converter fed BLDC motor drive

Fig. 3 shows a VSI feeding the BLDC motor drive. The speed of BLDC motor is controlled by varying the dc-link voltage of VSI. The PFC zeta converter is designed to operate in DICM, hence it acts as an inherent PF corrector. The complete operation of BLDC motor drive is realized using a single voltage sensor. An electronic commutation of BLDC motor is utilized for reducing the switching losses. An improved power quality is achieved for a wide range of speed control with power quality indices within the limits of IEC 61000-3-2.

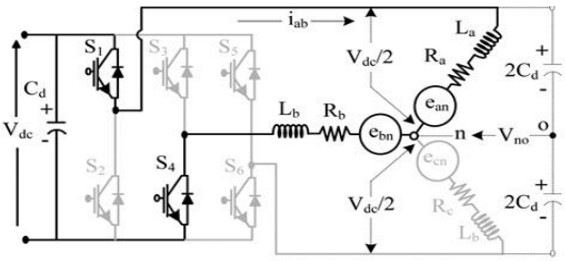

Fig. 3 VSI feeding BLDC motor drive

The PFC zeta converter is designed to operate in DICM, such that the current in input side inductor (I_{Li}) becomes discontinuous, whereas the current in output side inductor (I_{Lo}) and the voltage across intermediate capacitor (V_{c1}) remain in continuous conduction for a complete switching cycle. Figs. 4-6 shows the three different modes of operation of a PFC zeta converter in a complete switching cycle and its associated waveforms are shown in Fig. 7. Three different modes of operation are as follows.

Mode I ($0 < t < t_1$): As shown in Fig. 4, when switch (S_w) is turned on, the input side inductor (L_i) and the output side inductor (L_o) start charging. The intermediate capacitor (C_1) discharges in this mode of operation and charges the dc-link capacitor as shown in Fig. 7. Therefore, the voltage across intermediate capacitor (V_{c1}) decreases and the dc-link voltage (V_{dc}) increases in this mode of operation.

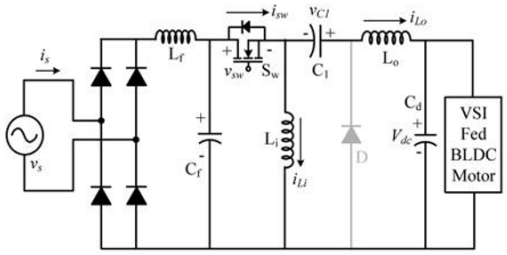

Fig. 4 Mode I operation of Zeta converter in DICM

Mode II ($t_1 < t < t_2$): When the switch (S_w) is turned 'off', the energy stored in the input and the output inductors (L_i and L_o) starts discharging to intermediate capacitor (C_1) and the dc-link capacitor (C_d) as shown in Fig. 5. The diode (D) starts conducting in this mode of operation. Hence, the voltage across the intermediate capacitor (V_{c1}) and dc-link voltage increases in this mode of operation as shown in Fig. 7.

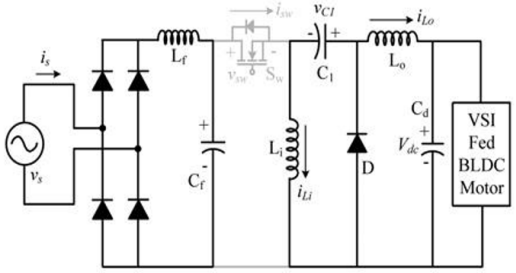

Fig. 5 Mode II operation of Zeta converter in DICM

Mode III ($t_2 < t < t_3$): This is the discontinuous conduction mode of operation, that is, the current in input inductor (I_{Li}) reaches zero and becomes negative as shown in Fig. 6.

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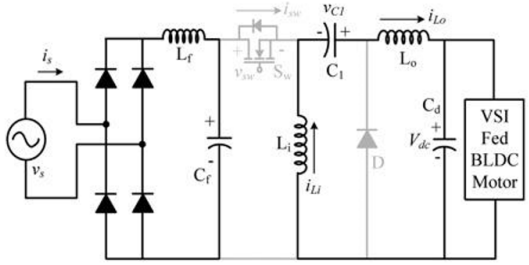

Fig. 6 Mode III operation of Zeta converter in DICM

The dc-link capacitor supplies the required energy to the VSI feeding BLDC motor; hence the dc-link voltage (V_{dc}) starts decreasing in this mode of operation as shown in Fig. 7.

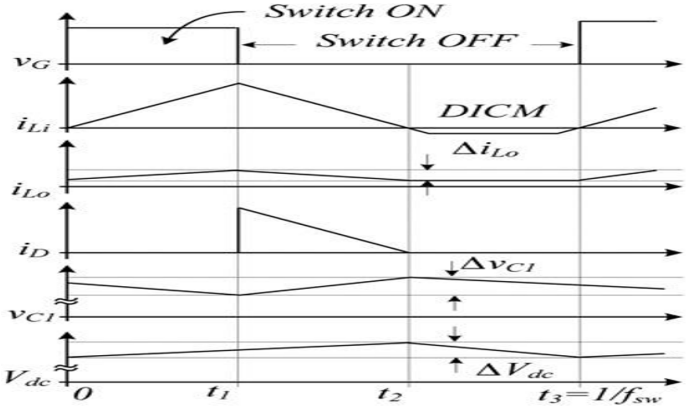

Fig. 7 Waveforms of Zeta converter in DICM

III. DESIGN OF THE PROPOSED SYSTEM

The PFC zeta converter is designed to operate in DICM such that the current flowing in input inductor (L_i) becomes discontinuous in a switching period. A front-end converter of 300 W is designed to feed a BLDC motor of 251 W. Therefore, for a wide variation of speed, the dc-link voltage has to be controlled from a very low value ($V_{dcmin} = 50V$) to rated value ($V_{dcmax} = 200V$) of dc-link voltage.

The input voltage, V_s applied to the PFC converter as

$$V_s(t) = V_m \sin(2\pi f_L t)\, V$$

where V_m is the peak input voltage (i.e. $\sqrt{2}V_s$ where V_s is the supply root mean square voltage), f_L is the line frequency, that is, 50 Hz.

Now, the voltage appearing after the DBR is given as

$$V_{in}(t) = |V_m \sin(2\pi f_L t)\, V$$

The output voltage, V_{dc}, of zeta converter which is a buck-boost configuration is given as

$$V_{dc} = \frac{D}{1-D} V_{in}$$

Where D represents the duty ratio.

The duty ratio, D is calculated by substituting the expression of V_{in} from above equation as

$$D = \frac{V_{dc}}{V_{dc} + V_{in}}$$

Moreover, the speed of the BLDC motor is controlled by varying the dc-link voltage of the VSI, hence the instantaneous power, P_i at any dc-link voltage (V_{dc}) can be taken as linear function of V_{dc} as

$$P_i = \left(\frac{P_{max}}{V_{dcmax}}\right) V_{dc}$$

where V_{dcmax} represents maximum value of dc-link voltage.

A. Design of Input Inductor (L_i)

The critical value of input inductor (L_{ic}) is expressed as

$$L_{ic} = \frac{V_{in}}{2I_{in}f_s} = \frac{R_{in}D}{2f_s} = \left(\frac{V_s^2}{P_i}\right)\frac{D}{2f_s} = \left(\frac{V_s^2}{2P_i f_s}\right)\frac{V_{dc}}{V_{dc}+V_{in}}$$

Where R_{in} is the input side resistance and f_s is the switching frequency which is taken as 20 kHz.

This expression exhibits a minimum value at the lowest possible value of supply voltage for which the converter is designed (V_{smin}) which is taken as 170 V. Hence the critical inductance for the two dc-link voltages (i.e. 200 and 50 V) at peak of supply voltage $\sqrt{2}V_s$ can be found as

$$L_{ic200} = \frac{V_{smin}^2}{2P_{max}f_s}\left(\frac{V_{dcmax}}{V_{dcmax}+\sqrt{2}V_{smin}}\right)$$
$$= \frac{170^2}{2\times300\times20000}\left(\frac{200}{200+170\sqrt{2}}\right) = 1.093 \text{ mH}$$
$$L_{ic40} = \frac{V_{smin}^2}{2P_{max}f_s}\left(\frac{V_{dcmax}}{V_{dcmax}+\sqrt{2}V_{smin}}\right)$$
$$= \frac{170^2}{2\times75\times20000}\left(\frac{50}{50+170\sqrt{2}}\right) = 1.658 \text{ mH}$$

Therefore, to achieve a discontinuous conduction at the worst-case scenario of maximum dc-link voltage ($i.e.\ L_{ic200}$)the value of input inductor L_i, must be selected lower than L_{ic200}

$$L_i < L_{ic200} \Rightarrow L_i < 1.093 \text{ mH}$$

Hence the value of L_i is selected as 100 µH to achieve a guaranteed discontinuous conduction.

B. Design of Intermediate Capacitor (C_1)

The critical value of intermediate capacitance C_1 is designed for a permitted ripple voltage as

$$C_{1c} = \frac{V_{dc}D}{\Delta V_{c1}f_s R_L} = \frac{V_{dc}D}{\eta V_{c1}f_s R_L}$$

where V_{c1} is the voltage appearing across capacitor, C_1. Hence, by substituting the expressions of intermediate capacitor voltage, $V_{c1} = (V_{dc} + V_{in})$, and emulated load resistance, $R_L = V^2_{dc}/P_i$ in above equation, obtained as

$$C_{1c} = \frac{P_i}{\eta(V_{dc}+V_{in})^2 f_s}$$

The maximum value of ripple voltage across intermediate capacitor occurs at maximum value of dc-link voltage and supply voltage since $V_{c1} = (V_{dc} + V_{in})$. Hence the maximum voltage for which the converter is designed is 270 V (V_{smax}), so peak voltage is $V_{in} = 270\sqrt{2}V$. Therefore, the intermediate capacitor is calculated as

$$C_{1c} = \frac{P_{max}}{\eta(\sqrt{2}V_{smax}+V_{dcmax})^2 f_s}$$
$$= \frac{300}{0.1\times(270\sqrt{2}+200)^2\times20000} = 443.08 \text{ nF}$$

Where η is taken as10% of V_{c1}.

Hence the intermediate capacitor of 440 nF is selected for the application.

C. Design of Output Inductor(L_o)

The critical output side inductor is designed as

$$L_o = \frac{V_{dc}(1-D)}{f_s\Delta I_{Lo}} = \frac{V_{dc}(1-D)}{f_s(\lambda I_{Lo})} = \frac{V_{dc}D}{f_s(\lambda I_{in})}$$

The above equation is rearranged as

$$L_o = \frac{V_{dc}D}{f_s\lambda I_{in}} = \frac{R_{in}V_{dc}D}{f_s\lambda V_{in}} = \left(\frac{V_s^2}{P_i}\right)\frac{V_{dc}D}{f_s\lambda V_{in}}$$

The maximum current ripple in an inductor occurs at the maximum power and for minimum value of supply voltage (i.e. $V_{smin} = 170\,V$). Hence the output inductor is calculated at the peak of supply voltage ($V_{in} = \sqrt{2}\,V_{smin}$) as

$$L_o = \left(\frac{V_{smin}^2}{P_{max}}\right)\frac{V_{dcmax}}{\lambda f_s\left(\sqrt{2}V_{smin}\right)}\left(\frac{V_{dcmax}}{V_{dcmax}+\left(\sqrt{2}V_{smin}\right)}\right)$$
$$= \frac{170^2}{300} \times \frac{200}{0.5\times 20000\times(170\sqrt{2})} \times \frac{200}{200+(170\sqrt{2})} = 3.64 \text{ mH}$$

Where λ is the ripple current which is taken as 50% of I_{Lo}. Hence L_o of 3.5 mH is selected for the application.

D. Design of DC-Link Capacitor (C_d)

The value of dc-link capacitor is expressed as

$$C_d = \frac{I_{dc}}{2\omega\Delta V_{dc}} = \frac{P_i}{2\omega k V_{dc}^2}$$

where$k$ represents the permitted ripple in dc-link voltage.

The maximum value of dc-link capacitor is achieved at minimum value of dc-link voltage with κ taken as 2% of V_{dcmin} and is calculated as

$$C_d = \frac{P_{min}}{2\omega k V_{dcmin}^2} = \frac{75}{2\times 314\times 0.02\times 50^2} = 2388\ \mu F$$

Hence the dc-link capacitor is selected as 2200 μF.

E. Design of DC Filter (L_f&C_f)

Moreover, a low-pass LC filter is used to avoid the reflection of higher-order harmonics in supply system. The maximum value of filter capacitance is given as

$$C_{max} = \frac{I_m}{\omega_L V_m}\tan(\theta) = \frac{(P_o\sqrt{2}/V_s)}{\omega_L V_m}\tan(\theta)$$
$$= \frac{(300\sqrt{2}/220)}{314\times 220\sqrt{2}}\tan(1°) = 344.7 \text{ nF}$$

Where I_m and V_m are the peak of input voltage and current.

Hence a value of filter capacitor, C_f is taken as 330 nF. Now, the value of filter inductor is designed by considering source impedance (L_s) of 3.5% of the base impedance. The additional value of inductance required is given as

$$L_f = L_{req} + L_s \Rightarrow \frac{1}{4\pi^2 f_c^2 C_f} = L_{req} + 0.035\left(\frac{1}{\omega_L}\right)\frac{V_s^2}{P_i}$$
$$L_{req} = \frac{1}{4\pi^2\times 2000^2\times 330\times 10^{-9}} - 0.035\left(\frac{1}{314}\right)\left(\frac{220^2}{300}\right) = 1.21 \text{ mH}$$

where f_c is the cut-off frequency and is selected such that $f_L < f_c < f_s$, hence it is taken as $f_s/10$.

Hence a LC filter with inductance L_f and capacitance C_f is selected as 1.21 mH and 330 nF, respectively.

IV. CONTROL OF THE PROPOSED SYSTEM

The control of the PFC zeta converter fed BLDC motor drive is classified into two parts as follows.

A. Control of Front-End PFC Converter

A voltage follower approach is used for the control of the front-end PFC converter which generates the PWM pulses for the PFC converter switch for dc-link voltage control. A single voltage control loop (voltage follower approach) is utilized for the PFC zeta converter operating in DICM. A reference dc-link voltage (V_{dc}^*)is generated as

$$V_{dc}^* = k_v\omega^*$$

where k_v is the motor's voltage constant and $\omega^*$is the reference speed.

Reference dc-link voltage V_{dc}^* is compared with sensed dc-link voltage (V_{dc}) to generate voltage error signal (V_e) given as

$$V_e(k) = V_{dc}^*(k) - V_{dc}(k)$$

where k represents the kth sampling instant.

This error voltage signal (V_e) is given to the voltage proportional–integral (PI) controller to generate a controlled output voltage as (V_{cc})

$$V_{cc}(k) = V_{cc}(k-1) + k_p\{V_e(k) - V_e(k-1)\} + k_i V_e(k)$$

Where k_p and k_i are PI gains of the voltage PI controller.

Finally, the output of voltage controller is compared with a high frequency saw-tooth signal (m_d) to generate the PWM pulses as

$$\left\{ \begin{array}{l} if\ m_d(t) < V_{cc}(t), \text{then } S_w = 'ON' \\ if\ m_d(t) \geq V_{cc}(t), \text{ then } S_w = 'OFF' \end{array} \right\}$$

Where S_w represents the switching signals to switch of PFC converter.

B. Control of BLDC Motor

An electronic commutation of the BLDC motor includes proper switching of VSI in such a way that a symmetrical dc current is drawn from the dc-link capacitor for 120° and placed at the center of each phase. Hall-Effect position sensors are used for rotor position sensing on a span of 120°. As shown in Fig. 4.2, a line current i_{ab} is drawn from the dc-link capacitor during the conduction of two switches (S_1 and S_4). The magnitude of this current depends on the applied dc-link voltage (V_{dc}), back electromotive forces (EMFs) ($e_{an}$and e_{bn}), resistance (R_a and R_b) and self and mutual inductance (L_a, L_b and M) of the stator windings. Table 1 shows the governing of different switching states of the VSI feeding a BLDC motor based on the Hall-Effect position signals ($H_a - H_c$).

θ, deg	Hall Signals			Switching States					
	H_3	H_2	H_1	S_1	S_2	S_3	S_4	S_5	S_6
NA	0	0	0	0	0	0	0	0	0
0-60	1	0	1	1	0	0	1	0	0
60-120	0	0	1	1	0	0	0	0	1
120-180	0	1	1	0	0	1	0	0	1
180-240	0	1	0	0	1	1	0	0	0
240-300	1	1	0	0	1	0	0	1	0
300-360	1	0	0	0	0	0	1	1	0
NA	1	1	1	0	0	0	0	0	0

TABLE 1 Switching states for electronic commutation of BLDC motor

V. MATLAB/SIMULATION RESULTS

A. Without Zeta Converter

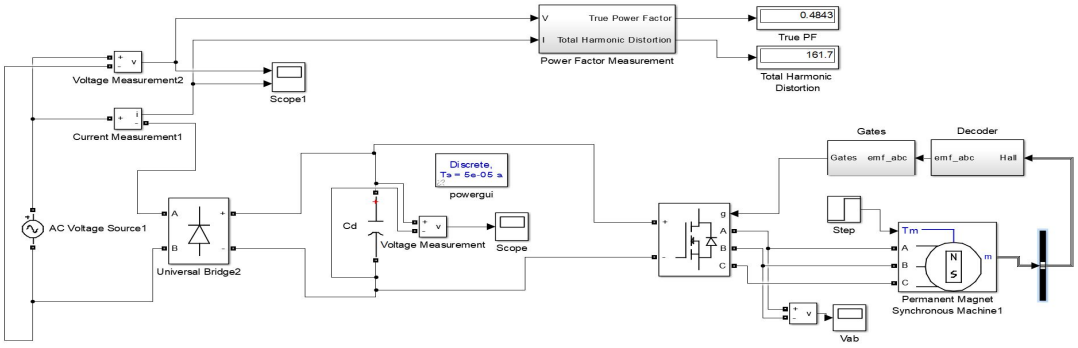

Fig.6.1.1 Conventional Diode Bridge Rectifier fed BLDC motor drive

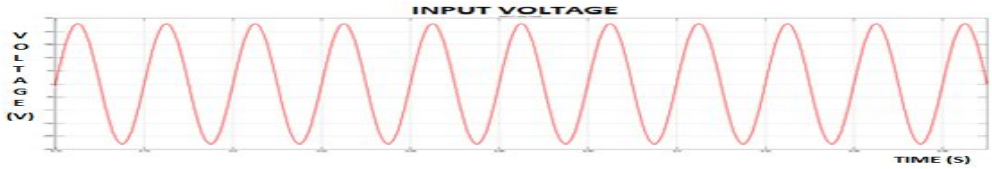

Fig.6.1.2 Input Voltage of Diode Bridge Rectifier

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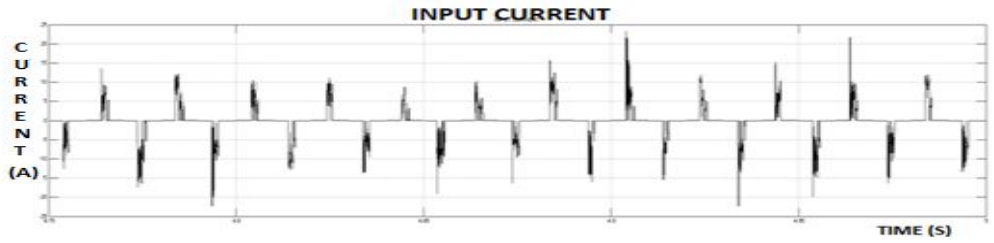

Fig.6.1.3 Input Current of Diode Bridge Rectifier

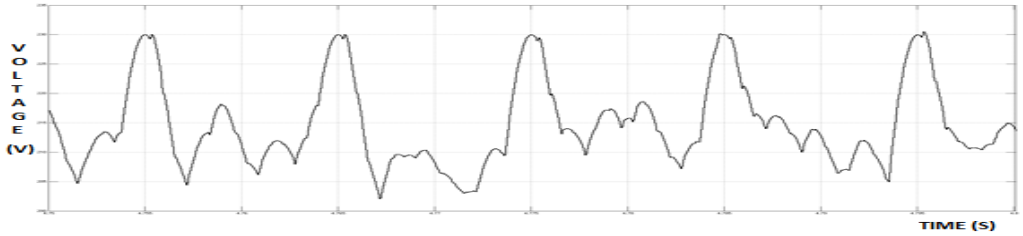

Fig.6.1.4 Rectifier Output Voltage

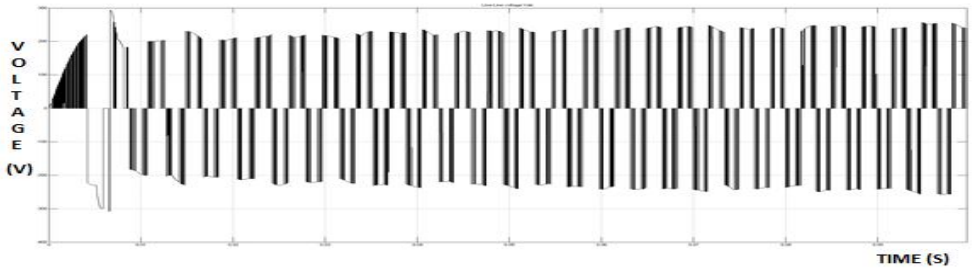

Fig.6.1.5 Inverter Output Voltage

B. With Zeta Converter

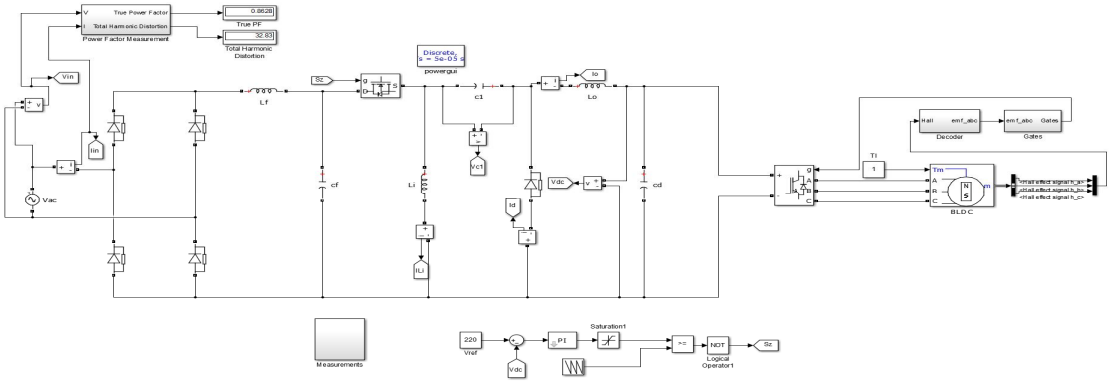

Fig.6.2.1 Proposed PFC zeta converter fed BLDC motor drive

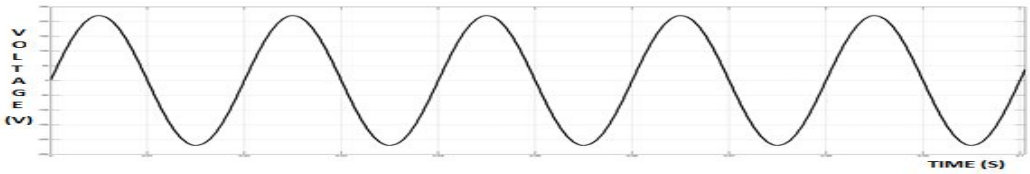

Fig.6.2.2 Input Voltage of Diode Bridge Rectifier

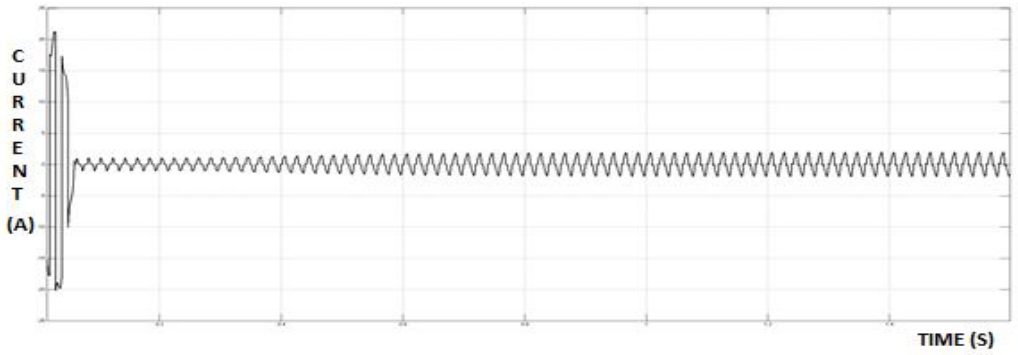

Fig.6.2.3 Input Current of Diode Bridge Rectifier

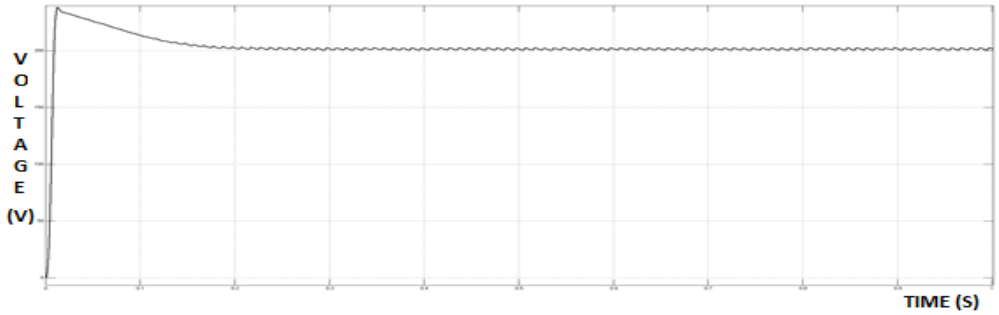

Fig.6.2.4 D.C link Voltage

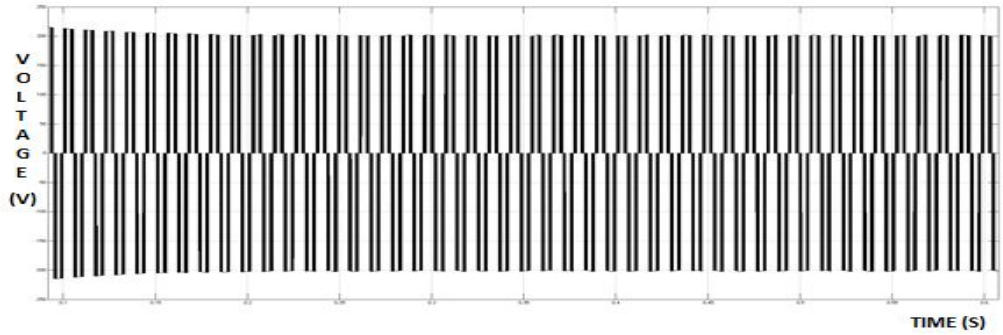

Fig.6.2.5 Inverter Output Voltage

C. Improvement in Power Factor

	Without zeta converter	With zeta converter
Power Factor	0.449	0.887

VI. CONCLUSION

A PFC zeta converter fed BLDC motor drive has been proposed for a wide range of speed control with UPF at ac mains. The speed of BLDC motor has been controlled by varying the dc-link voltage of VSI via the PFC zeta converter. The PFC zeta converter has been designed to operate in DICM, which required a voltage follower for dc-link voltage control. A single voltage sensor has been required for the complete drive, which makes it a cost-effective solution. Moreover, low-frequency switching pulses have been used for electronically commutating the BLDC motor which offers reduced switching losses in the VSI compared with conventional scheme of PWM-based switching of VSI. The proposed drive has been designed for achieving an improved power quality at ac mains for a wide range of speed control.

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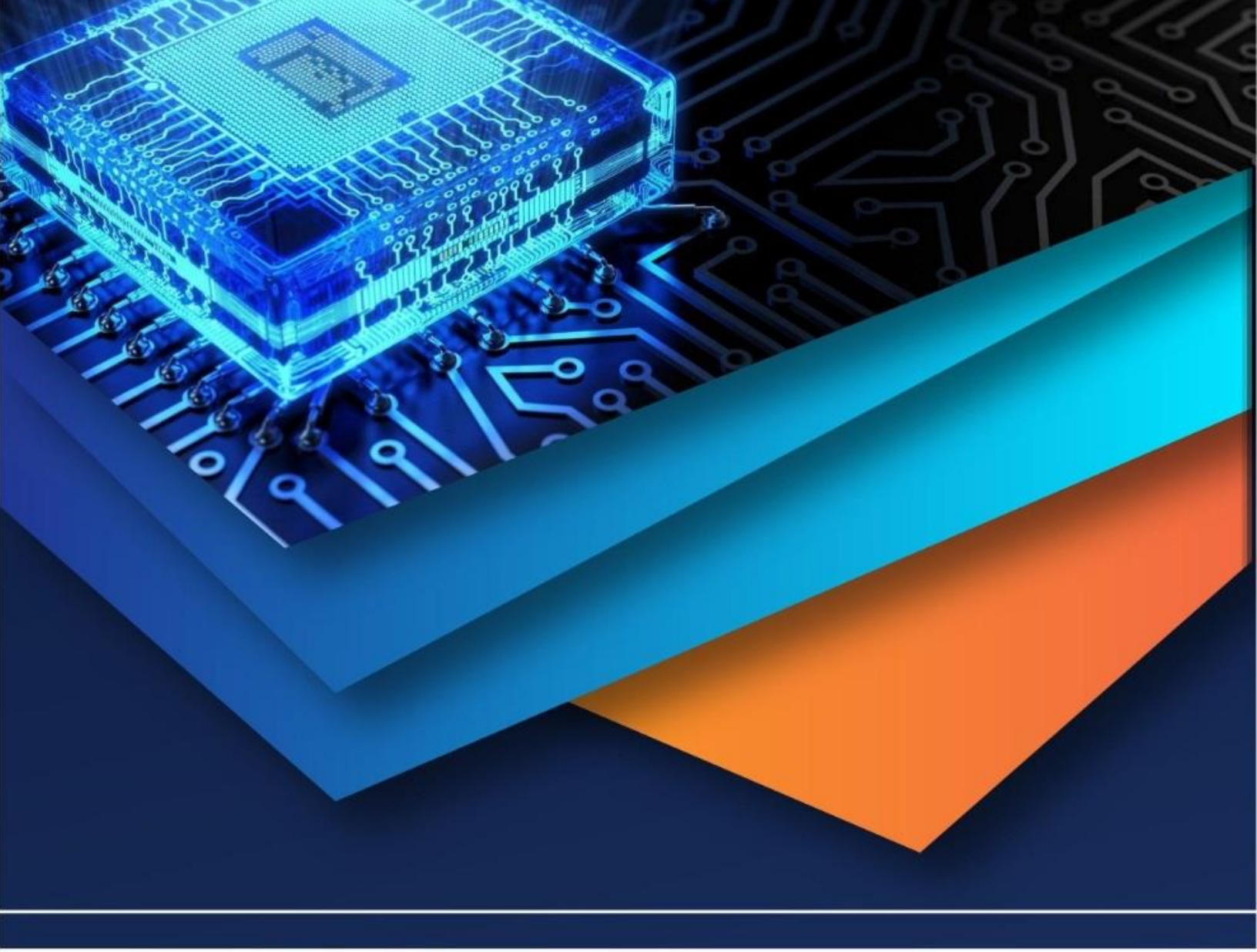

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