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Bridgeless Buck PFC Rectifier with Improved Power Factor

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Abstract: ***A bridgeless buck power factor correction rectifier that substantially improves efficiency at low line of the universal-line range is introduced. By eliminating input bridge diodes, the proposed rectifier's efficiency is further improved. Buck power factor correction (PFC) converters, compared with conventional boost PFC converters, exhibit high efficiency performance in the entire range of universal line voltage. This feature has gotten more attention for eliminating the zero crossing dead angle of buck PFC rectifiers. For this purpose, two auxiliary flyback converters without any active switches are applied to a bridgeless buck rectifier to eliminate the zero crossing dead angle and achieve unity power factor, low total harmonic distortion (THD) and high efficiency.***

Keywords*:* ***Bridgeless rectification, buck converter, power factor correction (PFC), Zero crossing distortion.***

I. INTRODUCTION

The use of power factor correction (PFC) converters as a current shaper in the front stage of ac/dc rectifiers is an effective method to provide high power factor (PF) and low total harmonic distortion (THD) for meeting [1]. On the other hand, high efficiency is a vital requirement of performance. Meeting the requirements of both high PF and efficiency poses a major challenge for ac/dc rectifiers. Boost converters are the most commonly used PFC converters. In universal-line (90–264 V) applications, maintaining a high efficiency across the entire line range poses a major challenge for ac/dc rectifiers that require power factor correction (PFC). For decades, a bridge diode rectifier followed by a boost converter has been the most commonly used PFC circuit because of its simplicity and good PF performance. However, a boost PFC front-end exhibits 1%–3% lower efficiency at 100 V line com- pared to that at 230 V line. This drop of efficiency at low line can be attributed to an increased input current that produces higher losses in semiconductors and input electromagnetic interference filter components. In [21]-[24], for Vin<Vout, an auxiliary flyback converter with an auxiliary switch, diode and inductor is activated to shape the input current reduce the zero crossing dead angle. However, in these topologies, three or four simultaneously conducting semiconductor devices increase the conduction losses. Due to transition from flyback to buck mode at Vin = Vout, the input current can change abruptly and increase the THD.

In [25], the output capacitor of an auxiliary flyback converter is in series with the switch of a conventional buck converter. Thus, the voltage of the flyback output capacitor is added to the rectified line voltage. As a result, the zero crossing dead angle of the input current is omitted. However, three simultaneously conducting active components in the conducting period of the buck switch increase the conduction losses and reduce the efficiency.

At lower power levels, i.e., below 850 W, the drawbacks of the universal-line boost PFC front-end may partly be overcome by implementing the PFC front-end with a buck topology. As it has been demonstrated in [3], the universal-line buck PFC front-end with an output voltage in the 80 V range maintains a high-efficiency across the entire line range. In addition, a lower input voltage to the dc/dc output stage has beneficial effects on its light-load performance because lower voltage- rated semiconductor devices can be used for the dc/dc stage and because lower input voltage reduces the loss and size of the transformer.

In this paper, a bridgeless buck PFC rectifier that further improves the low-line (115 V) efficiency of the buck front-end by reducing the conduction loss through minimization of the number of simultaneously conducting semiconductor components is introduced. Because the proposed bridgeless buck rectifier also works as a voltage doubler, it can be designed to meet harmonic limit specifications with an output voltage that is twice that of a conventional buck PFC rectifier. As a result, the proposed rectifier also shows better hold-up time performance. Although the output voltage is doubled, the switching losses of the primary switches of the downstream dc/dc output stage are still significantly lower than that of the boost PFC counterpart.

In [25], the output capacitor of an auxiliary flyback converter is in series with the switch of a conventional buck converter. Thus, the voltage of the flyback output capacitor is added to the rectified line voltage. As a result, the zero crossing dead angle of the input current is omitted. However, three simultaneously conducting active components in the conducting period of the buck switch

increase the conduction losses and reduce the efficiency. In this paper, a bridgeless unity PF buck rectifier is proposed. Two auxiliary flyback converters are used in a bridgeless buck topology to omit the zero crossing dead angles of the positive and negative half-line cycles. Thus, the proposed rectifier provides both high PF and efficiency. Without any auxiliary switches and only with one auxiliary diode, one low voltage small capacitor and an additional winding on the core of the buck inductor, the dead angle of the input current is omitted and a unity PF is achieved. The operation of the proposed rectifier is verified using a 150 W, 48 V experimental prototype operating in the continuous conduction mode (CCM) using peak-current-mode control method.

II. CONFIGURATION OF PROPOSED SYSTEM

The configuration of the proposed bridgeless buck rectifier is shown in Fig.1. The proposed converter consists of auxiliary fly back converter.

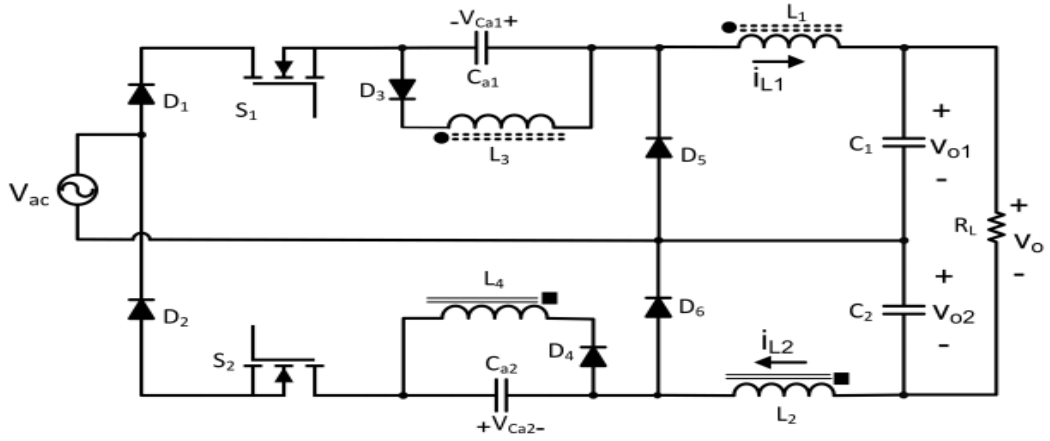


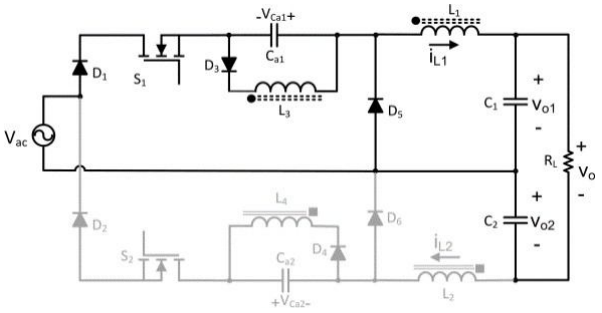
Fig. 1. Proposed bridgeless unity power factor buck rectifier.

III. OPERATION

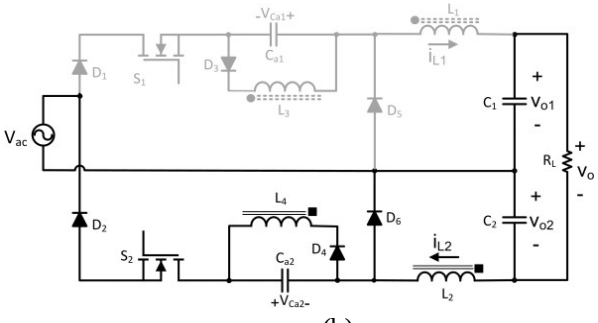
The proposed bridgeless unity PF buck rectifier is shown in Fig. 1, Figs. 2(a) and 2(b) show the operation of the rectifier in the positive and negative half-line cycles, respectively. Due to their similarity, only the positive half- line cycle is described. The buck converter of the positive half-line cycle, consists of a unidirectional switch implemented by diode D1 and switch S1, freewheeling diode D5, filter inductor L1, and output capacitor C1. The auxiliary flyback converter consists of diode D3, small capacitor Ca1 and inductor L3 that is couple with its buck counterpart L1 with a unity turn ratio. The operation of the rectifier is presented using theoretical waveforms (Fig. 3) and the following assumptions.

All of the components are ideal except for the coupled inductors L1,3 and L2,4, where their leakage inductances are included.

The output capacitors C1,2 are large enough to obtain constant output voltages VO1,2 in a switching cycle.



The initial voltage of Ca1 is equal to VO1 (VCa1 (t0) = VO1).(a)



(b)

Fig. 2. Operation of the positive and negative half-line cycles. (a) Positive half-line cycle. (b) Negative half-line cycle.

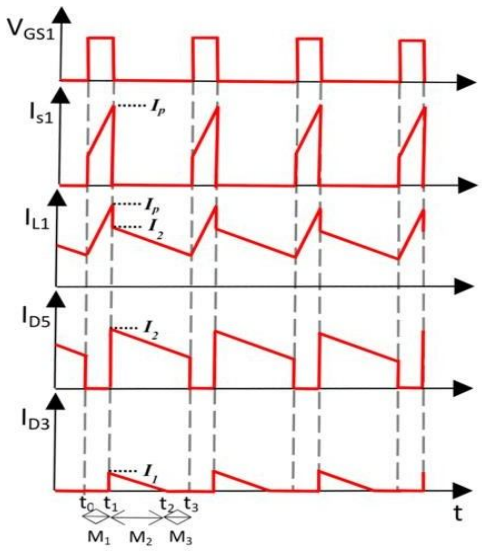


Fig. 3. Theoretical key waveforms.

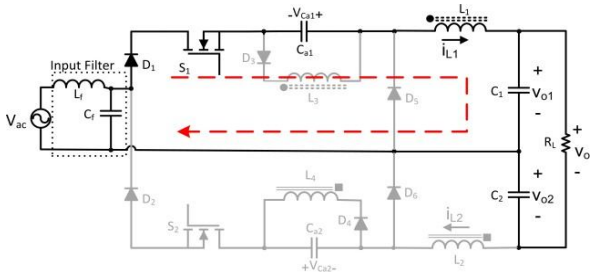
Mode 1 (t0-t1): According to Fig. 4a, by turning the buck switch S1 on, the voltage Vac+VCa1-VO1 is applied to the buck inductor L1 and iL1 increases linearly. The buck inductor current iL1 discharges the capacitor Ca1 and decreases its voltage VCa1 from the initial value VCa1 (t0) =VO1 to VO1 - ΔVCa1. The low voltage ripple of ΔVCa1 is desirable because the line voltage Vac is applied to the inductor L1 and the dead angle of the line current is omitted. The current iL1 is increased with a slope of Vac/L1 . At t = t1 = DT, switch S1 is turned off while iL1 reaches its maximum value Ip (Fig. 3).

Mode 2 (t1-t2): Since VCa1 and VO1 are almost equal, by turning the switch S1 off, the diodes D3 and D5 conduct simultaneously (Fig. 4b). Thus, by turning the switch S1 off, a part of the inductor L1 energy charges the capacitor Ca1 and the other part charges the output capacitior C_1.

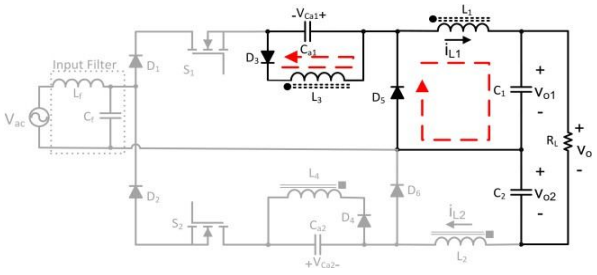
Mode 3 (t2-t3): This mode starts when the capacitor Ca1 is charged up to VO1 and the inductor current iL3 is zero (Fig. 4c). The inductor current iL1 freewheels through D5 and supplies the load power. According to the operating modes, the buck converter shapes the line current for Vac < VO1 and the dead angle of the line current is omitted, which results a unity power factor.

In [3], [4] to provide low THD and high PF, a complex control circuit is applied. In the proposed rectifier, by eliminating the zero crossing dead angle, the conventional peak current control method can be applied. In this method, when the switch current reaches the reference current, the buck switch is turned off.

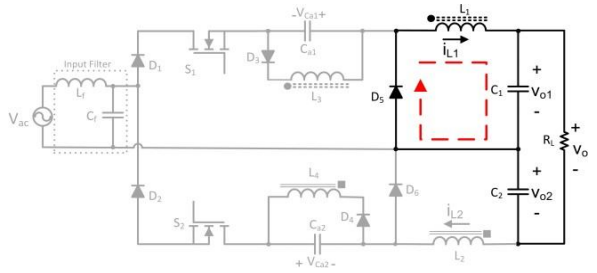
After a switching period, it is turned on again to shape the input current. In the proposed converter, each buck inductor is coupled with its flyback counterpart. Therefore, the series capacitor voltages are equal to their corresponding output voltages, VCa1=VO1 and VCa2=VO2. As a result, in the both half-line cycles, independent of the values of VO1, 2 and L1, 2, the line voltage Vac is applied to L1, 2 and the dead angle of the buck converter is omitted. In addition, in order to achieve similar input current amplitudes for the positive and negative half cycles, due to the applied peak current control method, the values of L1 and L2 should be almost equal. Furthermore, C1 and C2 should be large enough to provide a small ripple and the difference in their values has minor effect in the converter operation.



(a)



(b)



(c)

Fig. 4. Equivalent circuits of the three modes during the positive half-line cycle. (a) Mode 1. (b) Mode 2. (c) Mode 3.

IV. EXPERIMENTAL RESULTS

In the buck PFC rectifiers presented in [2]-[4], due to zero crossing dead angle, there is a strong tradeoff between the PF and THD performance and output voltage level. Since the line current is zero for $V_{in} < V_{out}$, increasing the output voltage deteriorates the PF and THD. On the other hand, decreasing the output voltage increases the current levels of the rectifier and leads to higher conduction losses and lower efficiency. This tradeoff is resolved in the proposed converter by eliminating the zero crossing dead angle. The performance of the proposed rectifier is verified using a 150 W, 48 V prototype circuit with a 110 V_{ac} line voltage. The schematic of the implemented circuit is shown in Fig.5.

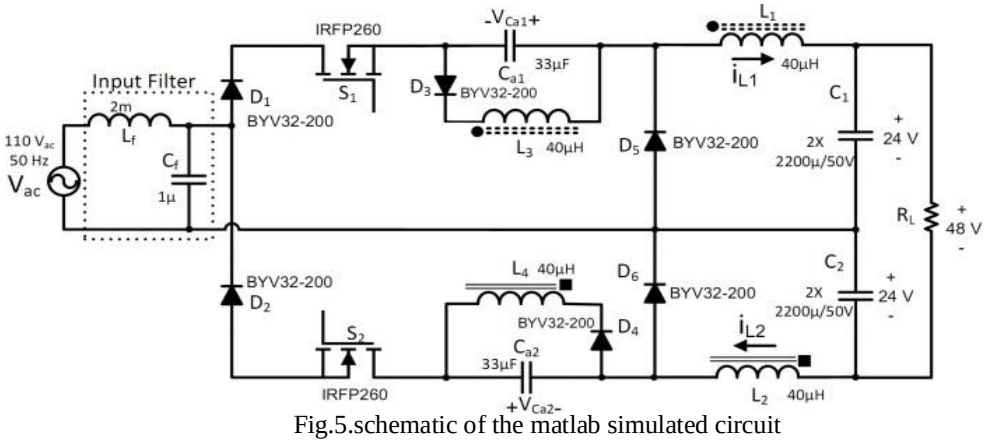


Fig.5.schematic of the matlab simulated circuit

For V_O=48 V, the average values of $V_{O1,\ 2}$ are equal to 24 V (Fig. 6). Based on (1), the minimum duty cycle D_{min} at the peak of the line voltage $V_{ac,max}$=155 V is equal to 0.13. In the design of a regular buck converter, the current ripple of the buck inductor is considered about 20% of its maximum value. Due to the short ON time of the buck switches at the peak of the line voltage (D_{min}=0.13) and restrictions on the response time of the elements of the control circuit, the maximum inductor current ripple $\Delta I_{L,max}$ is considered about 60% of the maximum inductor current I_p. As a result, the current control loop can follow the changes of the inductor current well. Thus, based on (6), for P_o=150 W, the maximum inductor current I_p is equal to 21 A and $\Delta I_{L,max}$ is 12.5 A. Based on (17), for f_s=40 kHz, the buck inductors L=L_1=L_2 are equal to 40 µH. To implement the coupled inductors $L_{1,\ 3}$ and $L_{2,\ 4}$ with a unity turn ratio, two ferrite cores (EE33/29) with 50 turns of wire are used.The measured leakage inductance of the coupled

inductors is about 0.5 µH. Based on (12), the condition of the second mode of operation is that the auxiliary flyback capacitors $C_{a1,\,2}$ should be greater than 10 µF. To ensure the second mode operation, 33 µF electrolyte capacitors are used for $C_{a1,\,2}$ and $\Delta V_{Ca1,2}$=1.5 V is obtained from (4). According to (15) and (16), the currents I_1 and I_2 are equal to 10 and 11 A, respectively (Fig. 3).

A comparison of the PF and THD of the proposed rectifier and Conventional rectifier for a 110 V_{ac} line voltage. It can be seen that the proposed converter with a simple auxiliary flyback converter and without an auxiliary switch has a PF of more than 0.979 and a THD of less than 15%. By eliminating the input bridge diodes, the number of conducting semiconductor elements in the inductor charging path has been reduced from 3 or 4 to 2. This feature decreases the conduction losses. Hence, it increases the efficiency so that the proposed converter shows a high efficiency of around 94%

V. MATLAB/SIMULATION RESULTS

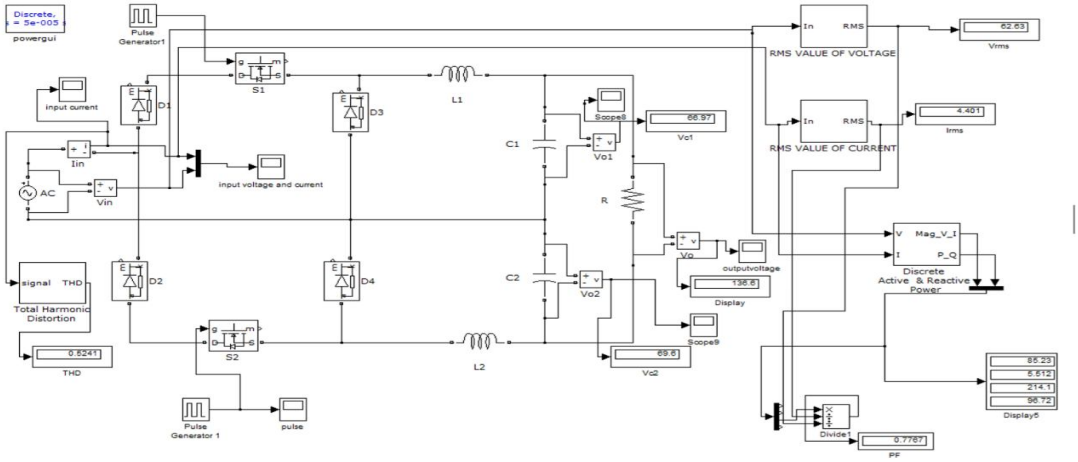


Fig.6.Matlab/Simulink circuit of Conventional Bridgeless Buck PFC Rectifier.

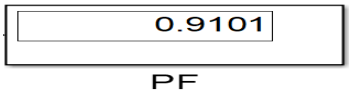


Fig.7.Power factor of Conventional Bridgeless Buck PFC Converter

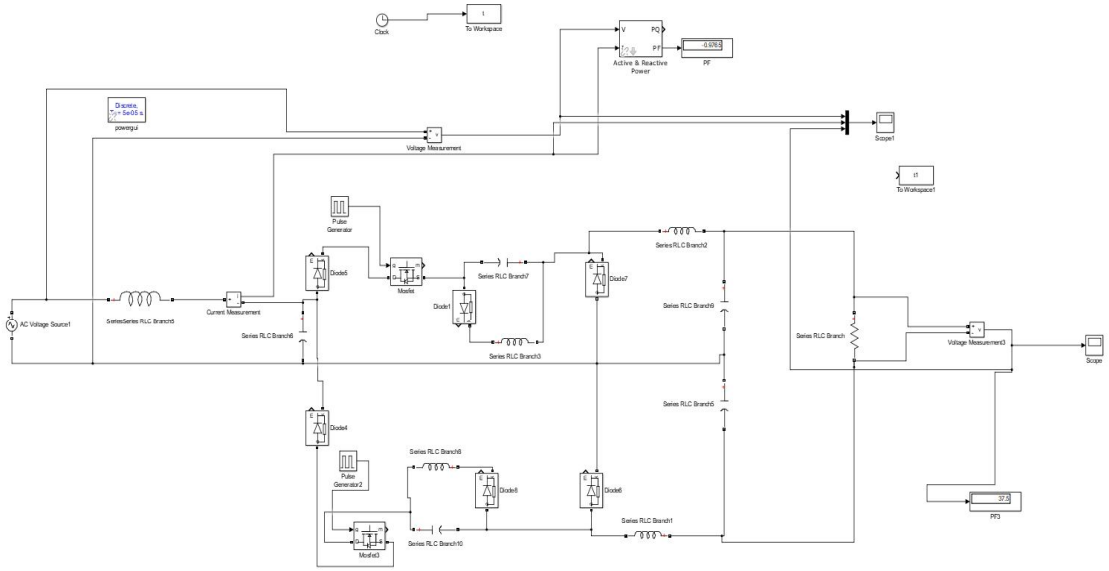


Fig 8 Block diagram of Proposed Bridgeless Buck PFC Rectifier

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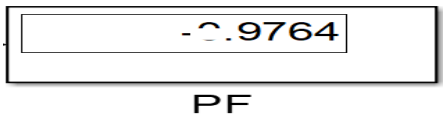

Fig 9 Power factor of Proposed Bridgeless Buck PFC Converter

By comparing two rectifier the power Factor is increased without using any special equipment. The resultant waves forms of proposed rectifier is shown below

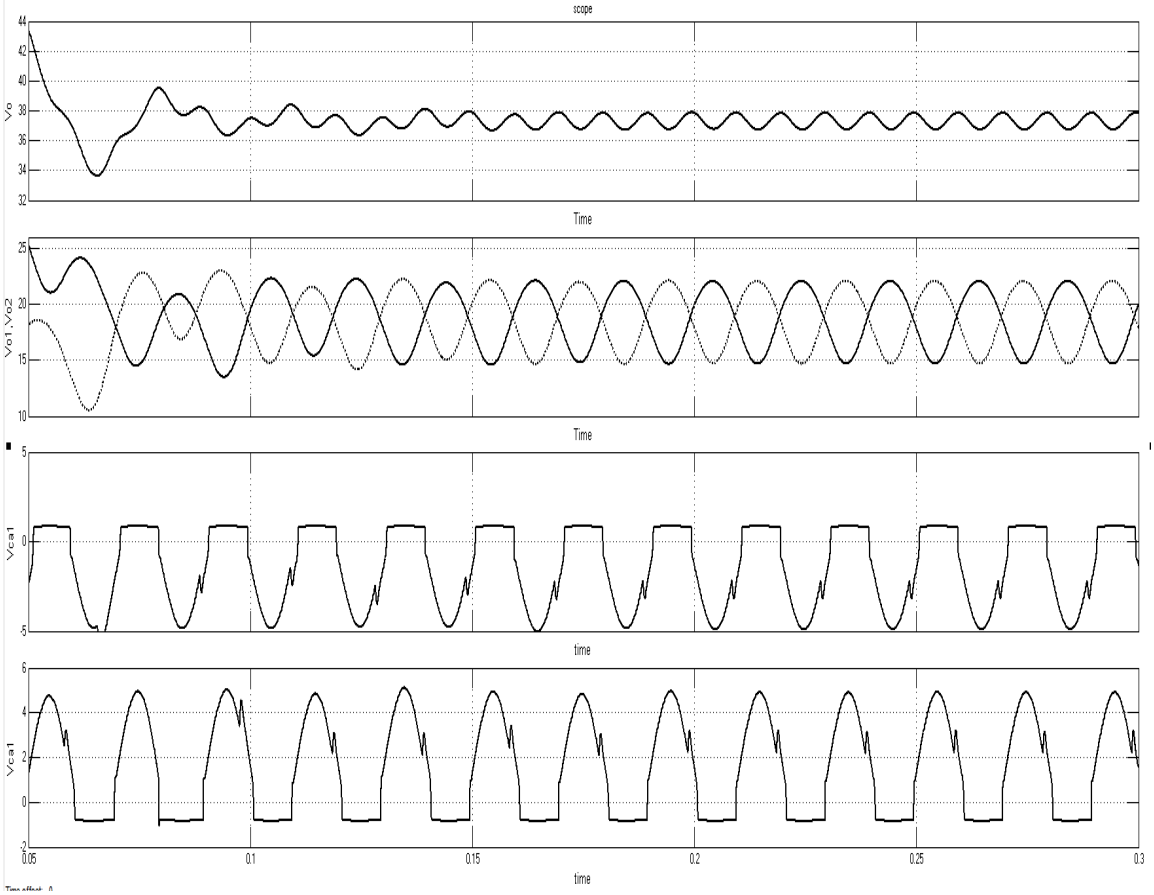

Fig.10.Low frequency voltages

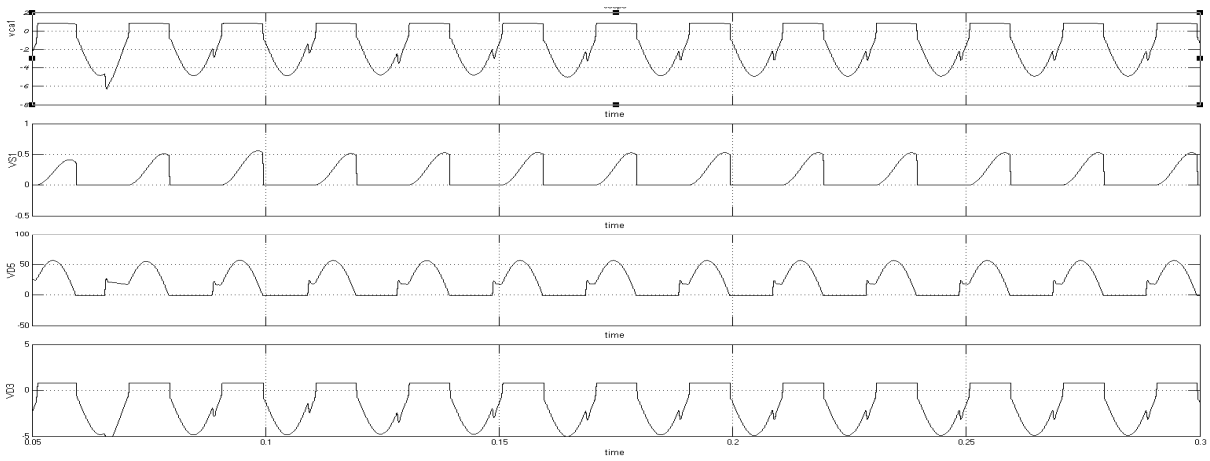

Fig.11.Switching voltages at peak of the line voltage

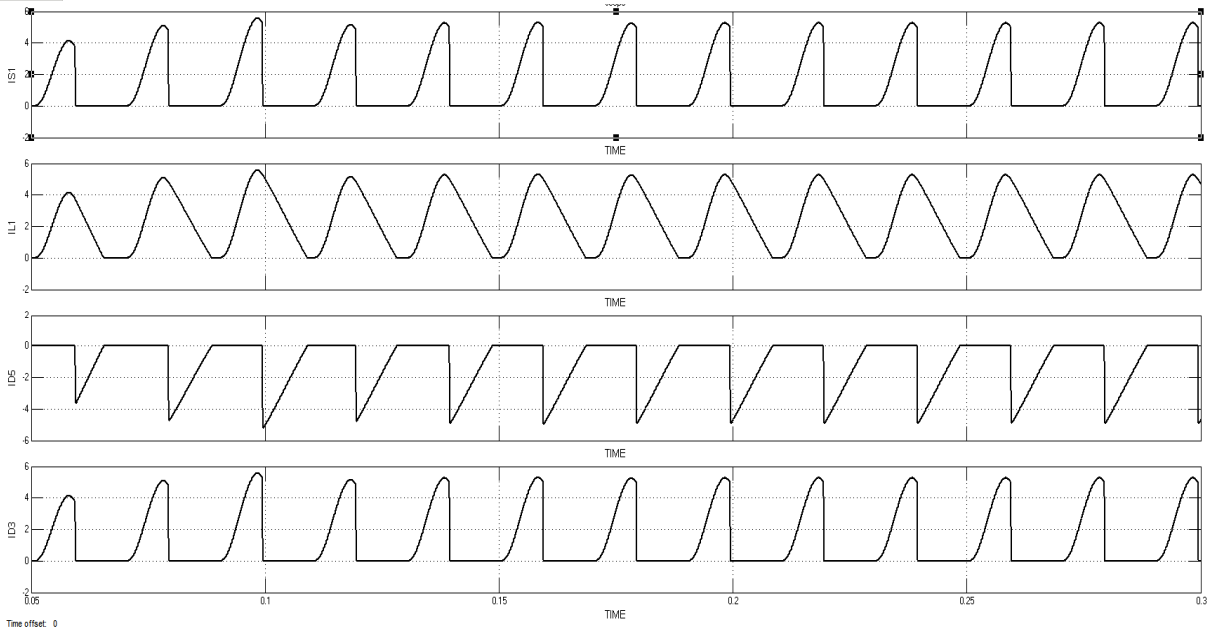

Fig.11.Switching current at the peak of the line voltage

VI. CONCLUSION

This paper presented a bridgeless unity power factor buck rectifier. It is shown that without any special design requirements, the dead angle of the buck rectifier can be eliminated. As a result, a unity power factor and a high efficiency can be achieved. A detailed theoretical analysis and design procedure have been presented and verified by experimental results obtained on a 150 W, 48 V output prototype, and 110 V line voltage. Thus, the proposed converter can achieve a unity power factor, a THD of less than 7% and a high efficiency of around 94%.

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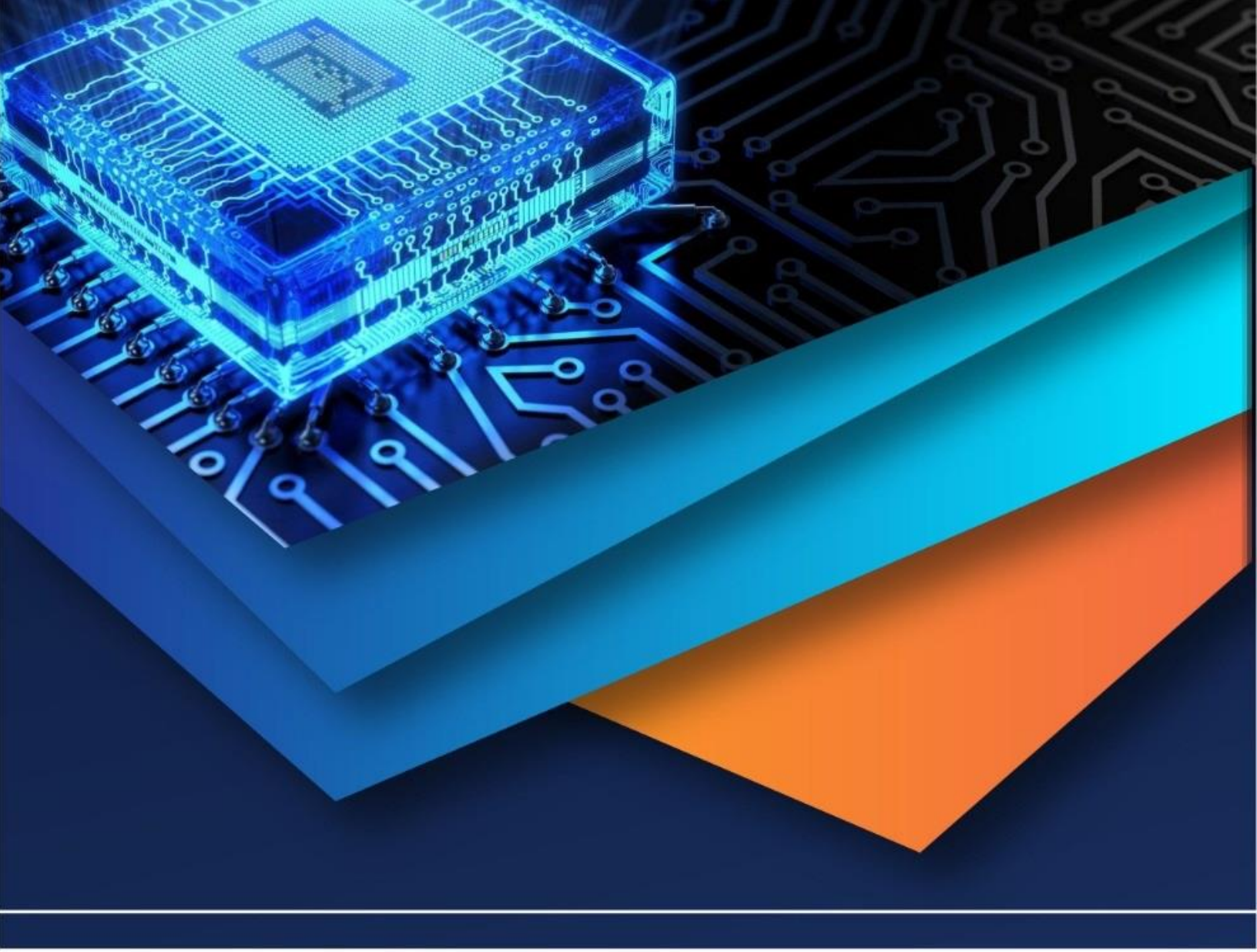

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