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Review on an Algorithm for Three Stage Clos Interconnected Network

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Abstract- ***Clos Interconnection network is one of the known connection networks in processing systems and distributed systems, which is used extensively in many fields such as Telecommunication networks, ATM switches and Data transmission. In order to eliminate the blocking in such networks, various routing algorithm have been proposed, each imposing extra costs due to hardware use and re-routing algorithm. This study offers a routing algorithm which takes a blocking-avoidance approach hence avoiding related costs. There is no blocking while the primary routing is performed from the input to output. This method has the complexity of*** $O(N\sqrt{N})$.
Keywords- ***Clos Interconnection Networks, Routing Algorithms, MIN, Crossbar Switches, Router***

I. INTRODUCTION

As one of the most important parts of parallel processing systems, interconnection networks make connection between switches. The topologies typically found in processing systems are often regular [1].
Topologies are classified as follows:

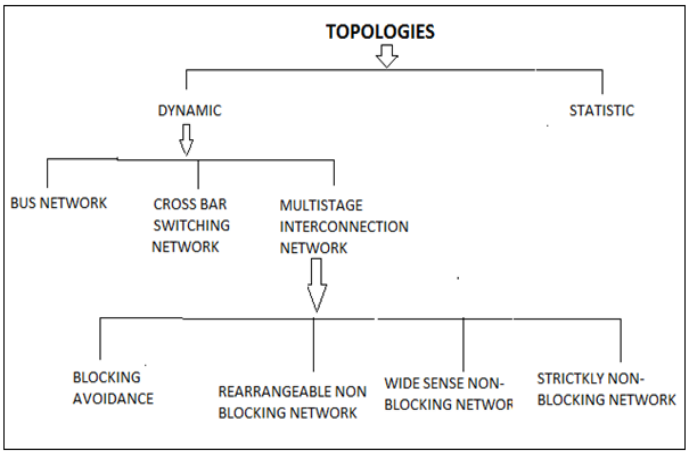

Fig: 1Classification of Network Topologies

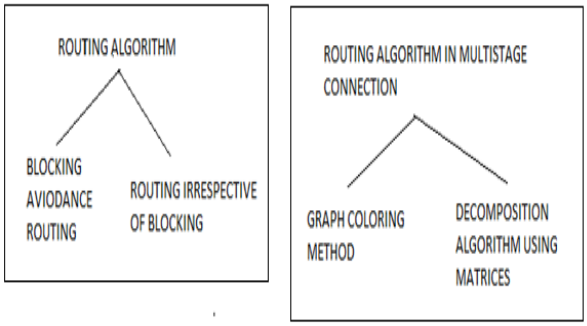

Fig: 2 Types Of Routing Algorithm

A. Types Of Routing Algorithm

1) *Blocking avoidance routing:* In the first method, routing of algorithm is performed in such a way that there is no blocking.
2) *Routing irrespective of blocking:* In the second method, initially the routing is performed from input set to output set. In

case of any blocking, attempts are made to eliminate it through changing the arrangements in network switching, using routing algorithm.

B. Types of Multistage Routing Algorithm

1) *Graph coloring algorithm:* Generally, graph coloring algorithm enjoys a better time complexity than decomposition algorithm, using matrix. However, as the network size is too large, it will be inefficient

2) *Decomposition algorithm using matrixes:* Decomposition algorithm using matrixes has the following advantages: Directly locating the problems and enjoying simplicity in switching settings [2]

Here routing algorithm is used for Clos interconnection networks. These routing algorithms are referred so as to find out the shortest distance between source and destination for faster and proper transfer of data. To do this routers are used [1].

II. CLOS NETWORK

Using small crossbar switches, Charles Clos introduced a type of interconnection network which is extensively studied and applied as a framework for ATM switches because it is, simple and regular, scalable, economical, fault-tolerant and highly efficient. Special attention has been paid to Clos three-stage networks as they are rearrange able for developing multi-stage networks. These three stage-networks are intended to be used for data communication and parallel computing system.

A switching network is composed of one or more switch stages that can create various paths through creating various connections between their inputs and outputs. Clos three-stage network is an example of multi-stage switching.

Clos network were first created in the mid-1950 as a method to switch telephone calls. Clos networks evolved into crossbar topologies and eventually into chasis based Ethernet switches using a crossbar switching fabric. Now Clos network are used in modern data centre networking architectures to achieve high performance and resiliency. This concept has been around for many years and now it is a key architectural model for data centre networking.

Charles Clos was a researcher and published a paper titled “a study of non blocking switching networks” in 1953. In this paper he described how telephone calls could be switched with equipment that used multiple stages of interconnection to allow the calls to be completed. The switching points in topology are called crossbar switches.

Clos network made reappearance many years later in 1990’s when early Ethernet switches were being developed. Clos network have now made their second reappearance in modern data centre switching topologies. However, this time, rather than being a fabric within a single device the Clos network now manifest itself in the way that the switches are interconnected. [8]

III. ROUTER

A router is a networking device, commonly specialized hardware that forwards data packets between computer networks. This creates an overlay internetwork, as a router is connected to two or more data lines from different networks. When a data packet comes in one of the lines, the router reads the address information in the packet to determine its ultimate destination.

Using information in the routing table or algorithm, it directs the packet to the next network on its journey. Routers perform the “traffic directing” functions on the internet. [4]

Most familiar type of router are home and small office routers. Eg: DSL (owner’s router), enterprise router, core routers.

Though routers are typically dedicated hardware devices, use of software based routers has grown increasingly common. The very first device that had fundamentally the same functionality as the router does today was Interface Message Processor (IMP); IMP’s were the devices that made up the ARPANET, the first packet network. The idea for router (called “gateways” at that time) initially come about through an international group of computer networking researchers called the International Network Working Group (INWG). These devices were different from most previous packet networks in two ways. First, they connected dissimilar kinds of network, such as serial lines and local area networks. Second they were connectionless devices, which had no role in assuring that traffic was delivered reliably.

Sometime after early 1974 the first Xerox routers became operational. By the end of 1976, three PDP- 11–base routers were in service in experimental prototype internet. Virtually all networking now uses TCP/IP, but multi protocol routers are still manufactured. Modern internet routers that handle both IPv4 and IPv6 [4] are multiprotocol, but are simpler devices. From mid 1970’s and in 1980’s general purpose mini computers served as routers.

Modern high speed routers are highly specialized computers with extra hardware added to speed both common routing

functions such as packet forwarding, and specialize functions as IPSec encryption.

IV. ALGORITHM PROPOSED FOR CLOS NETWORK:

Many proposed decomposition algorithms using matrix are said to be incomplete.

A. Neiman algorithm has been implemented, using decomposition matrix and time complexity $O(N\sqrt{N})$.

B. GS algorithm with complexity $O(N\sqrt{N})$ uses 2 matrixes, namely: Specification and Count. But Siu, Chiu, Lee and Carpinelli believes GS algorithm to be incomplete.

C. Later, a new method called the modified methods of GS was proposed. This algorithm was proposed at time $O(N\sqrt{N}Log\sqrt{N})$, by adding 3 steps to the main algorithm and deleting 2 steps for purpose of eliminating indefinite loops.

D. Later, an algorithm on the basis of Heuristic Routing Algorithm using minimum distribution priority scheme was introduced for routing Clos networks. This method had the capability of accessing all non-blocking routings, reducing its time complexity to $O(N\sqrt{N})$ in the worst situation [6].

V. THREE STAGE CLOS INTERCONNECTION NETWORK

A. Crossbar Switches

The Clos network is composed of crossbar switches. As many stage of these switches gives rise to the respective staged Clos interconnection network.

1) Properties Of Crossbar Switches

a) A crossbar switch is a assembly of individual switches between multiple inputs and multiple outputs.
b) The switches are arranged in matrix.
c) If crossbar switches has M inputs and N outputs, then a crossbar has a matrix with M x N crosss-points or places where the "bars" cross.
d) At each cross-point is a switch; when closed it connects input to output.
e) Collection of crossbars can be used to implement multiple layer and/or blocking switches.
f) A crossbar switching system is also called a co-ordinate switching system.

i) Applications of Crossbar Switches: Crossbar switches are most famously used in information processing applications, such as telephony and circuit switching. Its matrix layout is also used in some semiconductor memory devices. Eg: P-ROM. Crossbar switches are also used to form multistage Clos network. A special crossbar switches used in distributing satellite TV signals are called multi-switches.

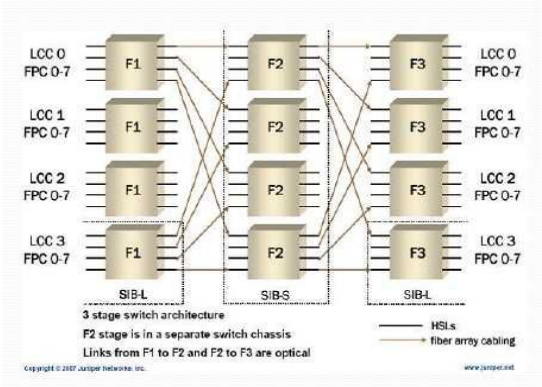

Fig: 3 Crossbar Switches.

2) Three Stage Networks: Clos three-stage networks $N \times M$ are represented as $c(n1, n2, m, r1, r2)$

Where,
N = represents the overall inputs of network and

M = as overall outputs of network.
n1=represent the number of inputs of each switch of input stage,
n2 = the number of outputs of each switch of output stage,
m = number of switches of middle stage,
r1 =number of switches of input stage and
r2 = number of switches of output stage.
If $N = M$ then $r1 = r2$, $n1 = n2$.
Such Clos networks where input equals output switches are called Clos symmetrical network and shown as $c(n, r, m)$.
Stages of a three-stage network:

- 1st stage : Input stage which includes r $(n \times m)$ switches.
- 2nd stage : middle stage which includes m $(r \times r)$ switches.
- 3rd stage : output stage which includes r $(m \times n)$ switches.

The network is capable of connecting one to one and one to many with $N = nr$ and $m \geq n$. There is a link between 2 switches in 2 continuous stages. As $c(n, r, m)$ knows all possible permutations between inputs and outputs. A link can be accessed between stages, provided it is usable and not engaged [9].

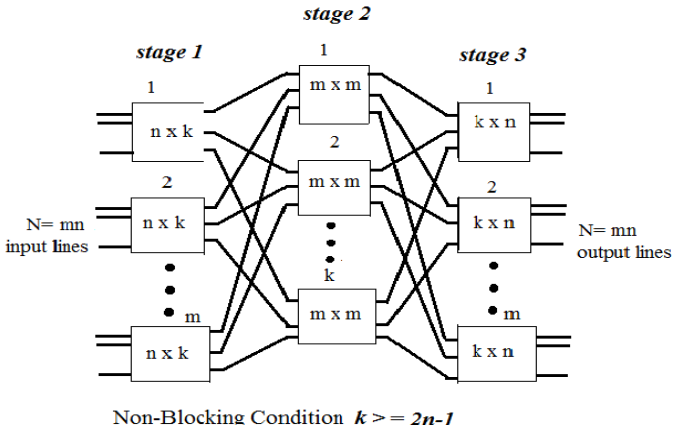

Fig: 4Three stage Clos network

VI. BLOCKING AVOIDANCE ROUTING ALGORITHAM IN CLOS NETWORKS:

It can be shown that with $k \geq n$, the clos network can be non-blocking like a crossbar switch. That is for each input-output matching we can find an arrangement of paths for connecting the inputs and outputs through the middle-stage switches. The following theorem shows that for adding a new connection, there won't be any need for rearranging the existing connections so long as the number of middle-stage switches is large enough.
Clos Theorem**:** If $k \geq 2n-1$, then a new connection can always be added without rearrangement.
Proof: Consider adding the nth connection between 1st stage *Ia* and 3rd stage *Ob* as shown in figure 2. We need to ensure that there is always some center-stage M available. If $k > (n-1) + (n-1)$, then there is always an M available. i.e., we need $k \geq 2n - 1$.

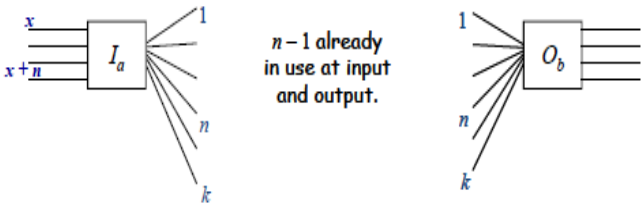

Fig: 5 Adding the nth conection.
Where input i is connected to output $\pi(i)$ and $0 \leq i \leq N-1$, $N = nr$.
The switch between input and output is assumed to be of non-blocking type.

P may be changed between input switches and output switches.

In this algorithm, the matrix is used in such a way that network initially has its connections. Then, the new inputs are added into the network in such a way that there will be not any blocking. This is made possible through 4 main matrixes (A, B, C, D) and an mono dimensional array (e). The matrixes consist of elements 0, 1. 0 represents the free link and 1 represents the engaged link in the network[11].

A. Matrices And Array (e) Description :

1) Matrix A represents a connection between input switches and inputs of each input switch. The number of rows (i) represents input switches and the number of columns (j) represents the inputs of each input switch.

2) Matrix B represents the connection between middle switches and inputs of each middle switch. The number of rows (i1) represents the middle switches and the number of columns (j1) represents inputs of each middle switch.

3) Matrix C shows the connections between output switches and inputs of each output switch. The number of rows (i3) encompasses output switches and the number of columns (j3) represents the input of each output switch.

4) Matrix D indicates the connection between the outputs of each output switch and output switches. Here, the row (i4) represents output switches and columns (j4) represent the outputs of each output switch.

5) Array (e): each member of this array represents the number of the engaged input of each middle switch. The length of the array equals the number of middle stages.

All steps are complete when the elements of matrix A are transferred to matrix D. That is, all contents of input switches are added in the network and the input stage links are free for receiving new inputs.

B. Blocking Avoidance Algorithm :

1) Initially, 0 is assigned to matrixes B, C, D and array (e).

2) Matrix A is derived from the inputs.

3) In matrixes B and A, a movement is made in parallel in such a way that in matrix A, the movement is made from row to row and in matrix B form column to column. When 1 is seen in matrix A, a free link is needed in middle switches to which the inputs are transferred. Then we turn to matrix B, searching for 0. On finding the first 0 in matrix B, we should replace it by 1 in matrix A.

4) Having transferred all engaged links of matrix A (input stage) to matrix B (middle stage) in such a way that there is no blocking in the input switches, now the output of middle stages should be arranged. To this purpose, the number of engaged input links into each middle switch is calculated, then added to the array (e). Having calculated all engaged links, we should assign the passive output links in middle switches (matrix B) to the engaged input links in middle switches (in array (e)).

5) We should arrange matrix B (middle stage) to matrix C (output stage) in parallel so that matrix B is examined in terms of columns and matrix C in terms of rows. On seeing 1 in matrix B, we should replace it by 0 in matrix C.

6) Finally, in order to transfer the engaged links to the output, we should make use of matrix D. That is, the movement in matrix C should be made from row to row and in metric D from the row to row in parallel. On seeing 1 in matrix C, it is replaced by 0 in matrix D.

C. Pseudo Code Of Blocking-Avoidance Routing Algorithm:

Step1) Initialize by Setting Middle Matrix(B), Matrix(C), Matrix(D) and Middle array (e) = False.

Step2) Read Input Matrix (A).

Step3) For each of row elements of Matrix A, that is "True", if ($A[i, j] == 1$) then
{Find The First column elements of Matrix B, that is "False",
if ($B[i1, j1] == 0$){Swap ($A[i, j]$, $B[i1, j1]$); }}

Step4) For each of row elements of Matrix B, that is "True", if ($B[i1,j1]==1$)
then {S++;}e [k++]=S; if ($e[k>0]$) then { $B[k][j1]=1$, k-- ;}

Step5) For each of column elements of Matrix(B) , that is "True" ,
if ($B[i1,j1]==1$) then {Find The First row elements of Matrix C,
that is "False", if ($C[i3,j3]==0$) {Swap ($B[i1,j1]$,$C[i3,j3]$) ;}}

Step6) For each of row elements of Matrix C , that is "True", if $C[i3,j3]==1$
then { Find The First row elements of Matrix D, that is "False",
if ($D[i4,j4]==0$) { Swap($C[i3,j3]$,$D[i4,j4]$);}}

As you can see, all elements in matrixes A, B and C can be transferred to the next stage matrix in a parallel manner. This speaks for the parallel routing in the proposed manner.[9] [11]

VII. COMPARING BLOCKING AVOIDANCE ROUTING ALGORITHM WITH THE PREVIOUS METHOD:

This algorithm and previously proposed algorithm are compared on the basis of :

A. *Complexity:*

The following should be taken into account to compute the complexity of routing algorithm:

1) m = n, this indicates that the number of middle stage switches (m) equals the number of input ports of the switches of input stage (n).
2) N= r×n, this indicates that overall network inputs are obtained by multiplying the number of switches of input stage (r) by the input ports of each switch of input stage (n).
3) $n = \sqrt{N}$.

Each matrix is read by time $O(N)$ and the main body of algorithm is formed at $O(N\text{n})$. thus, the overall complexity of proposed algorithm is :

$O(N\text{n})+3O(N\text{n})=O(N\text{n})$----------—> $ON\sqrt{N}$; for n=√N.

Table: 5.1 : Complexity of various algorithms.

Algorithm name	Complexity of routing Algorithm
GS Algorithm	N√N
GS Modification Algorithm	N√N log√N
Heuristic Algorithm	N√N

As table shows,

1) The proposed routing algorithm outperforms the GS modified routing algorithm, with the former maintaining the network hardware.
2) The proposed routing algorithm also equals Heuristic routing algorithm and GS routing algorithm in terms of algorithm complexity.
3) In GS routing Algorithm, there are indefinite loops which don't appear in the proposed routing algorithm in this study, resulting in higher efficiency of the proposed method.
4) In heuristic routing method, rearrangement is required. This leads to additional costs. While, in blocking avoidance approach, there is no such cost. This is because the blocking is eliminated while routing is being done.[5].

Hence, the better is the performance of this method over other methods.[7]

B. *Time :*

1) Regarding time, the algorithm proposed by this study outperforms the previously proposed methods.
2) The previous methods start routing without taking account of blocking.
3) That is, when routing is over, these methods make an attempt to eliminate the blocking through using some new algorithm, taking some time.
4) This method proposed by this study starts routing so as to prevent the occurrence of any blocking, saving a lot of time.

VII. CONCLUSION

This study presents a routing mechanism in Clos interconnection networks, taking a blocking-avoidance approach so that the routing is performed properly from input to output without blocking the links in network. While in the previous methods, the

strictly non-blocking network was defined by simple routing which results in high hardware costs. Or alternatively, the routing was performed irrespective of blocking. Then, a new algorithm was used to eliminate these blocking, leading to some costs. The method proposed by this study has solved this problem. On the other hand, this algorithm completes its cycle at time $O(N\sqrt{N})$ This type of routing can be used in communications switching as well as in data transmission networks for purpose of reducing the delay in transference time and for controlling the network traffic. The future studies can examine the ways in which new algorithms can be used to reduce routing time and the use of memory and to reduce the complexity of algorithm.

VIII. FUTURE SCOPE

Several research directions in randomised routing need to be pursued and are currently under investigation. The fault tolerance capabilities of the algorithm are to be examined. The algorithm turns out to be highly adaptable to fault tolerance and can tolerate many switch faults of various types. Other modes of routing than this, will be studied probabilistically and using simulation. Randomization will be applied to Clos network of more than 3 stages to determine the efficacy of randomization of this network as well as on the communication delay.

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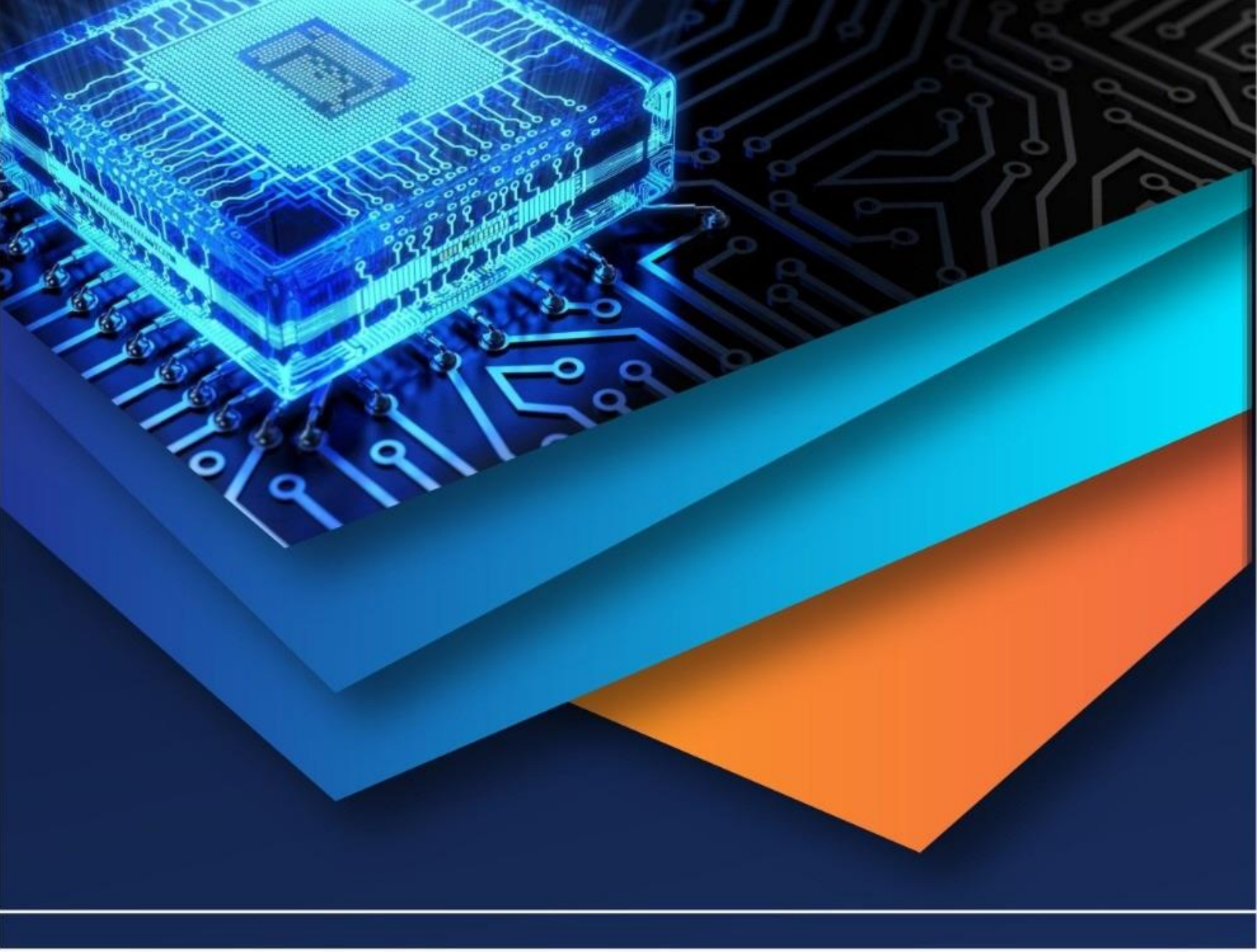

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