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Implementation of Low Power Voltage Level Shifter using GALEOR Technique for Sub threshold Operation

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Abstract: ***The Voltage Level Shifter is wide employed in varied integrated circuits lately like in analogue computers, simulation systems and in several electronic applications as filtering, buffering and comparison of signal levels. Usually voltage level shifter converts low levels of input voltages in to high output voltage levels. In this paper varied kinds of voltage level shifters area unit mentioned chiefly specialise in the ability economical voltage level shifter, before this architecture explain the architecture of high speed voltage level shifter. To reduce the power consumption implement voltage level shifter with GALEOR technique. GALEOR (Gated LEakage Transist OR), reduces the leakage current flowing through the circuits. new static power reduction technique named GALEOR, which reduces the leakage current flowing through the circuit by creating a stack effect using high threshold voltage transistors in between the pull-up and pull-down networks. GALEOR technique achieves on average 25% savings in leakage power. GALEOR Circuit is connected across the input and output terminals. The improved design power consumption is forty share but the high speed voltage level shifter with auxiliary circuit.. In this dual supply architectures are used. Those are low supply voltage VDDL=0.4V and high supply voltage VDDH=1V, Input frequency is 1MHz. The circuits bestowed during this work area unit analyzed by mistreatment the backend tool CADENCE.***
Keywords: sub threshold, level shifter, analog blocks, auxiliary circuit.

I. INTRODUCTION

A voltage level shifter incorporates a path receiving a provide voltage that varies between initial|a primary} operative price in an exceedingly first operative condition and a second high operative price, in a second operating condition [1], [2].A latch stage is connected to Associate in Nursing output branch and to a variety circuit, that receives a variety signal that controls shift of the latch stage. In digital circuits dynamic and short-circuit power consumption is reduced by lowering the worth of the facility provide voltage .It can be also reduced by increased supply voltage, because if this propagation delay of the circuits was increased. On the other hand minimized headroom in analog circuits decreases signal swings due to this increases the sensitivity to noise. Hence, in moderate-speed mixed signal circuits or in digital circuits wherever totally completely different elements operate at different speeds, dual-supply architectures are introduced in which a low voltage (i.e., VDDL) is supplied for the blocks that square measure in noncritical methods whereas analog and also the high-speed digital blocks square measure driven by a high provide voltage (i.e., VDDH) [3].In a system with dual supply voltages, level-shifting circuits are used convert the lower voltage levels into the higher ones to provide correct voltage levels for the succeeding digital blocks. In this manner to alleviate the degradation of the whole performance of the circuit, the required level shifters must be implemented with minimum propagation delay, power consumption, and silicon area.

The remaining of this paper is as follows. In Section II, economical voltage level shifter with auxiliary circuit is reviewed. The proposed circuit is introduced in Section III.Section IV presents the simulation results of the designed circuit validatory the potency of the planned structure. Finally, this brief is concluded in Section V.

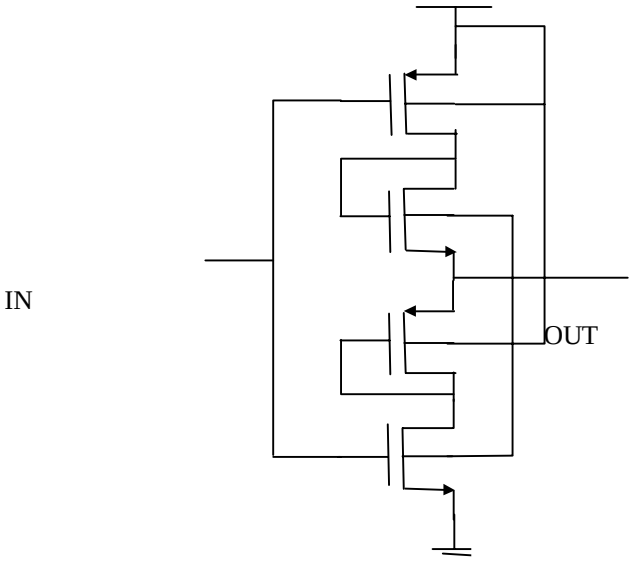

Fig.1. GALEOR Technique

When the Device density is high and threshold voltages of the transistors is low then mechanically increase the run current dissipation. The proposed static power reduction technique, GALEOR (GAted LEakage TransistOR) is use in high speed power efficient voltage level shifter it results in reduces the leakage currents in the circuits. This run power technique is applied to existing level shifter , in this circuitry one of the gated leakage transistors is connected bellow the pull-up transistor and another gated leakage transistor device is connected higher than the pull-down transistor of the present circuit specified gates of the gated run transistors square measure connected to their drain regions consecutive. GALEOR technique was first tested on standard cell gates and memory elements the researches shows by use of control logic to switch Area overhead is minimised. Because of the reduced output voltage swing Performance overhead is raised.

II. EFFICIENT VOLTAGE LEVEL SHIFTER WITH AUXILIARY CIRCUIT

High speed voltage level shifter provides higher|the higher} output response and better delay, however this circuit consumes additional power.To overcome this downside designed the economical voltage level shifter with auxiliary circuit.This circuit have AN auxiliary circuit therewith of economical voltage level shifter[4]. The main purpose of the auxiliary circuit is it activates solely within the high to low transition at the same time QC is charged to the worth more than the VDDL.

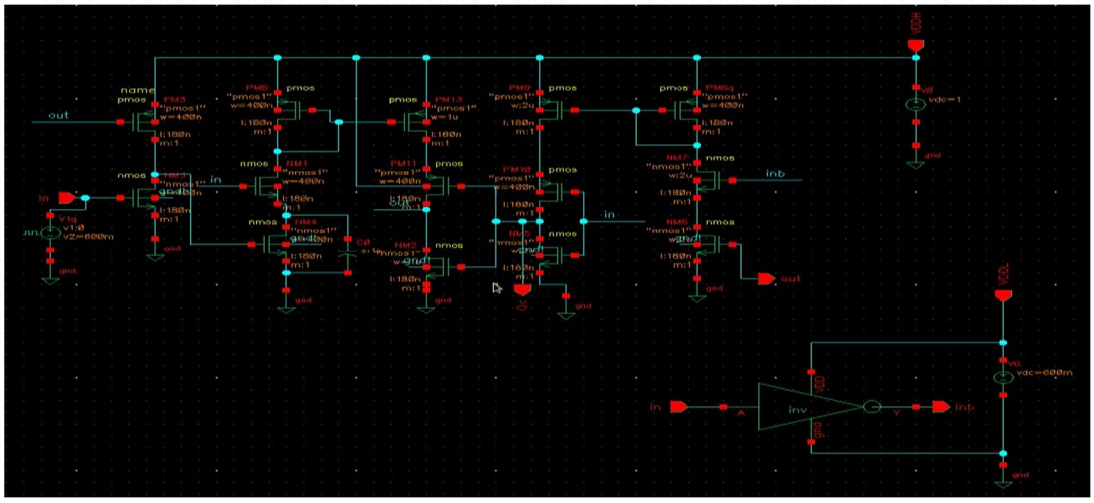

Fig.2. economical Voltage Level Shifter with Auxiliary Circuit .

The operation circuit is as follows. When IN value is from “High” to “Low” in this time of action OUT is related to the previous input logic level so MN6, MN7, and MP6 are going to be saturated and MN5 is cut off. Therefore, a transition current flows through MN6,MN7, MP6, this circuit have mirror structure at the MP6 then same amount of current mirrored at MP7 (i.e., IP7) at particular time MP7 is pulling up the node QC.It shows that MP4 I in stop and MP2 is activate with a price more than the VDDL.
After this OUT voltage is diminished utterly at the same time MN6 turned off then current flows through the MN6, MN7, and MP6 square measure zero[5].The whole operation states that auxiliary circuit is turns off within the low to high transition.It minimizes the facility consumption only the input vary is from in high to low.

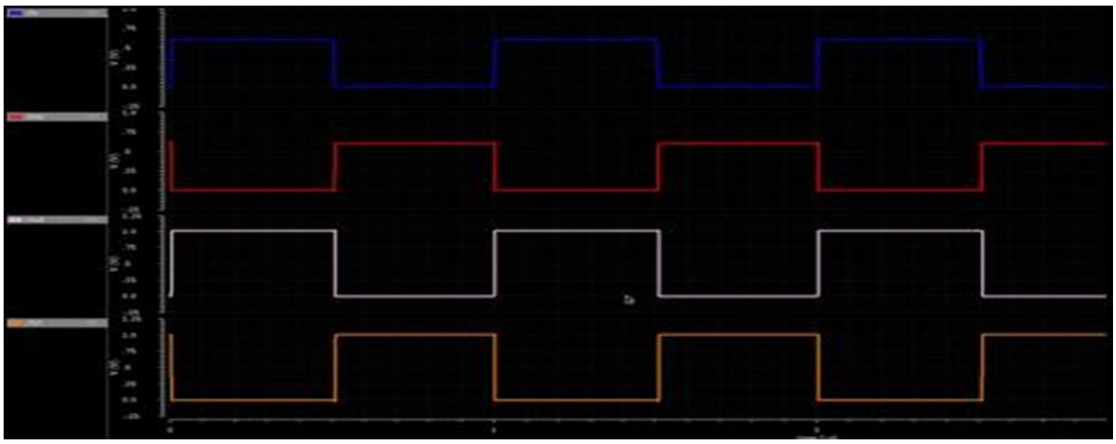

Fig.3. Simulation Results of Efficient Voltage Level Shifter with Auxiliary Circuit

Fig. 3. Shows the simulation results of efficient voltage level shifter when applied input IN is high, INB is low then output voltage is low and Qc is high.It shows the voltage levels during this specific circuit it drastically lowering the facility consumption, thus so as to cut back the facility consumption in low to high a circuitwas designed that is Low Power Voltage Level Shifter With GALEOR Technique For Subthreshold Operation .

III. LOW POWER VOLTAGE LEVEL SHIFTER WITH GALEOR TECHNIQUE FOR SUBTHRESHOLD OPERATION

High performance and procedure capability within the current generation processors square measure created doable by little feature sizes and high device density.To maintain this drive strength and management the ability dissipation in these processors, cooccurring cutting down of offer and threshold voltages is performed[6].As the name implies that when the circuit is operated in subthreshold region, in this region the low power voltage level shifter effectively converts low level of input voltage levels on to high output voltage levels voltage with the help of GALEOR (Gated LEakage TransistOR),Circuit.In this style of implementation have 2 high Green Mountain State gated run transistors NMOS and PMOS transistors, these are placed between the middle of pull-up transistor and pull-down transistor.Because of this arrangement stack result is elicited due to this stack result run current reduced and also the resistance of the run path is inflated.When the resistance of the run path is will increase run currents within the circuit was reduced.It suggests that the ability consumption of the whole circuit was reduced.The performance of the circuit depends on the ability consumption therefore the performance of the circuit was increased.

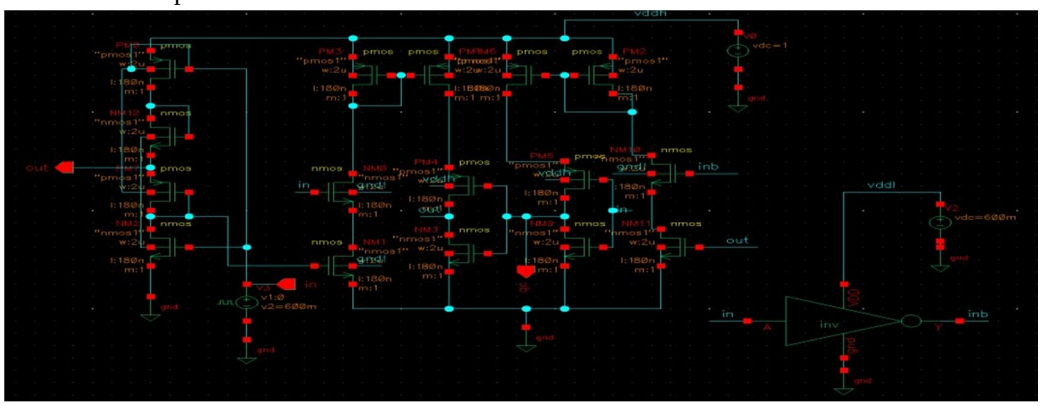

Fig.4. Low Power Voltage Level Shifter with GALEOR Technique

Input pattern of the each gate shows some effects on sub threshold voltages as well as leakage currents.

The run current of semiconductor device in an exceedingly stack may be a perform of variety of transistors and input patterns. The entire circuit was constructed in cadence virtuoso[4].Operation of this circuit is same because the before circuit i.e efficient voltage level shifter, it conducts both transitions those are high to low and low to high transition. But this low power voltage level shifter with GALEOR technique conducts only in high to low transition in this manner the total power consumed by the circuit was reduced. In this circuit conjointly electrical converter driven with low input voltage and it provides high output voltage to drive the ensuing digital block within the circuit. The circuit with GALEOR technique have reduced power and increased speed by shutting off the some transistors in the time of working ,the circuit was operated in subthreshold range but it's even have operating condition in on top of threshold vary. High device density and low threshold voltages lead to a rise within the run current dissipation[5].Large on chip caches are integrated onto the current generation processors which are becoming a major contributor to total leakage power. The proposed static power reduction technique, GALEOR (GAted LEakage TransistOR), reduces the leakage current flowing through the circuits. Area overhead is reduced by eliminating the utilization of management logic to modify between the active and standby states. Performance overhead is inflated thanks to the reduced output voltage swing.

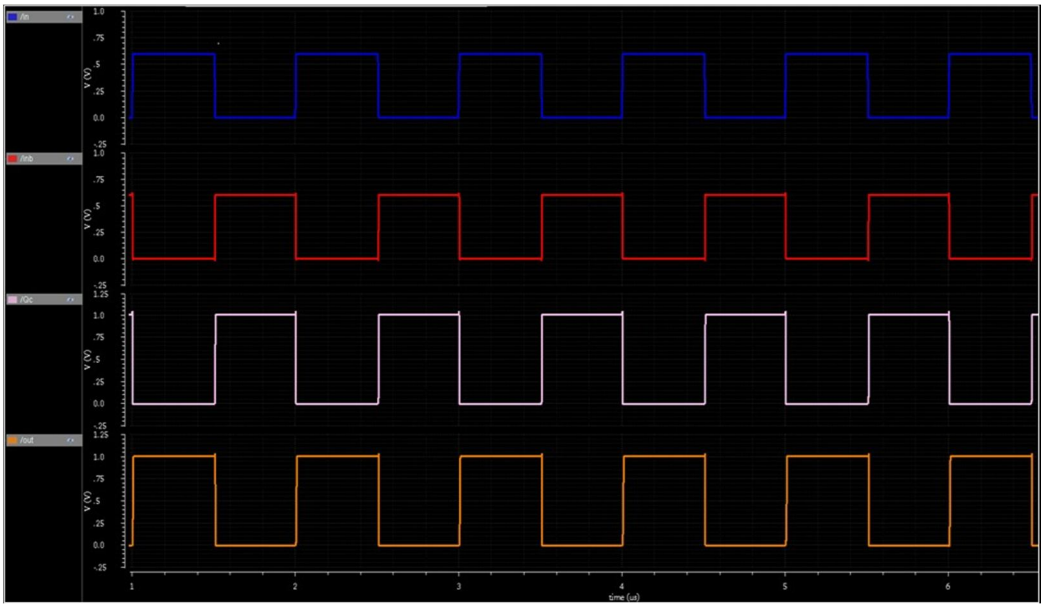

Fig.5. simulation results of low power voltage level shifter with GALEOR technique

When the IN voltage range is from high to low and INB is from low to high in this time of operation the transistors conduction is same as the efficient voltage level shifter but in GALEOR circuit it balances the power consumption so it results the overall power consumption was reduced. The out voltage is same phase as compared to IN but it reaches the value higher than the input voltage at the same manner Qc value us also reached certain worth same because the output however the 2 signals output and Qc square measure in opposite part.

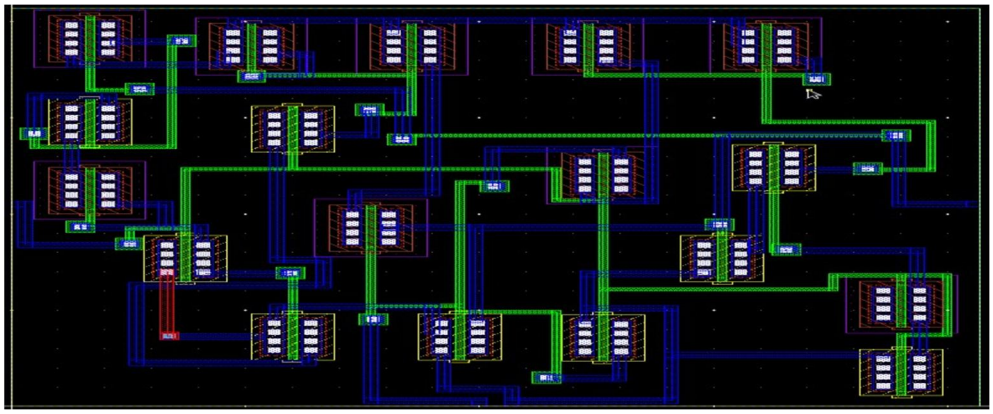

Fig.6. Layout of High Speed and Power efficient Voltage Level Shifter

IV. SIMULATION RESULTS

The projected voltage level shifter was verified by exploitation Cadence virtuoso in normal TSMC zero.18µm CMOS technology. The bend results have reduced power-delay product (PDP).

Table.1. power, delay and transistor count reports in 180nm Technology

.Circuit	Power	Delay	Transistor Count
Efficient voltage level shifter with auxiliary circuit	247nW	3.23ns	14
Low power voltage level shifter with GALEOR Technique	137nW	2.24ns	16

The given table contains the values at totally different frequencies and for varied values of Vddl, The delay and power square measure determined, the competition between devices is determined in sub-threshold region.
Due to lower temperature the time needed to come up with signals are going to be magnified and conjointly manufacture less current.

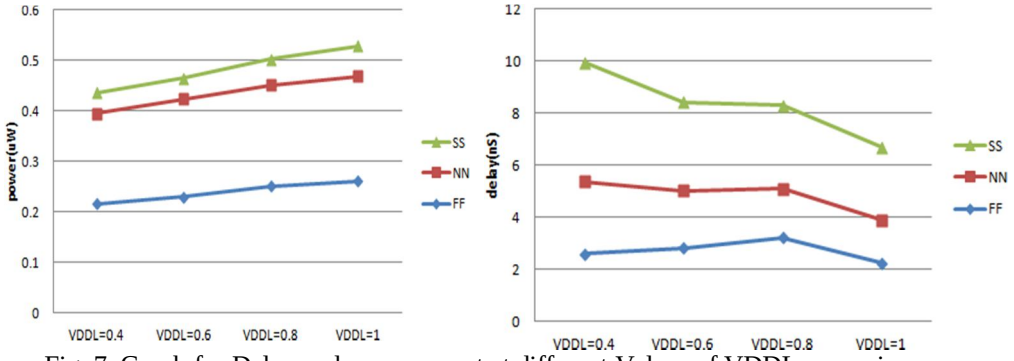

Fig. 7. Graph for Delay and power report at different Values of VDDL, on various corners.

This graphs shows the simulated output values of power and delay at totally different values of VDDL once provide voltage will increase then power consumption will increase and delay was reduced.

V. CONCLUSION

In this paper the planned circuit and existing circuit each square measure enforced in cadence virtuoso and determined the output engaging at totally different voltages to grasp the ability levels at each purpose. The experimental results shows the circuit with GALEOR circuit minimizes the power consumption and increase the speed by the help of GALEOR technique. The overall circuit achieves on average 25% savings in leakage power by connecting GALEOR Circuit across the input and output terminals.

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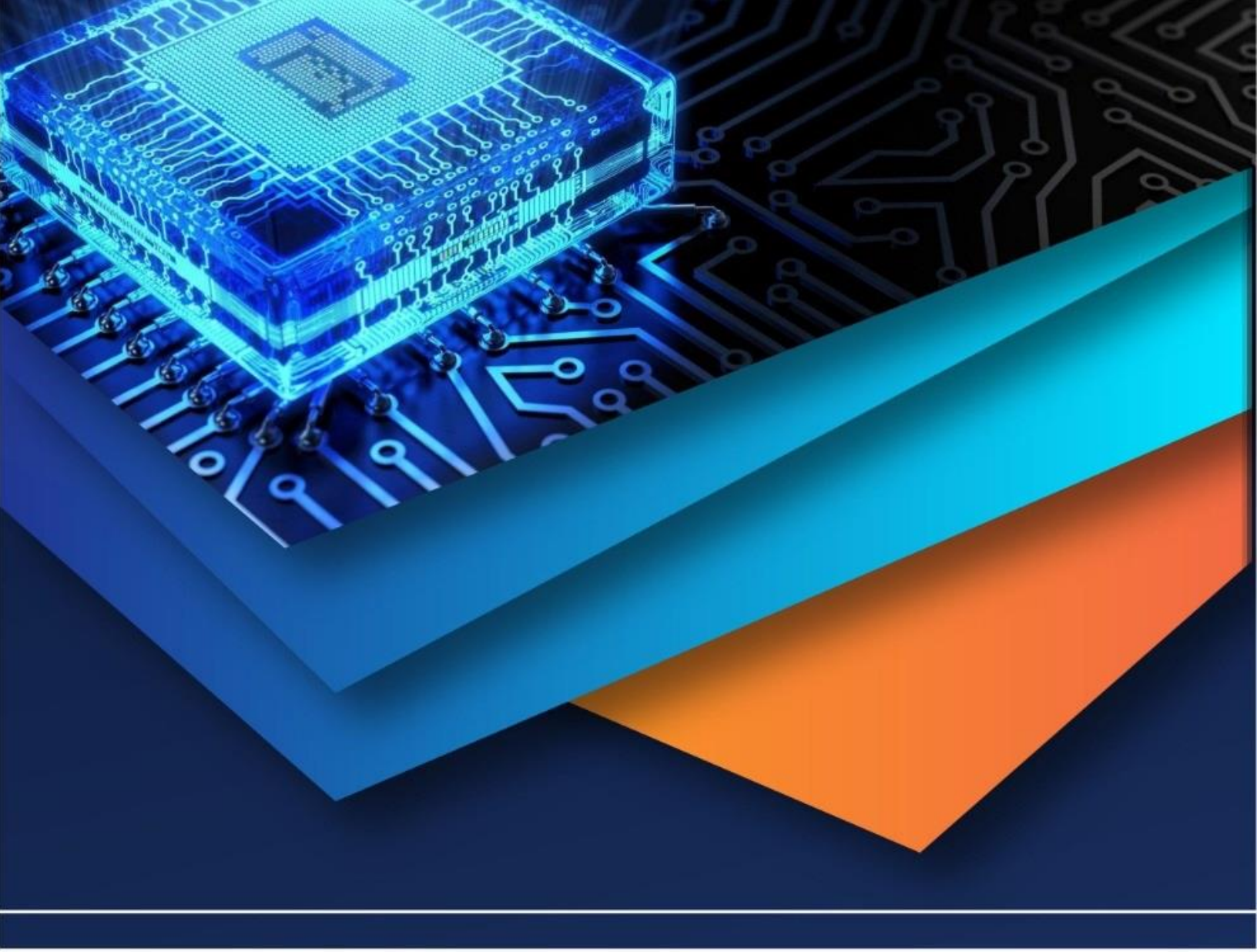

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