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Delay and Power Analysis of Three Coupled through Silicon Vias in 3D ICs

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***Abstract:** 3D IC is developing as an incredible response for the next generation system packaging and integration technology to accomplish low power utilization, high channel transfer speed and high-density integration capability simultaneously. With respect to the vertical interconnect for a 3D IC, through-silicon via (TSV) is a key part which can produce a myriad performance improvement with the extraordinarily decreased length of interconnects among vertically stacked dies. In this paper, the electrical equivalent model of a TSV is proposed and the electrical behaviour of three coupled TSV with the variation of length, diameter, and pith parameters are analysed.*

***Keywords:** Through Silicon Vias (TSVs), Three-Dimensional Integrated Circuits (3D ICs), Packaging*

I. INTRODUCTION

The legacy of planar scaling which has been satisfying the forecast in Moore's Law is at the edge of saturation. As technology advances in the nanometre era, the packaging density and system performance of individual chips improve. One of the primary reasons for the saturation is the physical size involved with semiconductor lithography that puts the limit to the dimension of transistors. The other significant issue related to scaling is the interconnect innovation. However, the scaling of the minimum feature size of the transistor slows due to the limitations of leakage power consumption, process variation, and cost issues. Since the finish of the last decade, the main pattern in the hardware industry is to increment the integration density in electronic gadgets utilizing three-dimensional (3D) integration. In addition, many electronic devices, such as tablets, laptops, and smartphones, have become more compact, and, they must achieve multi-function and high-throughput computing performance simultaneously. The production of integrated circuits (IC) is an important factor in the field of microelectronics. At higher levels of integration, the two-dimensional architecture results in numerous bottlenecks because of the area and routing congestion such as memory bottle neck in multimedia System on chips (SOCs). As the user demands are high regarding functionality of the system, the complexity of chip design increases and requires a large number of transistors which increases the size and delay of the circuit. As a new powerful paradigm for next-generation system integration and packaging technology, 3-dimensional integration emerges as a promising solution. With 3D integration, many chips can be integrated into a vertical axis, thus improving the system bandwidth by reducing the physical lengths of the channels among the integrated chips. At present, researchers are acknowledging 3D integration by stacking integrated circuit (IC) dies, where vertical interconnection is the fundamental way to communicate with other submodules. Thus, to accomplish the ideal execution in 3D framework, TSV interconnection is the key innovation.

In earlier days, the production of IC was designed using cable connections to the individual chips in the package. This leads to longer interconnection that lowers the performance of the device. To avoid such limitations, the chips can be connected together in place of each chip individually bound to the package substrate [1]. These interconnections are mostly implemented through the use of Through Silicon Vias (TSV). A TSV is a vertical metallic pillar surrounded by a dielectric material that passes through out the stacked plane matrices. By using TSVs the length of the interconnection has been lowered, this lowering significantly enhances device performance by decreasing power consumption and delay. The electrical property of a GSSG structure is analysed and implemented an accurate lumped model for the performance prediction of a TSV and studied about the bump radius, height and underfill material role in TSV performance and coupling factor [2]. The scalable and analytic electrical model is implemented for a TSV and the signalling performance and electrical behaviour at high frequencies are analysed in both frequency and time domains [3]. The Electromagnetic modelling for TSV interconnection is presented, that have an advantage of generating a model for large number of Through Silicon Vias using small number of basic functions that reduces the computational time [4]. However, few literatures are present on delay and power analysis it is very important to know the factors that are affecting these delay and power parameters. So, this paper mainly focused on these parameters.

The rest of this paper is composed of the following sections:

The architecture of TSV is discussed in Section II. The proposed TSV model is discussed in Section III. The simulations and results are discussed in Section IV. Some conclusions are offered in Section V.

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II. TSV ARCHITECTURE

A TSV consists of a cylindrical metallic pillar surrounded by a dielectric material that is used for connecting multiple devices in a chip. The top and bottom of this TSV is connected to bumps. The diameter of these bumps should be greater than the diameter of the TSV. The electromigration and scattering effects are lesser than the conventional wired interconnects and the transmission is uniform throughout the TSV. This helps in reducing the reliability issues and increases the device performance with low power consumption.

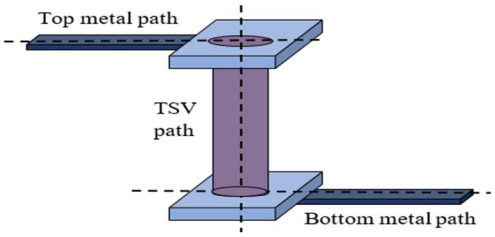


Fig. 1. TSV Structure

The above Fig. 1. Shows the structure of a single TSV connected to bumps on both top and bottom. The above figure is a 3D view of a TSV.

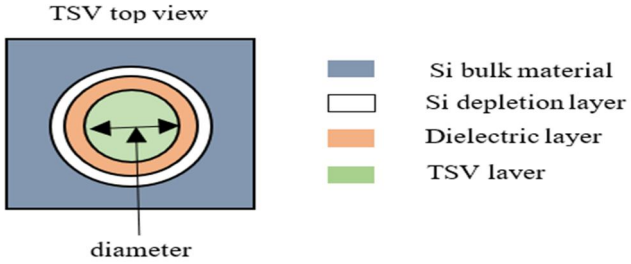


Fig. 2. TSV Top View

In Fig. 2. The total layers present in a TSV are clearly represented. The inner material is filled with the metal which is surrounded by a dielectric layer. These TSVs completely passes throughout the dies.

III.PROPOSED TSV MODEL

The proposed TSV model consists of three coupled interconnects that are connected parallelly which passes from top to bottom of 3D IC. The top and bottom of these TSVs are connected to bumps. These bumps are connected to underfill material that is used to form connectivity between chip and substrate.

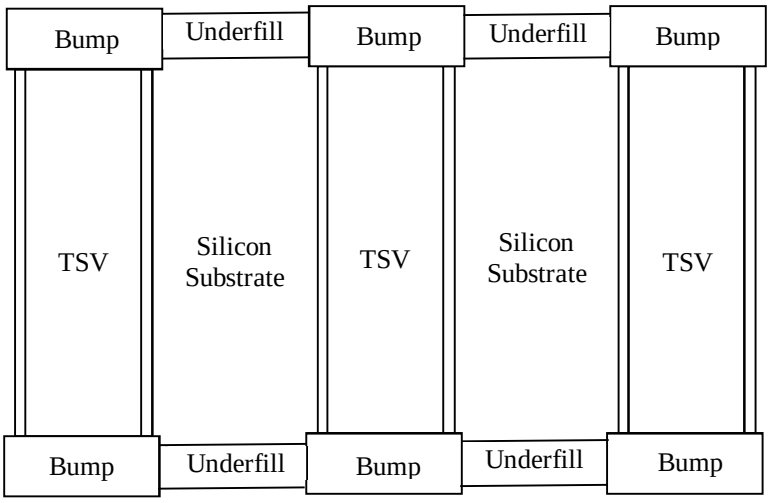


Fig. 3. Proposed TSV Model

The above Fig. 3 shows how the TSVs are located in the substrate. The bump diameter will be always greater than the diameter of TSV. Underfill is used to improve the reliability of a chip on a package, it is used to redistribute the thermomechanical stress created by the coefficient of thermal expansion (CTE) mismatch between organic substrate and silicon chip.

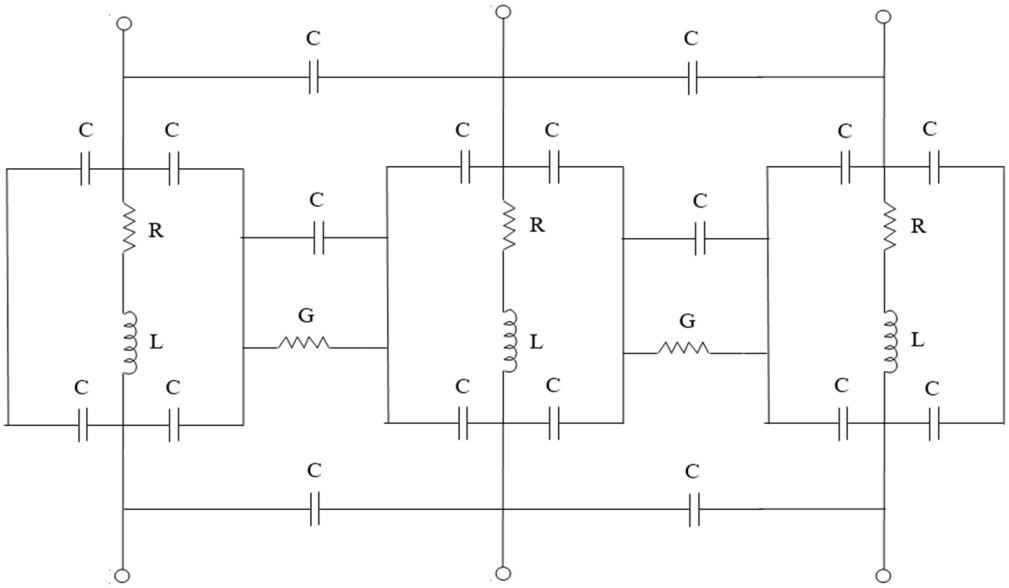
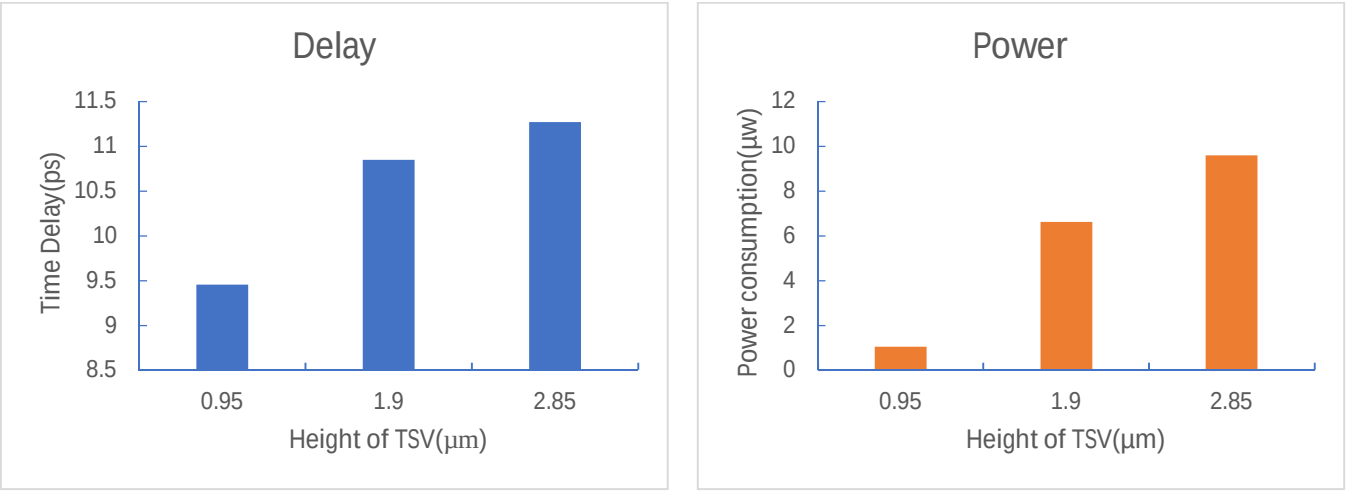


Fig. 4. RLCG Electrical Equivalent Model

The Fig. 4. Shows the RLCG components present in the circuit. Where R is the combination of TSV and Bump resistances, L is the combination of TSV and Bump Inductances, C is the combination of insulator and bump capacitances and G is the conductance of Silicon substrate. The top and bottom capacitors are the capacitances formed due to underfill material.

IV. SIMULATIONS AND RESULTS

The Electrical behavior of the above TSV model is analyzed by varying the height, diameter and pitch of TSV individually. The delay and power consumption values are examined from the above analysis. The variation in speed and power consumption is observed when the height of TSV is varied. As the height increased the delay and the power consumed by TSV also increased which has a huge effect on the overall performance.

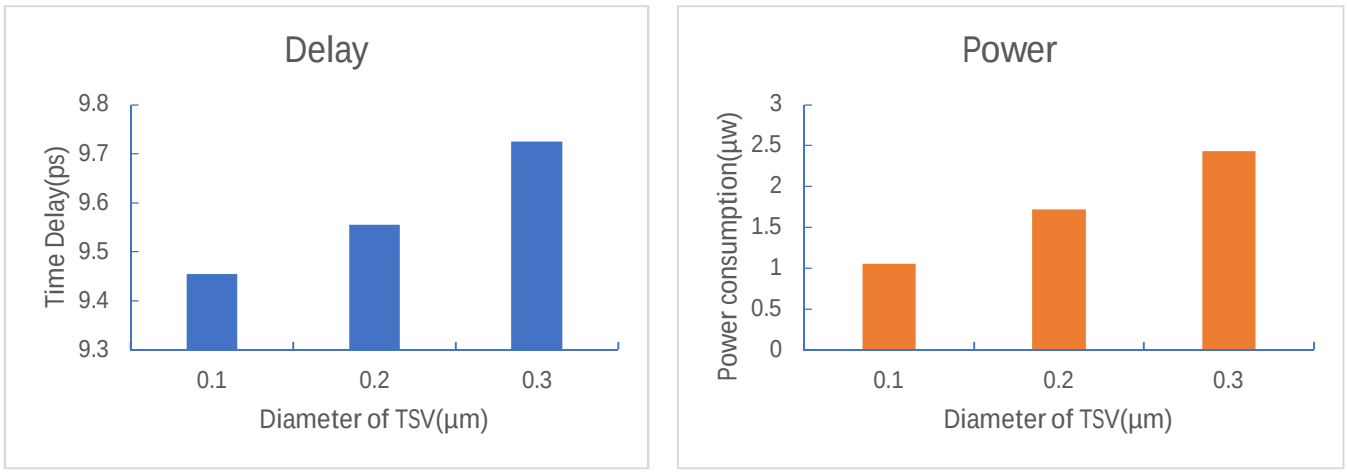


(a) (b)

Fig. 5. Graphical representation of (a)Delay and (b)Power at different heights of a TSV

The Fig. 5. Shows the impact of Height on delay and power. As the height is varied from 0.95 to 2.85 µm the delay and power also increased gradually.

The variation in speed and power consumption is observed when the diameter of TSV is varied. As the diameter increased the delay and the power consumed by TSV also increased but of very less amount which will have a slight impact on the performance.

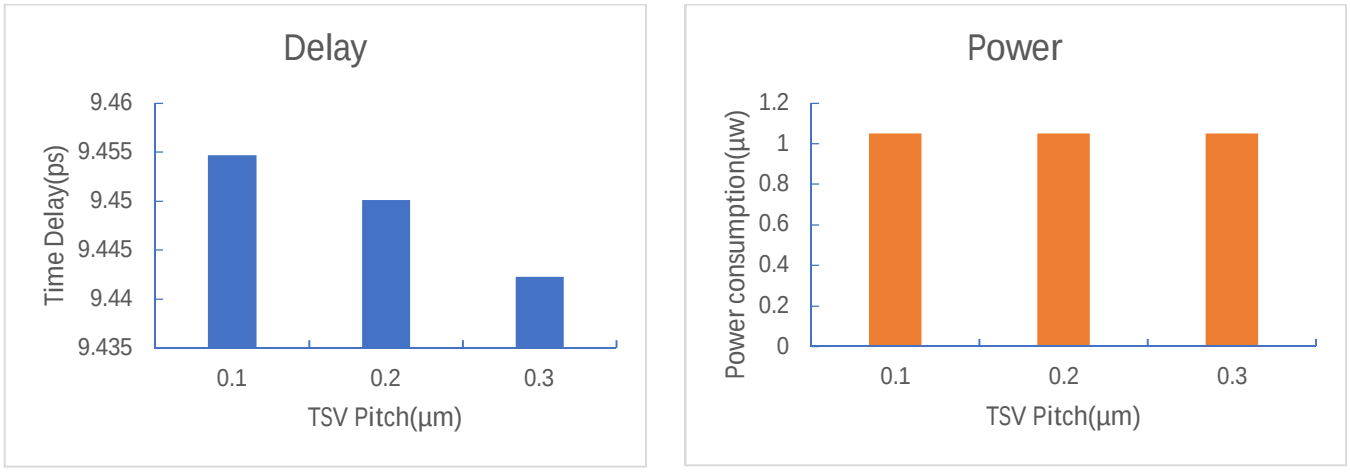


(a) (b)

Fig. 6. Graphical representation of (a)Delay and (b)Power at different diameters of a TSV

The Fig. 6. Shows the impact of diameter on delay and power. As the diameter is varied from 0.1 to 0.3 µm the delay and power are increased by having minor effects on reliability and performance.

The variation in speed is observed when the pitch of TSV is varied. As the pitch increased the delay is decreased but negotiable and the power consumed by TSV is constant among all the lengths.



(a) (b)

Fig. 7. Graphical representation of (a)Delay and (b)Power at different pitches of a TSV

The Fig. 7. Shows the impact of pitch on delay and power. Here pitch is the distance between TSVs. As the pitch is varied from 0.1 to 0.3 µm the delay is slightly reduced and the power is constant. From the above analysis this variation in pitch will not have any influence on the overall performance.

V. CONCLUSION

The Electrical Equivalent model for three coupled Through Silicon Vias (TSVs) was designed and studied the electrical behaviour of the designed model by varying the height, diameter and pitch parameters. The results of this analysis show that the height of TSV has major impact on the overall circuit that effects the total performance of the device. Whereas the other parameters have very slight impact but are considerable while using multiple TSVs.

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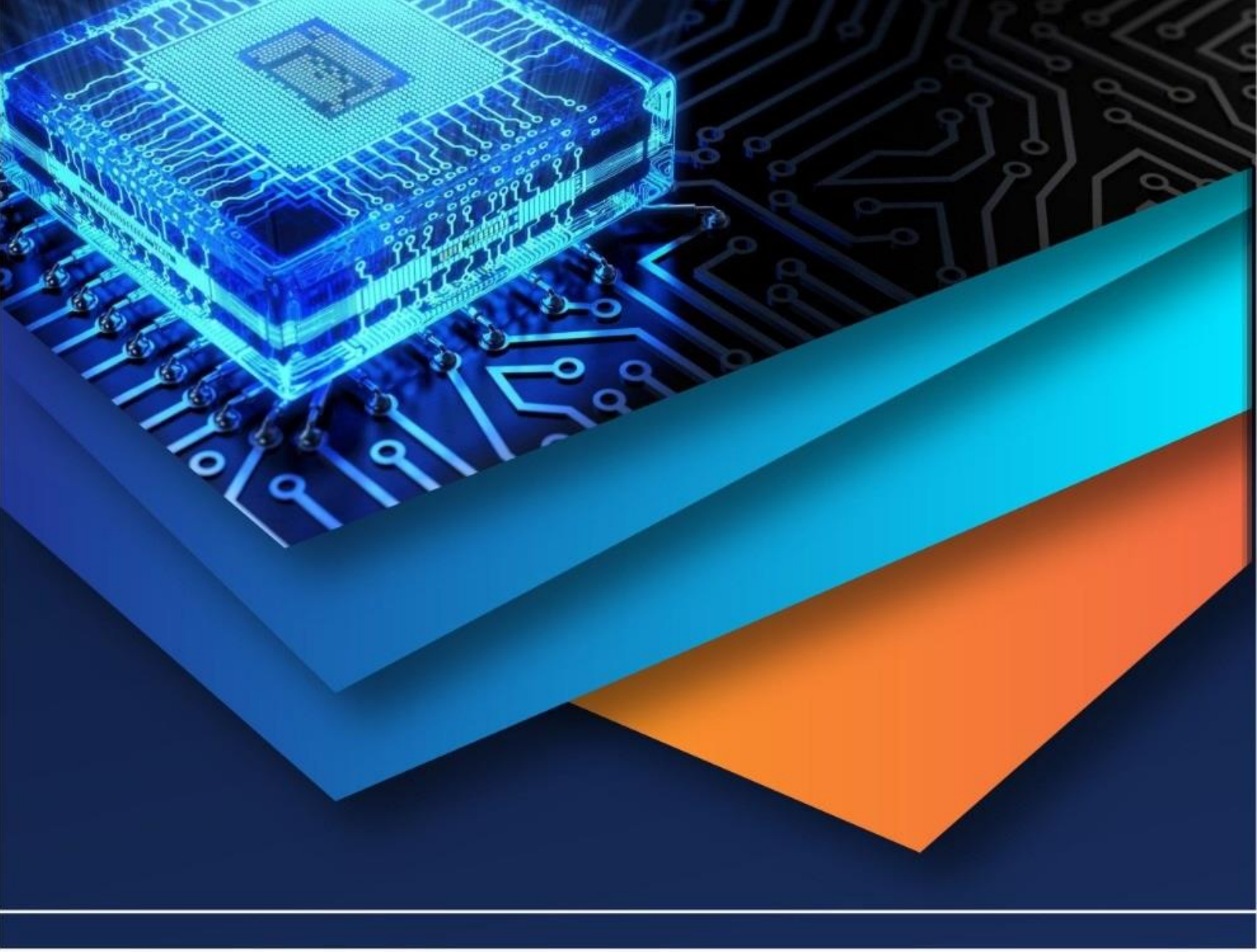

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