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High Speed Noise Tolerant Domino Circuit For Wide Fan-in AND-OR Gates

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Abstract: ***In this paper, a new technique is proposed for wide fan-in OR gates. Here the current comparison based domino circuit is used to design a low leakage, high speed wide fan-in circuit. Dynamic gates have been excellent choices in the design of high performance modules in modern microprocessors. Dynamic gates are indispensable for constructing wide high-speed OR and AND–OR gates in CMOS. They are especially useful in multiport memories, where single- ended read bit-lines are needed for compactness and (even) low-power consumption. Circuits implemented with dynamic logic have very low parasitic capacitance and the number of transistors required in this technique is very less compared to static CMOS logic. This wide fan-in OR gates are simulated using 14nm high performance predictive technology model demonstrate 60% power reduction and at least 2.41× noise-immunity improvement at the same delay compared to the standard domino circuits for 256-bit OR gates.***
Keywords: Domino logic, high-speed domino circuit, leakage power, noise tolerance, transistor sizing.

I. INTRODUCTION

Dynamic logic gates and circuits have been excellent choice in the design of high-performance modules such as multiple bit adders, subtractors, multipliers, comparators, multiplexers, registers, etc in modern VLSI microprocessors. The advancement in fabrication technology along with the shrinking device size has allowed for placement of nearly two billion transistors on Intel's latest processor . The digital logic gates and circuits designed using dynamic domino technique is considerably faster than the logic gates and circuits designed with standard static logic style. The aggressive technology scaling to improve the performance as well as the integration level makes the noise play a major role in design parameters like area, power and speed. Therefore the digital integrated circuit noise has become one of the most important issues in the design of deep submicron VLSI chips. The robustness and performance of wide fan-in dynamic circuits significantly degrade with increasing levels of process variations and sub threshold leakage. A number of design techniques such as PMOS feedback keeper transistor method to prevent the dynamic node floating problem, precharging the internal nodes to eliminate the charge sharing problem and weak complementary p-network is constructed to improve the noise tolerance to the level of skewed static CMOS logic gates, have been developed in the past three decades to minimize the effect of noise in dynamic circuits. It is also shown that voltage scaling aggravates the crosstalk noise in the dynamic circuits and reduces circuit noise immunity, motivating the need for noise-tolerant circuit design. To design a high performance domino logic circuit, there are two most important factors to be considered when designing a keeper circuit. The first factor is the additional loading caused by the keeper and its control circuits and the second factor is the keeper circuit should be capable of switching off very fast. If the keeper circuit remains ON during evaluation it will compete for longer time with the NMOS network during the pull down process. Designing feedback keeper circuit for wide fan-in gates is a challenging task since the leakage current largely depends on increase in variability. High fan-in compact dynamic gates are often employed in performance-critical units of microprocessors and other high-performance VLSI circuits. The use of wide dynamic gates is strongly impacted by reducing noise margins and increasing leakage currents in sub-14nm low- devices. Traditionally, dynamic floating nodes have been avoided by employing a static path through a pull-up and/or pull-down device referred "keeper". The increase in the variability and magnitude of the leakage current has become a major bottleneck in realizing such wide OR gates. Especially, in case of dynamic logic gates, the robustness of the dynamic node has to be guaranteed across different process corners without significant loss in the performance. In this paper, a 256-bit wide fan-in OR gate circuit is designed using current comparison based domino circuit. This technique reduced the parasitic capacitance at dynamic node. This type of domino circuits consists of an current mirror to replicate the leakage current of a dynamic gate pull-down stack and thus tracks process, voltage, and temperature. In this paper the effect of temperature on the circuit performance is analyzed in detail by sweeping the temperature from 25^0C to 70^0C. The performance of the dynamic circuits can be significantly improved by precise design and properly sizing the transistors. Usually in all the digital circuits the transistor gate length remains uniform. So the size of the transistor in digital circuits depends on the width of the transistor. In this paper the 256-bit wide fan-in OR gate domino circuit is implemented with L=0.014µm technology along with a supply voltage of 0.7V.

The paper is organized as follows. Section II details the circuit implementation and operation of the 256-bit wide fan-in OR gate using current comparison based domino techniques. Section III compares the performance of this circuit using the simulated results. Section IV concludes the paper.

A. Circuit Design

The circuit diagram of a wide fan-in OR gate circuit implemented using current comparison based domino (CCD) technique is shown in fig.1 and its layout is shown in fig.2. The wide fan-in OR gate circuit implemented using current comparison based domino (CCD) technique uses a current mirror to replicate the leakage current of the pull-up network and it tracks process, voltage, and temperature.

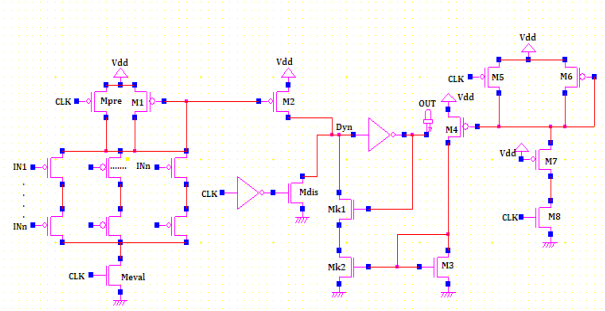

Fig.1.Wide fan-in OR gate using CCD

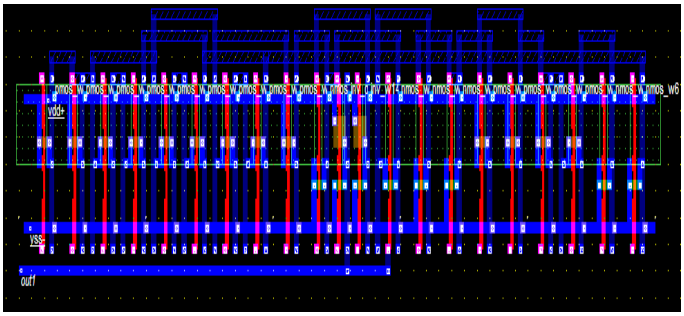

Fig.2. Layout of the wide fan-in OR gate circuit using current comparison based domino logic

The timing diagram of a 256bit wide fan-in OR gate is shown in Fig.3. The timing diagram shows output of the circuit. From this timing waveform, we know that CCD circuit must operate in two phases predischarge phase and evaluation phase. During the predischage phases clk=0. So dynamic node is fully discharged. So we get output as high. During evaluation phase clk=1. It has two state. First state, all inputs are high. When all inputs are high, it has some leakage current in its dynamic node. It can be eliminated using reference current circuit. In second state, one of the input flows to low. It cause dynamic node to charged fully to Vdd. So we get output as low.

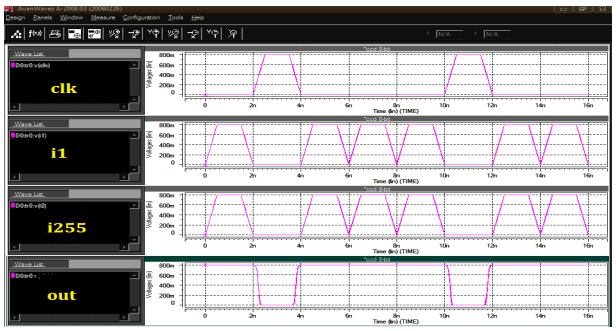

Fig.3 Timing diagram of the 256-bit wide fan-in OR gate using CCD

The Fig.4 shows, delay of 256 bit wide fan-in OR gate using CCD circuit. Delay varies depends on the temperature.

Temperature is main component of circuit. When the temperature increases gradually, delay of the circuit decreases. Because circuit get minimum amount of power. So it go to off stage.

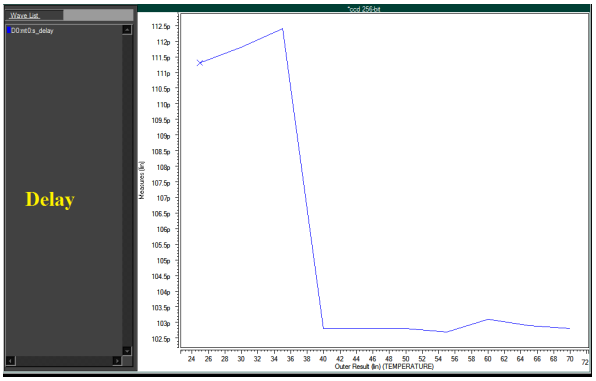

Fig.4 Delay Vs Temperature

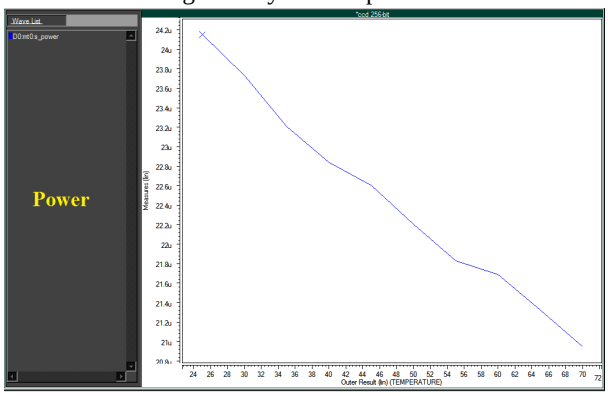

Fig.5 Delay Vs Temperature

The Fig.5 shows effect of temperature on the power consumption of the circuit. When temperature increases, power of the circuit decreases. So the circuit performance get reduced.

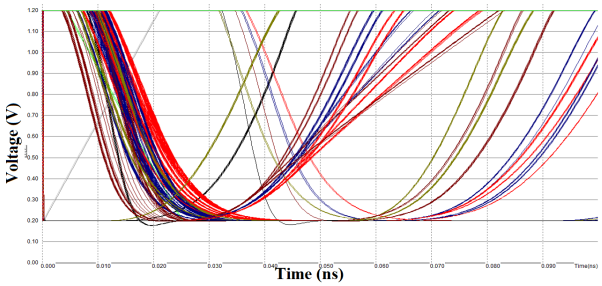

Fig.6 Voltage Vs Time waveforms of 256-bit wide fan-in OR gate using CCD

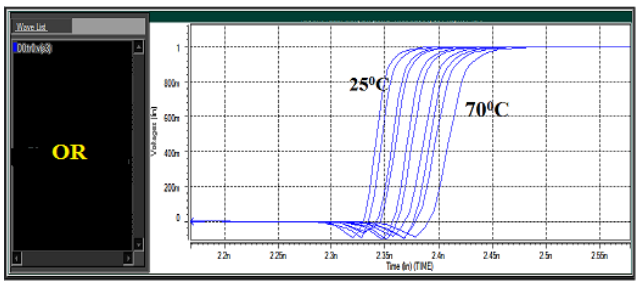

Fig.7 Effect of temperature on the performance of 4-bit adder using LCR

The output voltage Vs Time characteristic of the 256-bit wide fan-in OR gate is shown in Fig.6. This eye diagram shows the precharing and evaluation of the circuit. In this wide fan-in OR gate circuit a current mirror is connected to the keeper which

compensates for the sub threshold leakage current of the pull-down network. This current mirror circuit can be shared for all the logic gates in the circuit. In this configuration the keeper and current mirror circuit minimizes the delay of the circuit (delay in the order of pico seconds) by minimizing the effect of charge sharing. This circuit need proper selection of clock signal. If the clock frequency exceeds 500MHz, the performance of the 256-bit wide fan-in OR gate circuit degrades. The effect of temperature on the performance of 256-bit wide fan-in OR gate circuit is shown in Fig.7. In this work the temperature is varied from 25^0C to 70^0C. From the fig.8 it is clear that as the temperature increases the transition delay also increases due to the increase in leakage current. The circuit is implemented using L=0.014µm technology with V_{DD} =0.7V. The simulation results shows that the circuit performance is superior in terms of speed and power compared to the adder circuits implemented using standard static logic circuit techniques.

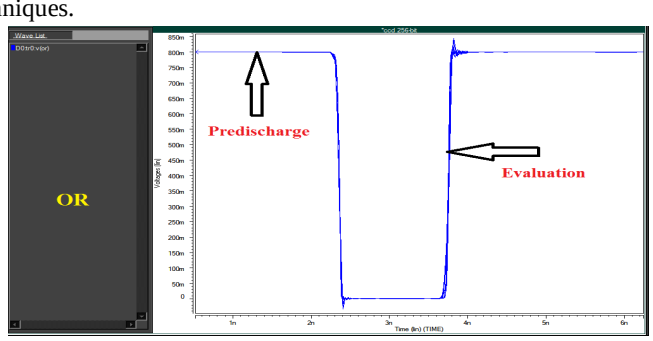

Fig.8 Voltage Vs Time waveforms of 256-bit wide fan-in OR gate using CCD

The pre-charge and evaluation phases of the OR(output) of a 256-bit wide fan-in OR gate circuit designed using CCD technique is shown in Fig.8. As the clock frequency increases the output voltage decreases due to the parasitic capacitances. The operation of the circuit is as follows. When clock goes low, the dynamic node will be predischarged to V_{DD} (predischarge phase) and the output remains high in this condition. When the clock signal changes the state from low to high the circuit evaluate the logic function (evaluation phase) and the output remains low.

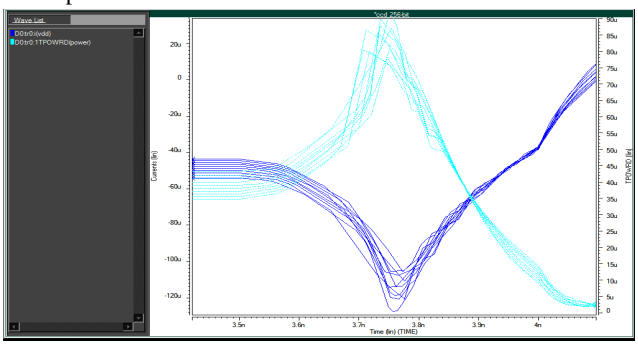

Fig.9 Power Vs Time waveforms of 256-bit wide fan-in OR gate using CCD

In Fig.9, the Power Vs Time waveform of 256-bit wide fan-in OR gate is shown. When Power is zero, the current is also zero. That means the circuit is in OFF state. When the circuit consumes small amount of power, the current in the circuit is also increases. The current is in negative because PMOS is operate in reverse biased region. The PMOs is operate in negative voltage only. That's why the circuit has negative current. In this paper 256bit wide fan-in OR gate is presented with L=0.014µm technology and with a supply voltage of 0.7V. These high performance domino styles improve the scalability of multiple bit domino logic gates. Using these method it is possible to implement the wide fan-in circuits with a transistor gate length of L=10nm along with a supply voltage of 0.7V. These wide fan-in circuits are superior in performance compared to conventional static logic wide fan-in OR and AND gates. These circuits minimize the chip area, minimize the leakage power, and improve the noise tolerance without much speed degradation. Also the delay between the gates is now reduced to the order of pico seconds. These types of domino logic circuits can be used in high performance microprocessors.

II.SIMULATION RESULTS

The simulations were performed using L=0.014µm technology along with the supply voltage V_{DD}=0.7V. In this paper a 256-bit wide fan-in OR gate is constructed using current comparison based domino circuit. In this type of circuit a single reference current is used to share reference current to all the transistor in the circuit. Since a single current mirror structure can be shared among more than one domino logic circuits, the CCD technique is useful for constructing wide fan in circuits such as multiple

bit adders, registers, multiplexers etc. The Fig.10 shows simulation result of wide fan-in OR gate using CCD technique. It shows voltage at the different node and output at predischarge and evaluation phase.

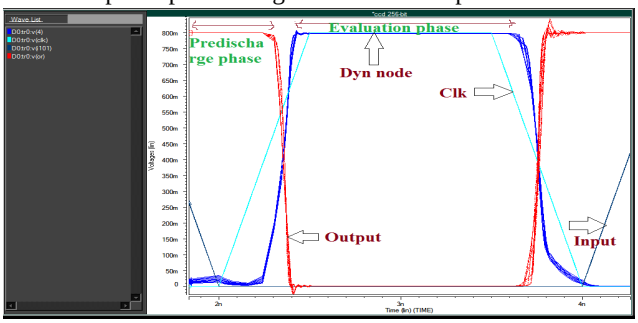

Fig.10.Simulation result

III. CONCLUSION

As the technology scales down, the leakage current of the pull down evaluation network increases, especially in wide fan in dynamic gates such as wide OR gates, wide AND-OR gates used in microprocessors. This will increase the power consumption and reduce the noise immunity. In this paper, the performance of 256-bit wide fan-in circuit designed using current comparison based domino circuit technique is analyzed in detail. The 256-bit wide fan-in OR gate circuit is simulated using L=0.014µm technology along with supply voltage V_{DD}=0.7V. The experimental results shows that these AND-OR gate circuits gives superior performance .

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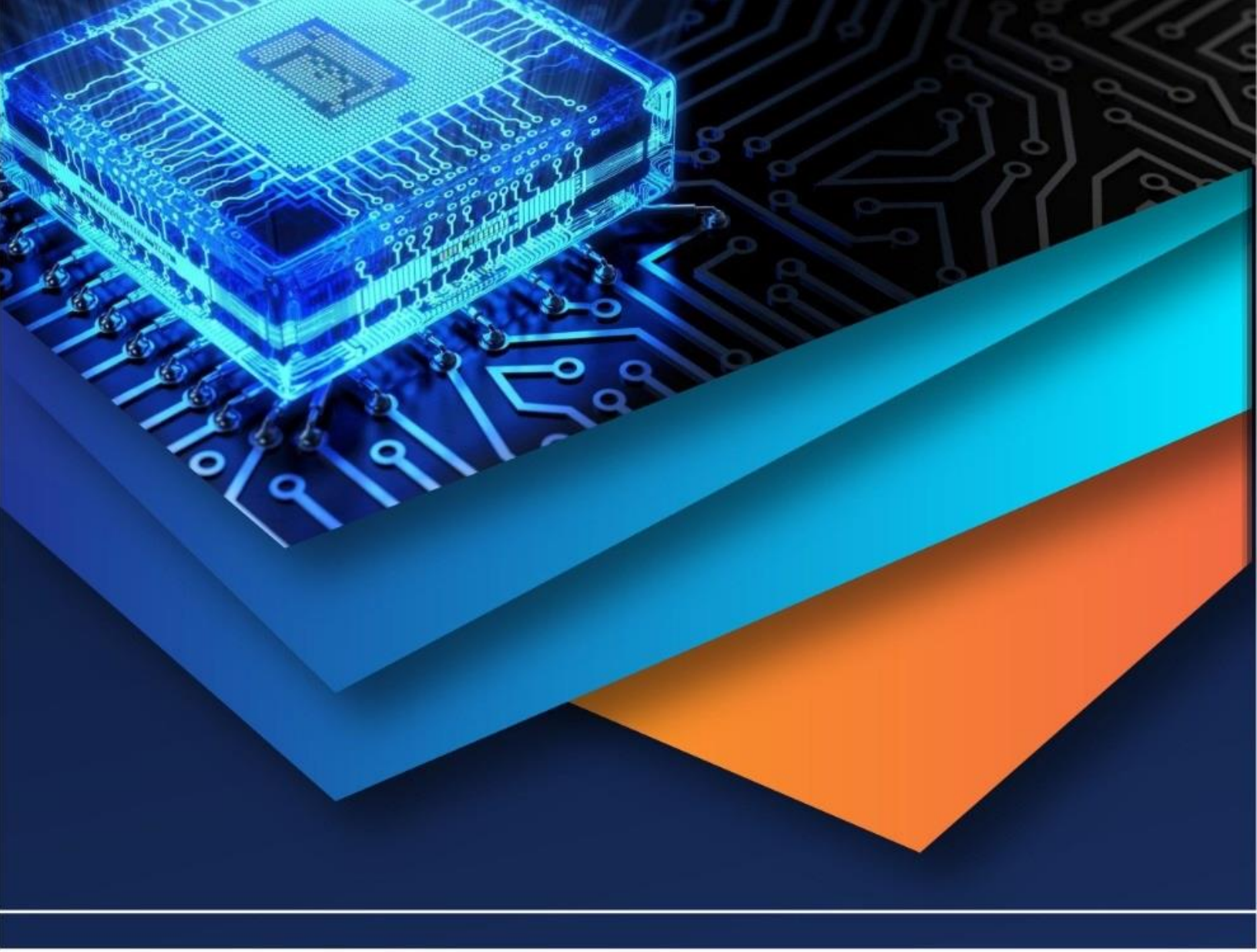

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