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38-42ghz CMOS Power Amplifier With Matched Co-Planar Strip Line

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Abstract- In this work, design of CMOS power amplifier (PA) with matched co-planar line for millimeter wave applications is proposed. This new design of CMOS power amplifier achieves high output power and power added efficiency with good matching. A 50Ω co-planar transmission line as a matching network is adopted in class AB PA for enhancement of efficiency. The circuit is simulated using 65nm TSMC CMOS technology in ADS tool. As shown by the simulation results: at 38-42 GHz under 1.5 V power supply, the output power is 19dBm while input power signal is 0dBm, the power gains more than 20dB of broadband within 38.5GHz to 41.8GHz, and the power added efficiency（PAE）is 74%.

Keywords— Coplanar strip line; Millimeter wave (MMW); CMOS power amplifier (PA)

I. INTRODUCTION

The extensively growth of CMOS devices in microwave based industries is establishing a new market opportunity. Good researchers are founding continuously new solutions which would be implemented into the existing wireless system networks to provide the wider bandwidth, the high quality and new added services. A millimeter wave (MMW) frequency band is the most promising technology for providing broadband wireless communications [1]. The extensive progress of CMOS technology has enabled its application in microwave and millimeter wave technologies. Presently, the CMOS technology has became one of the most attractive choices in implementing transceiver due to its low cost and high level of integration [2]. Despite of the advantages of CMOS technology, the design of CMOS transceiver in millimeter wave applications exhibits several challenges and difficulties that the designers must overcome. In addition, Kinetic performances of active devices with patch antenna have been improved, where MMW designs can be considered [3]. Power amplifier (PA) is an important unit of the wireless transceiver, so designing a high performance PA is the key to improve performance of wireless receivers [4]. However, the designing and implementation of CMOS PA is very difficult. Demands in different aspects of the PA require designers to consider comprehensively how indicators can compromise between one another. Today, several authors are designing a power amplifier using LC matching networks and to achieve maximum PAE of 50%. In [5], two stage class AB PA is designed for 3G applications and achieves PAE of 50%. In this work, Class AB PA is selected as it displays higher power efficiency as well as linearity. Single-ended two-stage amplification form is used in this design. In order to achieve more efficient match, co-planar line is adopted. This design has demonstrated a simple structure, but with high stability, as well as superior overall performance, which can be used as a transmitter for millimeter and microwave applications.

II. COPLANAR MICROSTRIP LINE DESIGN ANALYSIS

The co-planar line has become the best known and most widely used planar transmission line for RF and Microwave circuits. This popularity and widespread use are due to its planar nature, ease of fabrication using various processes, easy integration with solid-state devices, good heat sinking, and good mechanical support [9]. In this paper, we have design a co-planar line at 14 GHz with new dimensions and simulated in ADS tool. This design work taken a RT durroid substrate with thickness of t = 0.545 mm at the height h = 25mil above a lossless ground conducting layer. The dielectric between metal layers is assumed to have ϵ_r = 2.36 and tanδ = .002. At 14GHz, a 50Ω line given these parameters would have a width and length is 4mm and 0.9mm respectively and the calculated with help of equation is given below. The 3D view of line is shown in Fig.2. The resulting impedance bandwidth (S_{11}) -38.08dB with wideband of 4.5GHz in the ranging from 14GHz to 18GHz shown in fig. 1-3 respectively. The equivalent model of this coplanar strip line is shown in fig. 2.

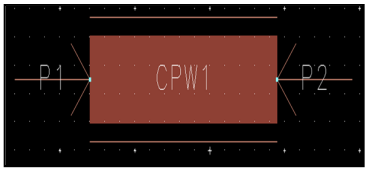

Fig.1 Geometry of the designed CPW

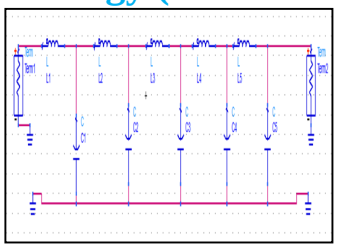

Fig.2 Equivalent circuit of the designed CPW

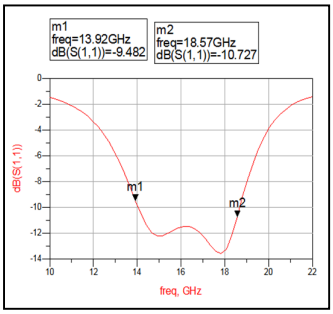

Fig.3 Return loss Vs frequency

III. POWER AMPLIFIER

Power amplifiers involve a balancing of many different parameters, including power added efficiency (PAE), maximum output power, linearity, maximum stable gain, power dissipation, stability, input/output matching, and breakdown voltage. As with many RF component designs, these requirements are often in conflict with one another. As the fulfill these requirements of PA design, different topologies like common source (CS), Common Gate (CG) etc. are available which are briefly discuss below.

A. CMOS Topology

The common source (CS) and common gate (CG) topologies are two popular architecture choices which are widely used for PA design. Common source structure is used in this circuit. Meanwhile, in order to achieve the gain of more than 20 dB, power amplifier use single-ended two-stage amplification form. Single-ended topology can be avoided application of the balanced-unbalanced transformer [6], which could simplify the integration process and improve the cost efficiency per unit of PA. For matching using LC networks as input and output achieves PAE up to 50% but if adopted 50Ω transmission line like micro-strip, CPW etc then it is possible to achieve PAE of 80%. In a co-planar line, conductor losses increase with increasing characteristic impedance due to the greater resistance of narrow strips. Conductor losses follow a trend that is opposite to radiation loss with respect to W/h. The power handling capacity of a co-planar is limited by heating because of ohmic and dielectric losses and by dielectric breakdown. An increase in temperature due to conductor and dielectric losses limits the average Power of the Co-planarline, while the breakdown between the strip conductor and ground plane limits the peak Power. In order to determine the optimum load, the transistor should have its input matched to the source using a co-planar line at the centre frequency of the operating band is connected to a variable load resistance at the output node.

B. Design Consideration

Fig.1 shows the basic schematic PA circuit, it includes bias circuit, input matching network, and output matching network and inter-stage matching network. A two-stage amplifier bias circuit is composed of DC power VGG1 and VGG2. The gate values of VGG1 and VGG2 are chosen as 0.6V. A suitable quiescent point is provided, so the amplifier works at the mode of Class AB. As shown in the figure, input and output ports have 50Ω impedance. The desired impedances are obtained with the help of matching circuits. The power amplifier takes a small-amplitude signal at the output RF frequency as its input and drives a high power representation of the input into a lower impedance load. Generally, the load is an antenna having a resistance of 50 ohm. The purpose of the power amplifier is therefore to amplify the high frequency signal to be sent by the transceiver. The PA should be able to amplify the signal to transmit signals at powers high enough for the receiver to recover the desired signal. Table1. Show the design specification of PA.

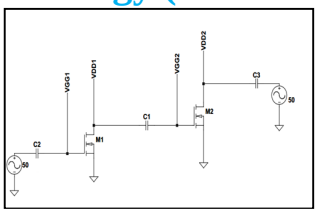

Fig.1 Basic Geometry of class AB power amplifier

Table1 Shows specifications and technology of MOS transistors

	Device Width (µm)	Length (µm)	Biasing (V)
M1	55	.065	1.5
M2	157	.065	1.5

IV. CIRCUIT DESIGN

A 38 GHz to 42 GHz two stage of CMOS PA is designed using 65nm commercial TSMC design kit in Agilent advanced design system. Fig6. Shows circuit schematic of PA. Parasitic capacitances of input and output RF bond pads are also considered in the circuit simulation. By improving the input matching, it is possible to achieve the maximum power efficiency, diminish signal distortions caused by reflection, and hence enhance linearity, further stabilize the circuit. T-circuit network is composed of C1, C2and CPW1, which could be achieved by using input impedance and source impedance (50Ω) match and achieves the good reverse isolation (S_{11}), is -34dB and 50Ω input impedance with the help of equation given below and its simulation results are shown in Fig.7 and Fig.8 respectively.

$$Zin = \frac{1}{g_m + jwC_{gs}} \quad (1)$$

$$S_{11} = 20.log_{10}\left(\left|\frac{Z_{in} - R_S}{Z_{in} + R_S}\right|\right) \quad (2)$$

The high pass L-type output matching network is composed of C4and CPW6, so load impedance of 50 Ω is transformed to the best load value, thus the required output power can be obtained. Selecting on-chip inductor is the key to design a matching network, because it determines the quality of the matching network. The inter-stage L-type matching network is composed by CPW4 of the first stage amplifying circuit and MIM (Metal-Insulator-Metal) capacitor C3 [7]. All dimension values of co-planar lines are CPW1, w=0.86mm L=4mm; CPW2, w=0.62mm L=2.5mm; CPW3, w=0.62mm L=2.5mm; CPW4 w=0.62mm L=2.5mm; CPW5, w=0.62mm L=2.5mm; CPW6, w=0.62mm L=2.5mm. The best power transmission is achieved by inter-stage matching between the first stage and the second stage. This matching network could also be used to adjust the amplifier gain flatness [8]. The maximum of S_{21} is reached nearby the centre frequency of 38 GHz to 42 GHz by adjusting capacitance, thus the best power added efficiency of 73% can be achieved that is shown in fig9 and fig10 respectively. The output power stops increasing after Pin=13dBm point. It is shown on the fig.11 at input power of 0dBm, output power Pout=11dBm.

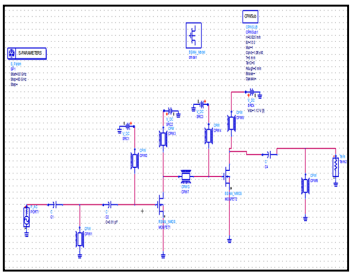

Fig.6 Complete design of receiver system at 38 GHz to 42 GHz

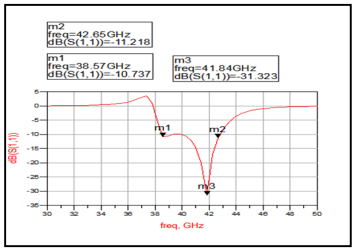

Fig.7 Return loss Vs frequency

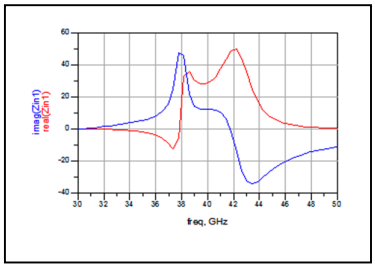

Fig.8 Input impedance Vs Frequency

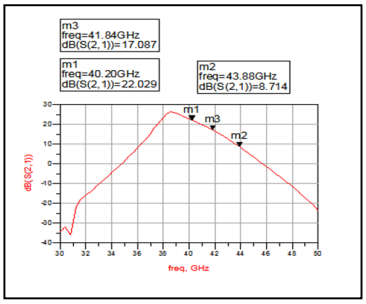

Fig.9 forward gain Vs Frequency

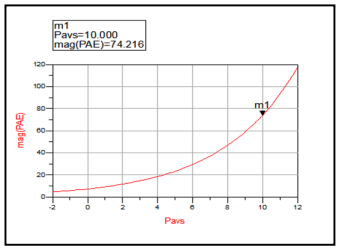

Fig10. PAE Vs Pin

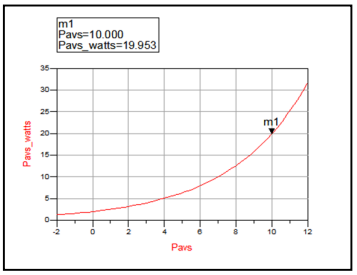

Fig.11 Pout Vs Pin

V. CONCLUSION

The CMOS PA is designed for MMW applications in this paper, based on TSMC technology. The single-ended two stages of PA are designed using 65nm CMOS process at 38 GHz to 42 GHz in this circuit. Performance standards are met for this new design technique. Simulation results of the designed circuit are shown that gain of 27dB, S_{11} of –33dB and PAE of 74% with the DC power dissipation of 25mW under 1.5 V power supply. The proposed method of PA using co-planar line in MMW applications increases the overall efficiency.

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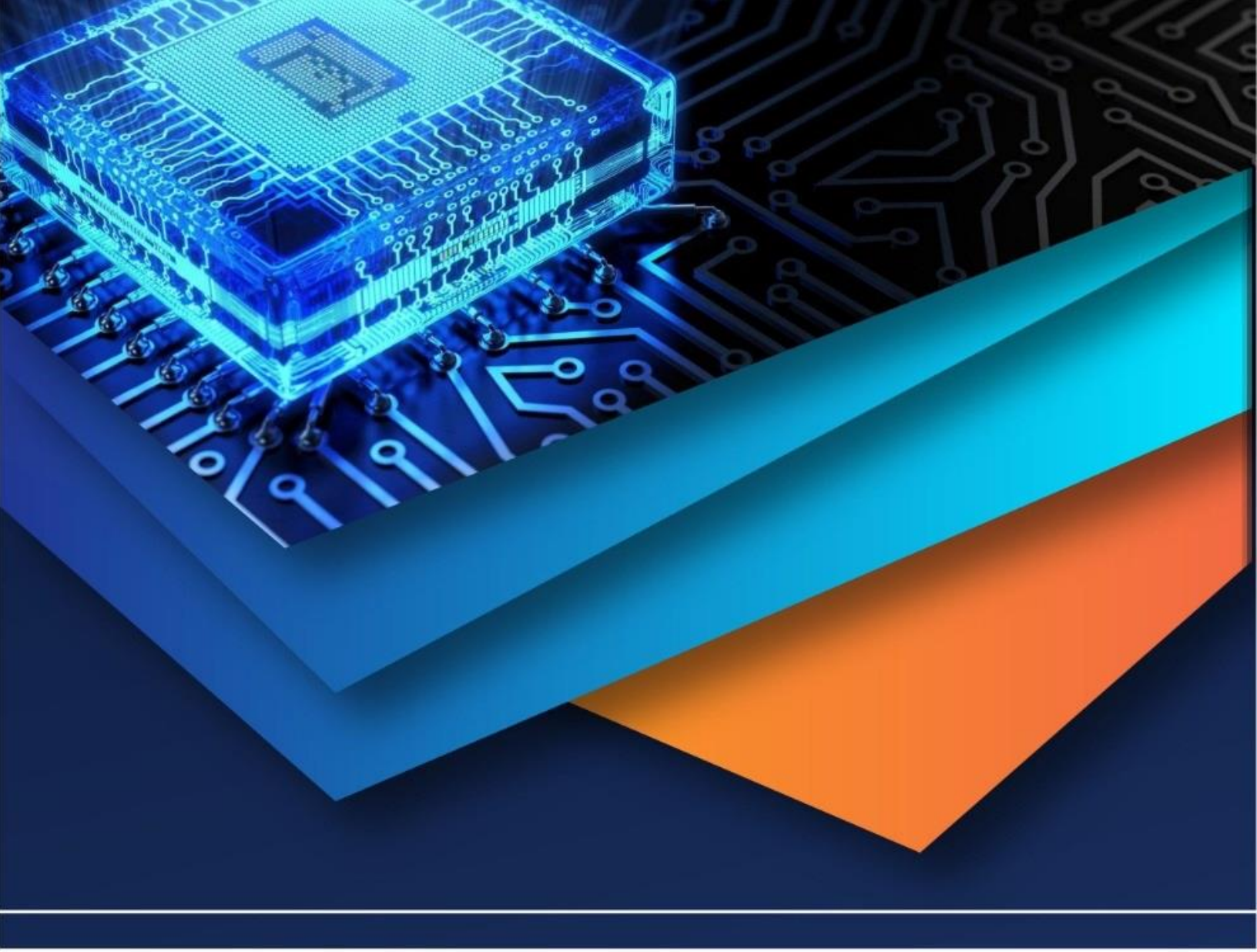

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