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Architecture of BIST for Memory Testing

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Abstract*: *Memories are the most essential component in all storage devices. Memory structure become complex when it is upgrading. Due to higher level of integration in memory size, manufacturing cost of the device is reducing and testing cost is increasing. Testing is needed to give the fault free products. Large number of bit pattern requires more time to test the circuit. Test algorithms are necessary to minimize the testing time. In this paper, the memory built-in self-test mechanism is represented for enhancing the functionality of the memory. The main motive behind the use of this technique is to smooth the progress of the memory for self-test. This is achieved with the help of an advanced method known as Built-in self-test architecture, March algorithm is also been utilized for the proficient fault coverage. The main intent of this paper is to reduce the whole test time and improve the yield by considering the economic circumstances as well.

Keywords*: *Built-In Self-Test (BIST), Test algorithm design, Complete linear feedback shift register (CLFSR), Memory, Test time.

I. INTRODUCTION

In a silicon die different types of memories can be fabricated and it is called as System on Chip. The advantage of SOC is low power consumption in computing market and it gives the efficient fault coverage for a targeted fault. RAM and ROM are the most common two different types of memories. Almost all memories having the property of random access .Volatile memory losses it stored data when the power to the chip is turned off but it is less expensive than non-volatile memory. Embedded memories will continue to dominate the increasing system on chip content in the near future, approaching 90% in some cases. A primary concern of digital IP provider is to develop the IPs and to make the IP usable for more years. Hence the memories are the most used IPs in modern SoC.

Therefore memory yield and eminence must have a dramatic impact on overall SoC price and outgoing product quality. At present, the area occupied by the embedded memories takes more than half of the total area of a typical system on chip and the ratio is expected to keep increasing in the future. To improve the yield, FIFO arrays are usually equipped with spare elements and external testers have been used to test the FIFO arrays and configure the spare elements. However, in the SoC environment, the overall test time is prohibitively increased if the test response data from the FIFO arrays are sent to the external testers. To achieve good quality there is a need for well understanding of memory design, modelling their faulty behaviours in a suitable and precise manner. The memories are more failure-prone than logic. So testing such embedded memory is a challenging task and is also very essential for the organized design.

II. LITERATURE SURVEY

In [1] the paper explains “An optimal algorithm for testing stuck-at faults random access memories” Which includes the identification of multiple stuck-at faults in Random access memories. It is an efficient algorithm for optimal test sequences. This correspondence presents an optimal algorithm to detect any single "stuck-at-I" "stuck-at-O" fault and any combination of "stuck-at-I," "stuck-at-O" multiple faults in a random access memory using only the n-bit memory address register input and m-bit memory buffer register input and output lines.

It is shown that this algorithm requires 4 X 2n memory accesses. In [2] the paper explains Implementation of Random number generator using LFSR for high secured multi-purpose applications. In ancient time the random numbers are generated with the help of software later it moves towards hardware.

The generated random numbers are very useful in circuit testing. In [3] the paper presents “Realistic built in self test for static RAMs Design and test of computers” explains specification and design of a self-test mechanism for static random-access memories (RAMs).

The test algorithm provides excellent fault detection, and its structure is independent of address and data scrambling. The self-test machine generates data backgrounds on chip and is therefore suitable for both bit-oriented and word-oriented SRAMs. It is also suitable for both embedded SRAMs and stand-alone SRAMs, and adapts to boundary-scan environment. Because of the regular and

symmetric structure of the test algorithm, the silicon overhead is only 3% for a 16 K synchronous. In [4] the proposed system explains about the implementation of configurable linear feedback shift register (CLFSR) in VHDL and evaluates its performance with respect to logic, speed and memory requirement in FPGA. Behavioural implementation of CLFSR in VHDL is configurable in term of number of bits in the LFSR, the number of taps position of each in the shift register stage and seed value of LFSR.

III.PROPOSED DESIGN METHODOLOGY

A. BIST Architecture

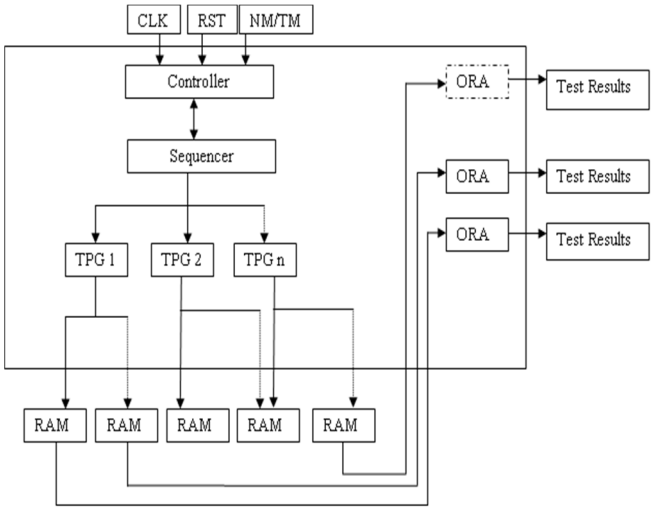

Fig. 1 Proposed BIST architecture

B. M BIST Architecture

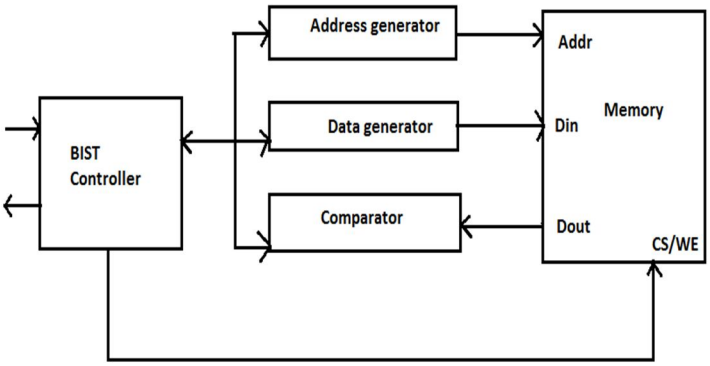

Fig. 2 Proposed MBIST architecture

The Proposed model consists of BIST Controller, Memory under test and Comparator blocks. BIST Architecture is being utilized for testing of the circuit. The BIST controller manages the operation of BIST in both normal mode and Test mode. Whenever the BIST signal is active high the controller proceed its operation in BIST mode. Whenever the BIST signal is active low controller will be allowed to perform the normal mode operations.

In the BIST mode sequence activation signal is sent to the sequencer, once it receives the activation commands from the controller--the sequencer starts generating the signals for the test pattern generator. March testing takes a significant impact on this architecture by declining the overall faults. CLFSR is being utilized for the generation of both test vector and addressing sequences and is given to the memory cores. Output response analysis is done to check the test result.

While testing the memory different types of faults model occurs. One should also need to care about the fault models during the selection of an algorithm. March C- Algorithm is chosen for the efficient tests of memory because it covers the stuck-at, transition, coupling faults as well. With this, the fault coverage will be more resulting in good product quality. Different types of March algorithms are presented in the below table.

Name	Algorithm
MATS	{↕(w0);↕(r0,w1);↕(r1)}
MATS+	{↕(w0);↑ (r0,w1);↓(r1,w0)}
MATS++	{ ↕ (w0);↑ (r0,w1); ↓ (r1,w0, r0)}
MARCH X	{ ↕(w0);↑ (r0,w1); ↓ (r1,w0);↕(r0)}
MARCH C-	{ ↕(w0); ↑ (r0,w1);↑ (r1,w0); ↓ (r0,w1); ↓ (r1,w0);(↕ r0)}
MARCH A	{ ↕ (w0); ↑(r0,w1,w0,w1); ↑(r1 ,w0,w1);↕(r1,w0,w1,w0); ↑ (r0,w1,w0)}
MARCH Y	{ ↕ (w0); ↑ (r0,w1, r1); ↓ (r1,w0, r0);↕(r0)}
MARCH B	{ ↕ (w0);↑ (r0,w1, r1,w0, r0,w1); ↑ (r1,w0,w1); ↓ (r1,w0,w1,w0);↓ (r0,w1,w0)}

Table 1 Different March Algorithms

IV. EXPERIMENTAL SETUP AND RESULT

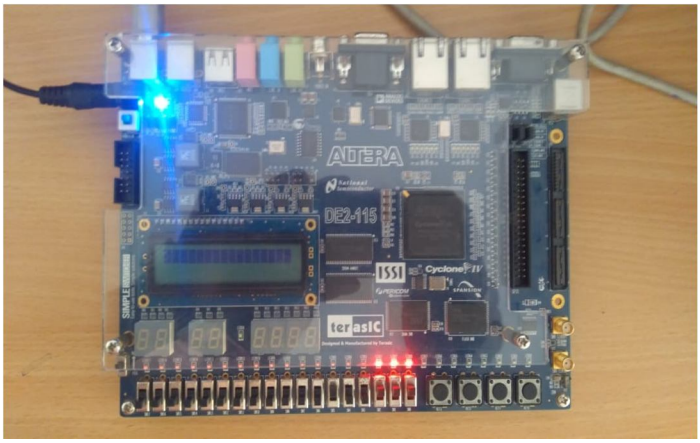

Fig. 4 Experimental setup of proposed system

The Simulated result of the proposed BIST scheme is illustrated here. Xilinx 14.2 is used for synthesis and simulation of the proposed architecture. For implementation purpose Cyclone 4 FPGA is used. For testing purpose March C- algorithms are utilized. The RTL view of the proposed BIST architecture is shown in the figure below.

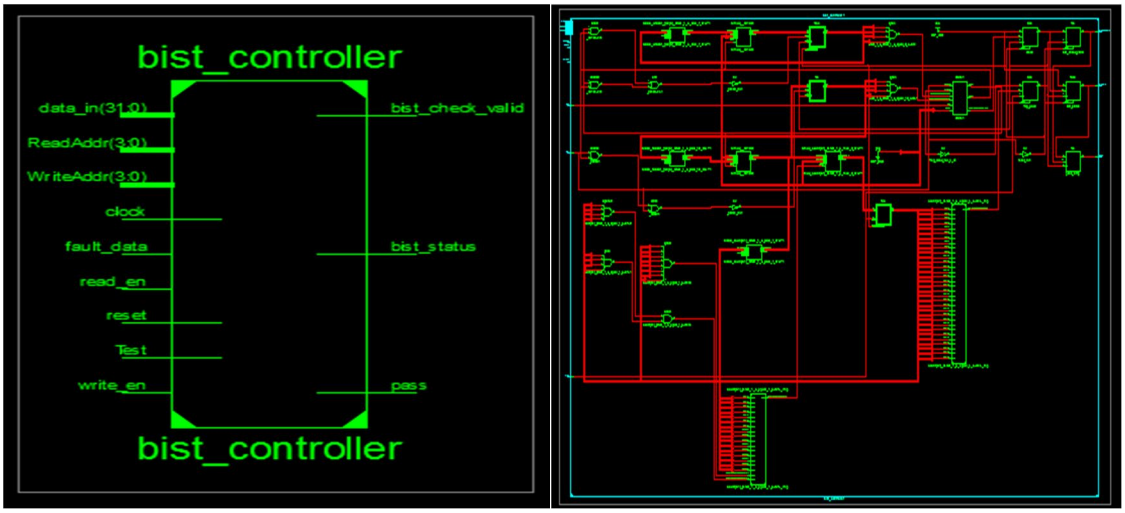

Figure 4 RTL schematic of proposed BIST scheme

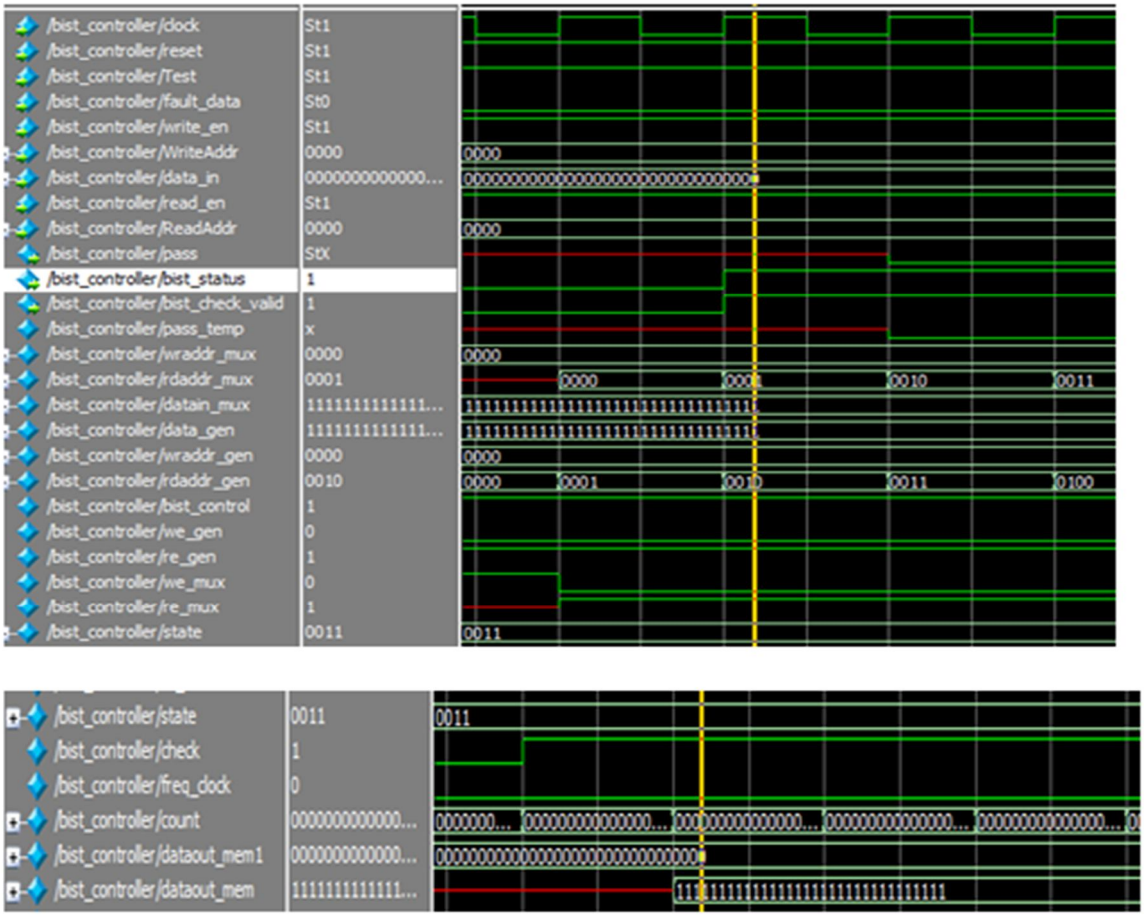

Figure 5 Simulation Result Of Addr_4_Test_1 Output

V. CONCLUSION

This paper has discussed the strong architecture of BIST for memory testing considering the fault models, intending to provide a good quality product, ease of testing, high time to market. March C- algorithm takes over the part in detecting maximum faults. Configurable CLFSR design reduces the hardware complexity. The detected faults are been discussed in Experimental Results.

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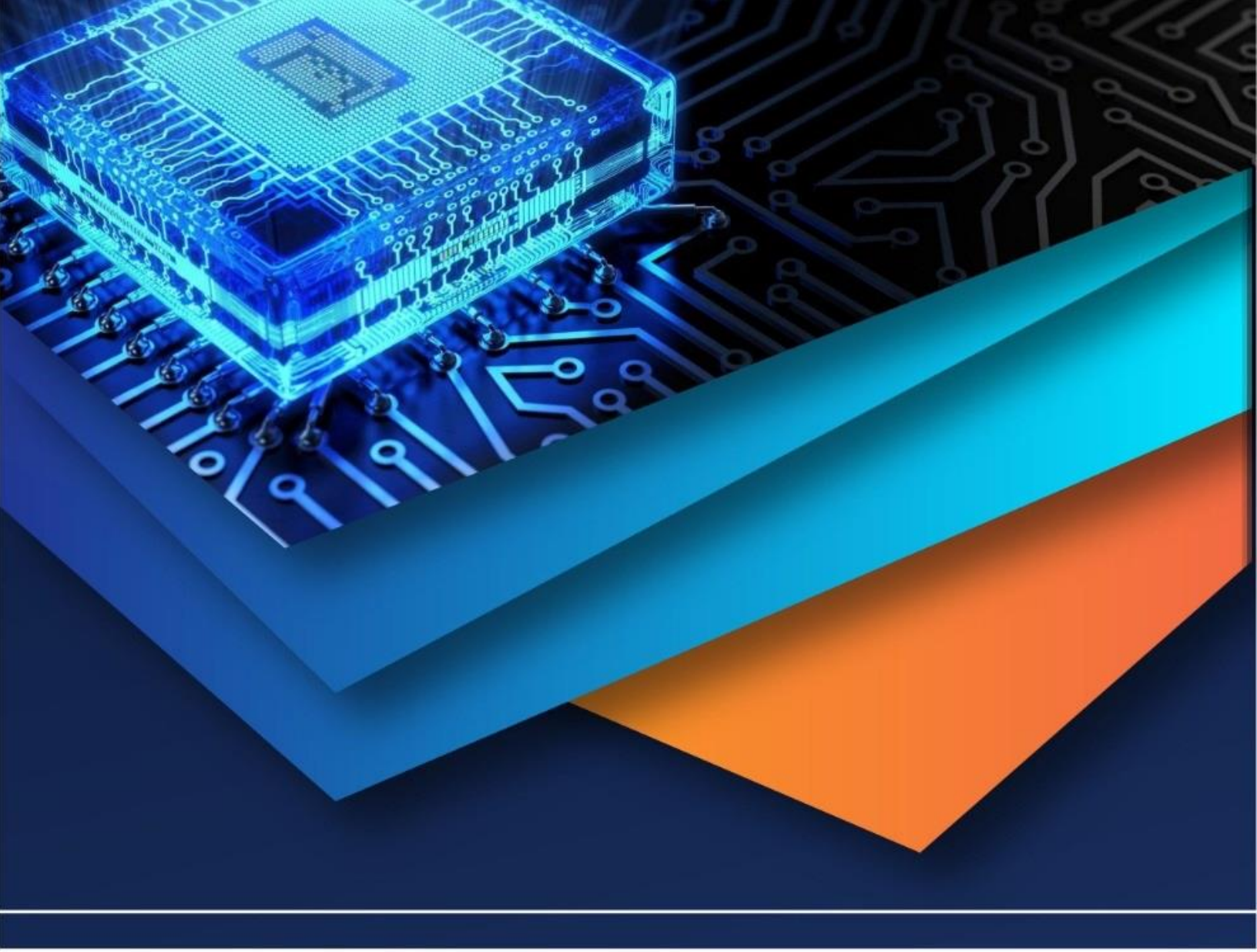

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