iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 7 **Issue:** X **Month of publication:** October 2019

DOI: http://doi.org/10.22214/ijraset.2019.10050

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.177
Volume 7 Issue X, Oct 2019- Available at www.ijraset.com

Design of Router 1X3 using HDL

Supriyareddy Patil[1], Dr. Baswaraj Gadgay[2]
[1]*PG Student Dept. Of VLSI Design & Embedded Systems VTU Centre for PG studies, Kalaburagi, Karnataka, India*
[2]*PG Co-ordinator /Regional Director VTU Centre for PG Studies, Kalaburagi, Karnataka, India*
[3] *Assistant Professor VTU Centre for PG Studies, Kalaburagi, Karnataka, India*

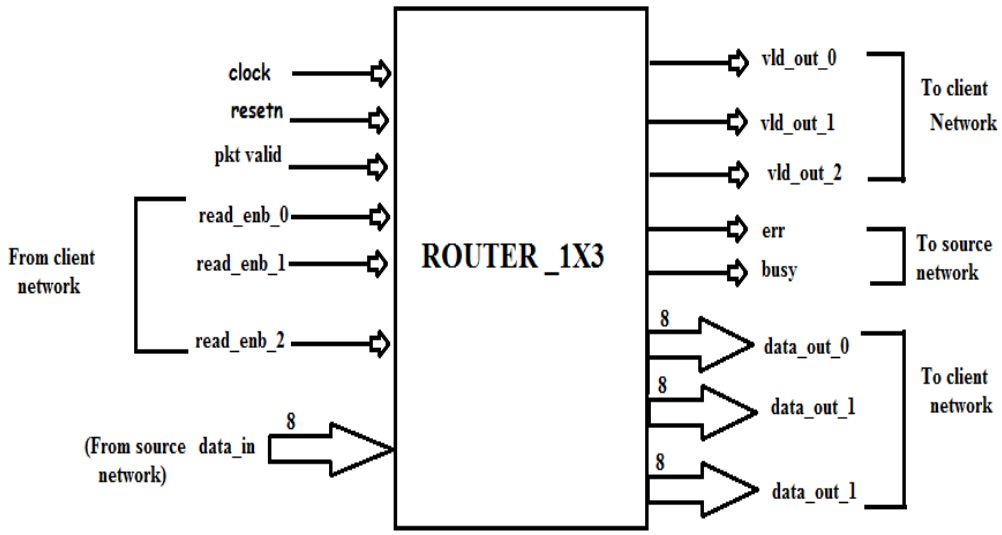
Abstract: Routing will enable to pass the message from one computer to another computer based upon the IP addresses. Router is a device which forwards the information between different computer networks i.e. transferring the information from source to the destination. The router can be connected to LANs (Local area networks) or WANs(wide area networks).It will perform the traffic directing function and it reads the network address information in the packet header to determine the ultimate destination Router drives the incoming packet which comes from the input port to output ports based on the address contained in the packet. In this paper we have designed the router which will send the information to three different networks and it consists of several components like FIFO (first in first out), register, synchronizer, FSM(Finite state machine).
Keywords: Hardware description language (Verilog), Router, Xilinx, Data.

I. INTRODUCTION

A router is connected to three or more data lines which will forward the data packets between different networks using the information, it will directs the packets to the next network. When the information comes on the network lines, the device will read the address to find is ultimate destination .Until the data reaches to the destination node it will forward the data packets from one router to the other router through the internet. A router is a device that forwards data packets along networks. It drives an incoming packet to an output channel based on the address fields contained in the packet header. Routers use headers and forwarding tables to determine the best path for forwarding the packets, and they use protocols to communicate with each other and configure the best route between any two hosts. It is an OSI layer 3 routing device. When multiple routers are used in interconnected networks, the routers can exchange information about destination addresses using a routing protocol.

II. ROUTER 1X3

Block Diagram Of Router –Top Level RTL Module



ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.177
Volume 7 Issue X, Oct 2019- Available at www.ijraset.com

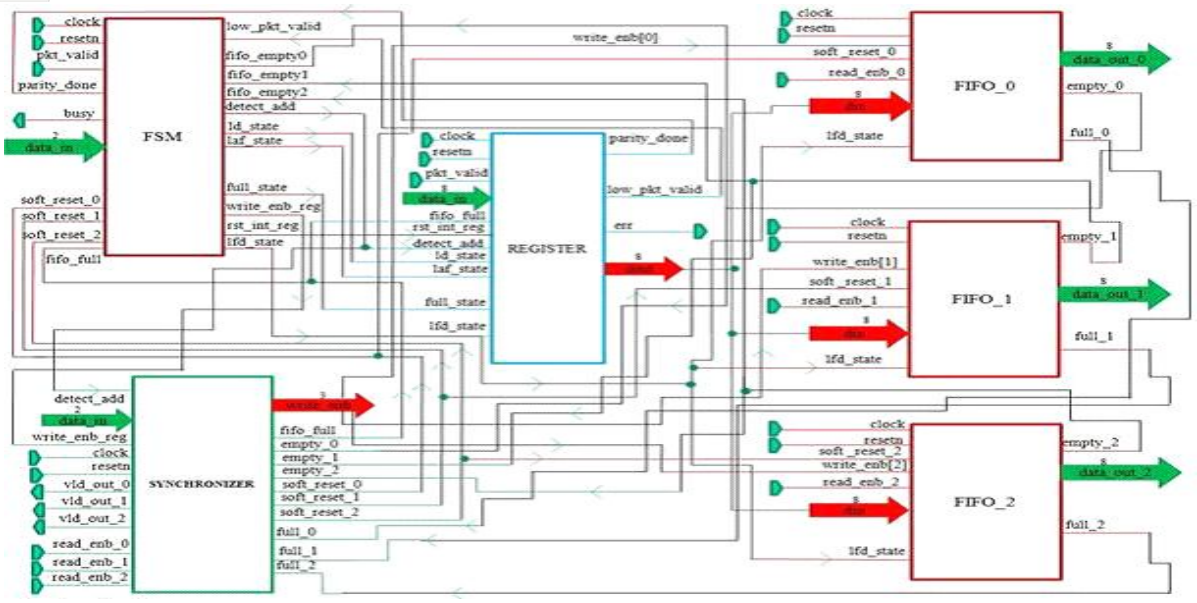


Figure 1

In this design router consist of six important components, which are as follows

Register, FIFO(first in first out), synchronizer ,FSM(finite state machine) .In this project FSM works like a controller which will provide the control signals to the FIFO, and register block.

1) *FIFO Block:* Each fifo is of 9 bit wide and 16 bit depth. There are 3 fifo in router design, Based on the control signals provided by the FSM block, FIFO will store the data coming from the input port. If resetn is low then full =0, empty = 1 and data_out = 0. For Write operation: The data from input data_in is sampled at rising edge of the clock when input write_enb is high and fifo is not full.For Read Operation: The data is read from output data_out at rising edge of the clock, when read_enb is high and fifo is not empty. read and Write operation can be done simultaneously. Full – it indicates that all the locations inside fifo has been written. Empty – it indicates that all the locations of fifo are empty.
2) *Synchronizer Block:* This block provides synchronization between FSM block and three FIFOs so that single input port can communicate with 3 output ports. This module provides synchronization between FSM and FIFO blocks.. It will detect the address of channel and will latch it till pkt_valid is high, address and write_enb_reg will be used for latching the incoming data into the FIFO. fifo_full output signal is generated, when the present FIFO is full, and fifo_empty output signal is generated by the present FIFO when it is empty.

If data = 00 then fifo_empty = empty_0 and fifo_full = full_0
If data = 01 then fifo_empty = empty_1 and fifo_full= full_1
If data = 10 then fifo_empty = empty_2 and fifo_full = full_2 Else fifo_empty = 0 and fifo_full = 1.

The output vld_out signal is generated when empty of present fifo goes low, that means present fifo is ready to read. vld_out_0 = ~empty_0 vld_out_1 = ~empty_1vld_out_2 = ~empty_2 .The write_enb_reg signal which comes from the fsm is used to generate write_enb signal for the present FIFO which is selected by present address.There are 3 internal reset signals (**soft_reset_0**, **soft_reset_1, soft_reset_2**) for each of the FIFO respectively. The respective internal reset signals goes high if **read_enb_X** (**read_enb_0**,**read_out_1**,**read_out_2**) is not asserted within 30 clock cycles of the **vld_out_X**(**vld_out_0**,**vld_out_1** or **vld_out_2**) being asserted respectively.

3) *FSM:* The 'fsm_router' module is the controller circuit for the router.This module generates all the control signals when new packet is sent to router. These control signals are used by other modules to send data at output, writing data into the fifo.
4) *Router_Reg:* The router_reg module contains the status, data and parity registers for the router_1x3.These registers are latched to new status or input data through the control signals provided by the fsm_router.This module contains status, data and parity registers required by router.All the registers in this module are latched on rising edge of the clock.Data registers latches the data from data input based on state and status control signals, and this latched data is sent thefifoor storage. Apart from it, data is also latched into the parity registers for parity calculation and it is compared with the parity byte of the packet. An error signal is generated if packet parity is not equal to the calculated parity

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.177
Volume 7 Issue X, Oct 2019- Available at www.ijraset.com

III. SIMULATION RESULTS

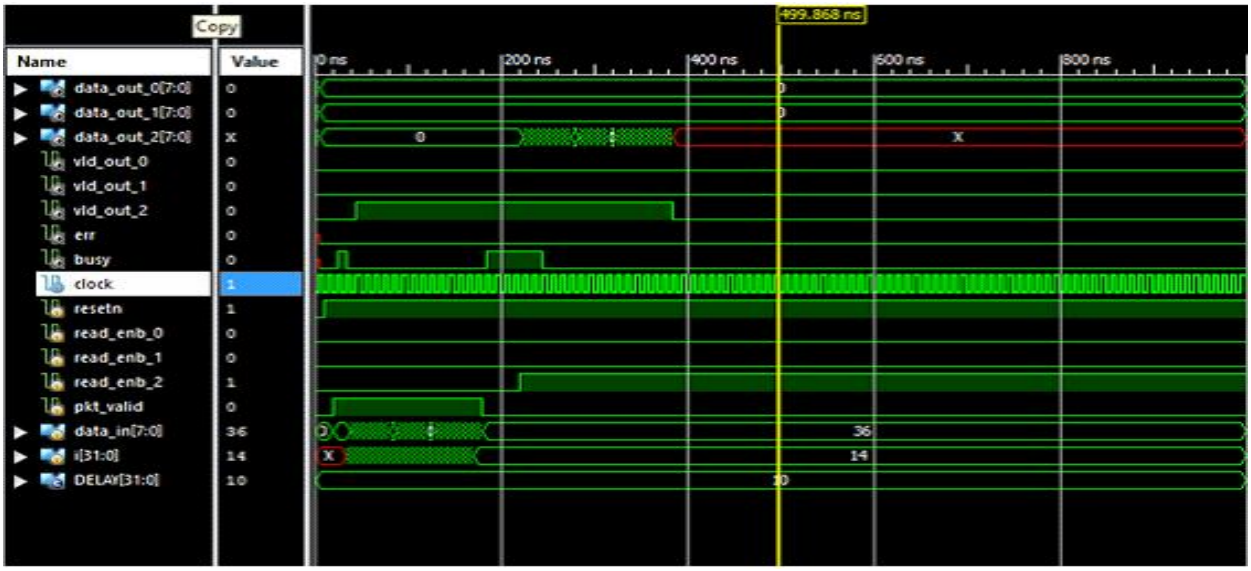


Figure 2 Router Top Module Output

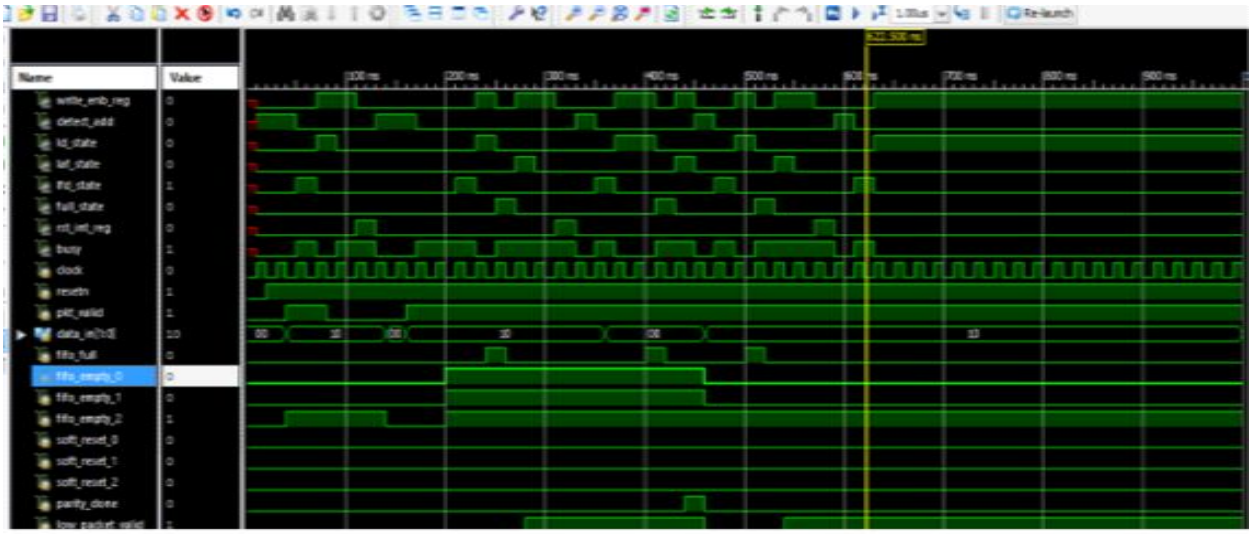


Figure 3 Router FSM Module Output

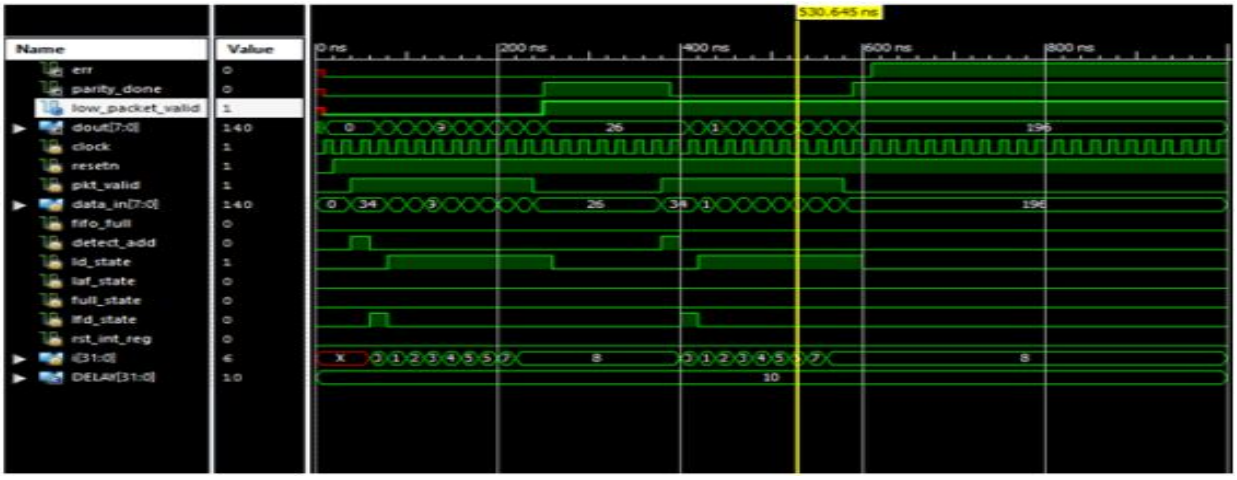


Figure 4 Router Synchronizer Module

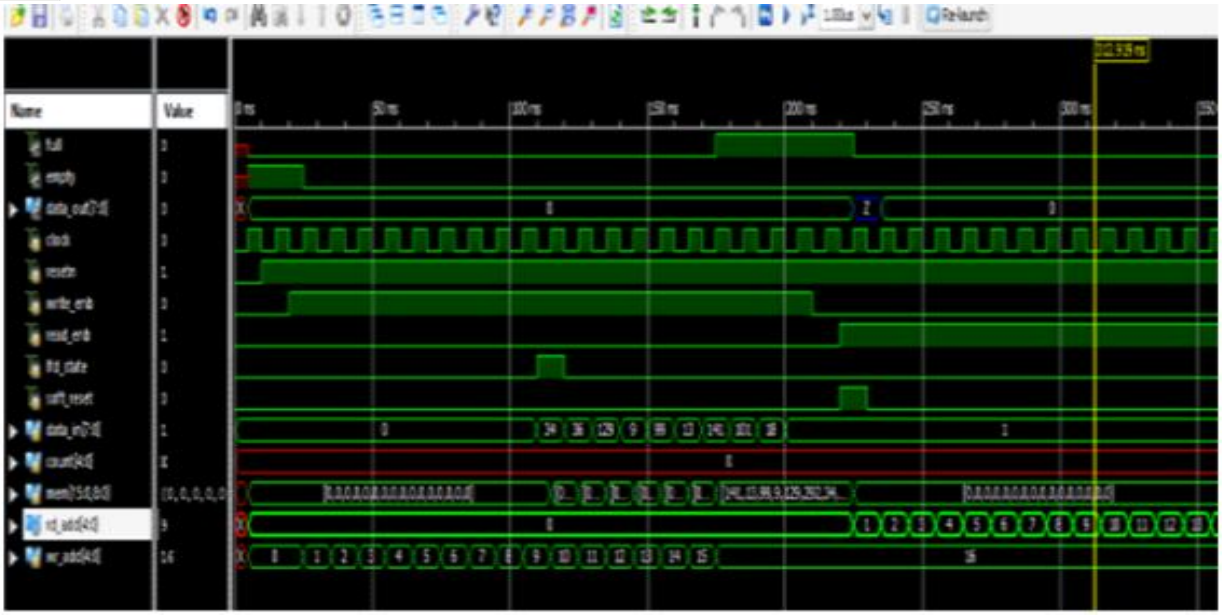


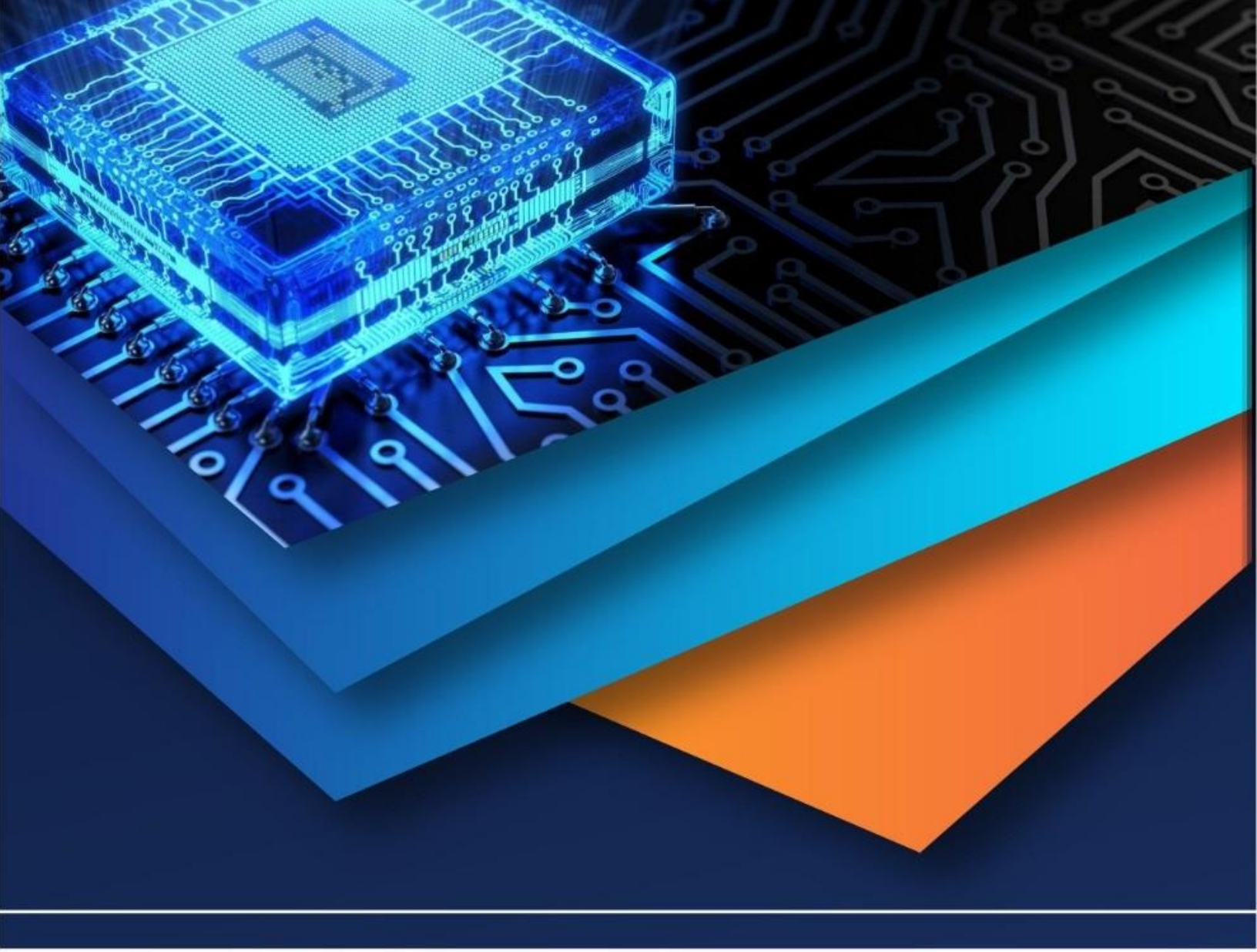
Figure 5 Router Fifo Module

IV. CONCLUSION

This paper is intended to present an overview of the design of router 1x3 and successfully we have designed all the components of router like fifo(first in first out),synchronizer,register,fsm(finite state machine).

REFERENCES

[1] Verilog HDL:- Samir Palnitkar
[2] System Verilog:- Chris Spear
[3] The ASIC Website
[4] https://en.wikipedia.org/wiki/Wireless_router
[5] opencores.org



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY