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Effect of Parasitic Inductance on Inverter Module Performance

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Abstract— Effect of circuit parasitic inductance is an important consideration in application and characterization of Insulated Gate Bipolar Transistor Module (IGBT). Higher value of parasitic inductance causes higher voltage overshoot peak. This paper demonstrates how the performance of the half H-bridge IGBT inverter module is affected by it. Comparison of $V_{ce(peak)}$ values of IGBT modules having different Stray inductance is done for analysis purpose. Simulation results show the effectiveness of our approach.
Keywords— Semiconductor Devices, IGBT Characterization, Parasitic Inductance, Voltage Overshoot Peak, Double Pulse Measurement

I. INTRODUCTION

IGBT has become a very important power electronics device used in many industrial fields because of having the advantages like short switching time and low power loss, [1][2]. The crucial way to successfully use these improvements to their maximum advantage, in particular the faster switching speed, requires careful attention to parasitics present in the system; mainly stray inductance and capacitance which are normally unwelcomed for IGBT modules.

This paper provides an instinctive understanding of these increased parasitic effects. The effects of parasitic inductance and capacitance include current and voltage overshoot as well as ringing. These stray elements are always present. Faster switching speeds at high voltages and current causes higher dv/dt and di/dt. This voltage drop across stray inductance whose value is in nanohenries can be problematic. This paper addresses these concerns and explains the initial characterization of typical IGBT module.

A. Parasitic Inductance

When a current passes through conductor it creates a magnetic field which produces an inductive effect. This unintended inductance is called parasitic inductance. It can interrupt the usual flow of current in circuit. The voltage drop across this inductance can be expressed as,

$$V = Ls*(di/dt)$$

If di/dt is high then, voltage drop across parasitic inductance can be notable.

II. DOUBLE PULSE MEASUREMENT

Fig.1 shows basic circuit diagram of Double Pulse Measurement. This method is used to measure the switching energies, turn-on and turn-off power loss, and conduction loss of power electronics devices (Transistor and freewheeling diode) at different voltage and current levels [1]. Fig.2 shows typical waveforms for gate, current and voltage. Inductor, L is connected as load across the off switch (T_2). Double pulse is applied to gate terminal of transistor, T_1. The two pulses are made by short pulse following the long pulse. Time period of the pulse depends on the current on which inverter is driven.

A. Circuit Operation

When first turn-on pulse is given, current across IGBT and load increases. Turning-off pulse will make current in load to free wheel through diode, D_2. Because turn-off pulse time is very small current across load seems linear. When second turn-on pulse is given, current overshoot occurs and at second turn-off pulse voltage overshoot occurs.

III.SIMULATION AND RESULT

Simulation is done using PSIM (Power Simulation) software. The simulation circuitry for top IGBT of half H-bridge inverter is shown in Fig.3. The values taken into the consideration for the experiment are listed in Table I. The chosen IGBTs are ideal one. To make sure about result soundness and exactness two identical IGBT modules in total were measured at same test condition and results were compared. Fig. 4(a) - Fig. 4(d) represents simulation waveform of gate pulse (V_g), collector current (I_c), load current (I_l) and collector-emitter voltage (V_{ce}) respectively. Fig.5 shows the voltage overshoot peak waveform of both modules. As we can see that increase in stray inductance, increases the voltage overshoot peak value. The peak values are tabulated in

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Table II.

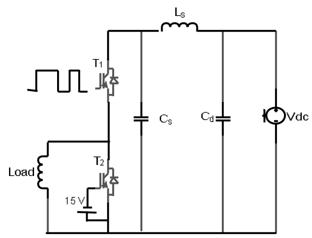

Fig. 1 Basic circuit diagram of double pulse measurement

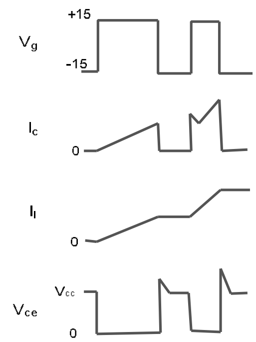

Fig. 2 Basic waveforms of double pulse measurement

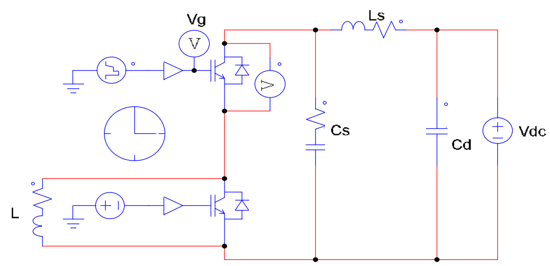

Fig. 3 Simulation Circuit

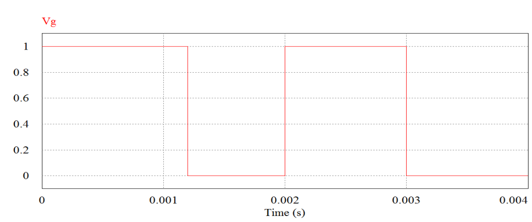

Fig. 4(a) Gate Pulse (V_g) Waveform

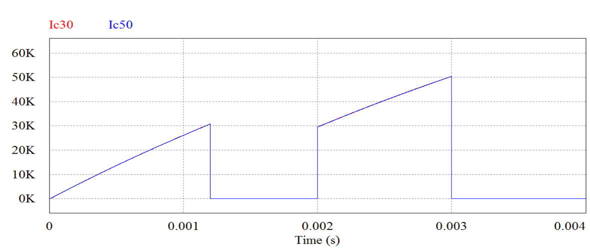

Fig. 4(b) Collector Current (I_c) Waveform

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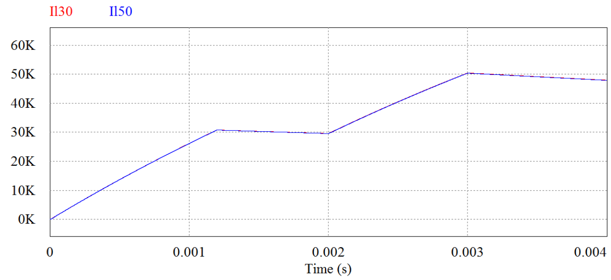

Fig. 4(b) Load Current (I_l) Waveform

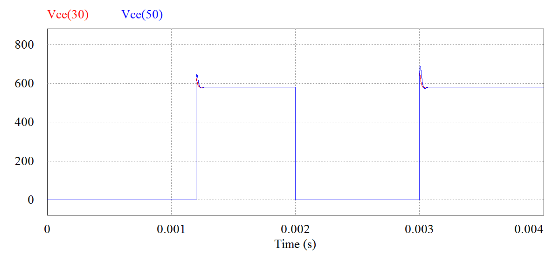

Fig. 4(b) Collector-Emitter Voltage (V_{ce}) Waveform

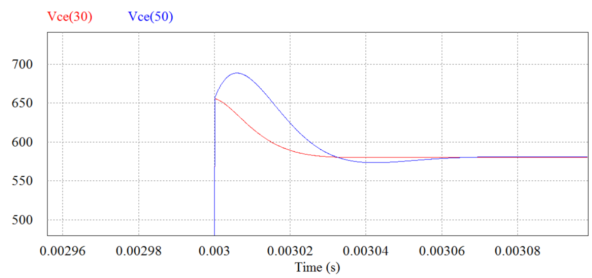

Fig. 5 Voltage Overshoot peak Waveform

TABLE I
SIMULATION PARAMETER VALUES

Parameter	Value
Dc input (Vdc)	580 V
Load Inductor (L)	20 µH
Gate Voltage (V_g)	+15/-15 V
Stray Inductance (L_s)	30 nH, 50nH
Pulse-1 On Period	1.2 ms
Pulse-1 Off Period	0.8 ms
Pulse-2 On Period	1 ms

TABLE II
VOLTAGE OVERSHOOT VALUES

Stray Inductance (L_s)	$V_{ce(peak)}$ value
30nH	655.77 V
50nH	688.66 V

IV. CONCLUSIONS

Due to extremely fast switching speeds, the voltage overshoot occurring at turn-off can easily exceed the maximum voltage rating of the device. With cautious layout practices, the parasitic inductance can be minimized. In conclude, to keep the inverter safe from voltage overshoot and get the best performance, it is recommended to keep the stray inductance as low as possible.

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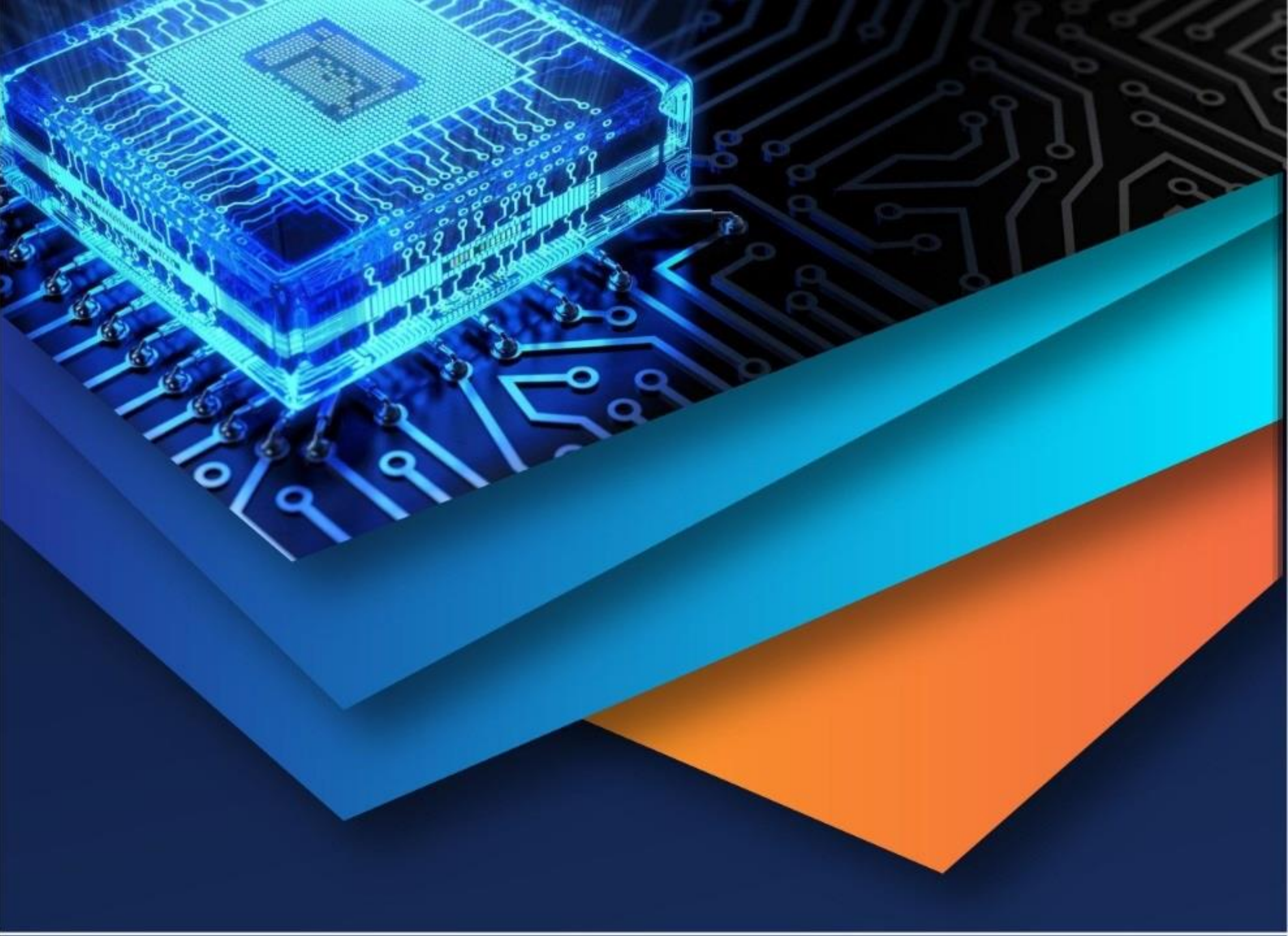

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