iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 8 **Issue:** III **Month of publication:** March 2020

DOI:

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.429
Volume 8 Issue III Mar 2020- Available at www.ijraset.com

Design and Analysis of Arithmetic Logic Unit using Reversible Logic

Nitin Krishna V
B.E. Student, Dept of Electronics and Communication Engineering, PSG College of Technology, Coimbatore

Abstract: ***In the recent years, reversible logic has become a promising technology in the areas of low power VLSI design, nanotechnology, quantum computing, etc. The performance and reliability of digital systems which are now implemented using conventional logic gates can be enhanced by usage of reversible logic gates, which pave for low power consumption and lesser quantum delays, thus increasing the speed of computation. An ALU is the fundamental building block of any digital logic programmable device and any computing system. Incorporating the concepts of reversible computing in the design of an ALU can significantly enhance the performance and speed of operation of digital systems. Furthermore, reversible logic based ALU consumes very less power as compared to existing conventional ALU designs. In this paper, an existing ALU design and a novel ALU design are compared, analysed for different bit lengths (1,8,16,32,64). A detailed analysis on reversible logic design parameters, power consumption parameters and FPGA utilization parameters is carried out. These designs are analysed and simulated using the Xilinx Vivado tool and implemented on Zedboard Zynq 7000 Evaluation and Development kit(xc7z020clg484-1). It can be concluded that the proposed design outperforms the existing design.***
Keywords: Reversible logic, reversible ALU design, quantum cost, garbage output, low power VLSI design.

I. INTRODUCTION

Over the past few decades, phenomenal growth has been achieved in the design of computers and other digital logic processing devices like mobile phones, calculator, etc. Incorporating several millions of transistors into a single chip has enabled computations and operations to be efficient and fast. However, having very high transistor densities will lead to increase in power dissipation. Existing technologies like CMOS will reach their boundaries in the near future as believed by today's researchers. Power dissipation and vulnerability to computing errors are the most important problems associated with the existing technologies. Reversible Logic is believed to be a prominent technology that could alleviate the drawbacks of the existing technologies. Reversible circuits are called lossless circuits, as there is neither energy loss nor information loss. These circuits are very attractive for applications where extremely low power consumption, or heat dissipation, is desirable in areas ranging from communications, low power VLSI (Very Large-Scale Integration) technology, DNA computing to nanotechnology. Furthermore, reversible logic has been found to be very useful in quantum computing where the quantum evolution is inherently reversible.

[1] R. Landauer's research depicts that the amount of energy (heat) dissipated for every bit operation that is not reversible is given by KT ln2, where K is the Boltzmann's constant (1.3807×10-23 JK-1) and T is the operating temperature of the system. For T equal to the room temperature (300 K), KT ln2 is approximately equals 2.8×10-21 J, which might seem is small but it is non-negligible. Say, for example if we assume that all the 1.75 billion transistors in a processor (e.g., Intel i5 core) dissipate heat at a rate equal to the processor's operating frequency (2.5 GHz), then the processor would consume a power of approximately (2.5 x 10^9) x (KT ln2) x (1.75 x 10^9) = 12.258 mW (Assuming that the room temperature is 300K). The loss incurred is not tolerable as we are in need of designing ultra-low power consuming devices. Furthermore, Moore's law states that speed and capability of computers can be expected to double every two years, as a result of increases in the number of transistors a microchip can contain. The increase in transistors will lead to further power consumption and power dissipation due to information loss. If this goes on, there will be an intolerable amount of heat dissipation by computer systems. The advent of revolutionary technologies in computing is the need of the hour. One such technology is reversible computing. [2-3] In 1973, C. H. Bennett concluded that no energy would dissipate from a system as long as the system was able to return to its initial state from its final state regardless of what occurred in between. [4] shows that the theory of reversible computing is based on invertible primitives and composition rules that preserve invertibility and the constraints to be met with deal with both functional and structural aspects of computing processes. [5] depicts that the laws of physics won't have an impact on the reduction in the size and quantum behaviour of computers. [6] Reversible logic can be defined as thermodynamics of information processing. Hence, it is used to reduce the power dissipation by preventing the loss on information. It is shown in [7] that parallel adder/ subtractor can be extended to design low power Reversible ALUs, Multipliers and

Dividers. [8] presents four designs for reversible full-adder circuits and their implementation in CMOS logic and pass transistor logic. [9] presents a detailed description on reversible computing, quantum implementation of reversible gates, challenges and promising features of reversible logic. Furthermore, it delineates how reversible logic technology will pave way for achieving ultra-low power computing. [10] presents a design of reversible logic ALU using DKG gate as the reversible full adder unit and it is understood that reversible logic based ALU outperforms existing conventional ALUs. In [11], two highly programmable, low-cost and low-delay 4*4 reversible logic gates were presented, verified and compared to existing similar logic structures and the proposed MRG and PAOG matched the HNG as the best existing 4*4 reversible gate. In [12], a reversible ALU using R gate, BME gate and DKG gate was designed and implemented in Spartan 3E FPGA. In [13], a reversible ALU design is proposed which can perform eight arithmetic operations and four logical operations. [14] proposed a reversible ALU that reduces the information by reusing the logic information bits logically and it realizes the goal of reducing the power consumption and a comparison with conventional ALU designs is made. [15] depicts how n-bit Toffoli, Peres and Fredkin gates improve the synthesis results of many larger functions, both in terms of gate count and quantum cost.

Section 2 of the paper presents brief definitions on concepts and important terminologies associated with reversible logic, power consumption parameters like static power, dynamic power, etc and FPGA design and utilisation parameters like LUTs, nets, etc. Section 3 of this paper presents some of the important basic reversible logic gates, their quantum costs and quantum representations. In section 4, a brief overview on ALU and its components is provided. Section 4 presents the existing design[10] and proposed design. Circuit diagram, RTL Schematic, various logical and arithmetic operations of both designs are provided. Section 5 of the paper consists of simulation results of existing design and proposed design for different bit lengths, waveform results from Xilinx Vivado tool and also charts and tables of comparison of parameters like gate count, number of garbage outputs, power parameters, delay incurred and FPGA utilisation parameters. Section 6 presents the conclusion of the paper and section 7 is the reference section.

II. DEFINITIONS PERTAINING TO REVERSIBLE LOGIC

A. *Reversible Function*

A multiple output Boolean function F(x1; x2; ... ; xn) of n Boolean variables is said to be reversible, if it can satisfy the following conditions:

1) The number of outputs is equal to the number of inputs.

2) Any output pattern has a unique pre-image that is, there must be a one-to-one mapping between the inputs and outputs.

B. *Reversible Logic Gates*

A gate is said to be reversible, if it has a reversible function. Reversible gates can be used to “fan-out” the input signal. Since the output is a mere copy of the input, we can easily recover the input from the output.

C. *Constant Inputs / Ancilla Inputs*

This refers to the number of inputs that are to be maintained constant at either logic 0 or logic 1 in order to synthesize the given logical function.

D. *Garbage Outputs*

Garbage outputs refers to the number of outputs which are not used in the synthesis of a given function. In certain cases, these become mandatory to achieve reversibility. Garbage is the number of outputs added to make an n-input k-output function ((n; k) function) reversible**.**

Inputs + constant inputs = outputs + garbage

E. *Quantum Cost*

Quantum cost refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit. The quantum cost of each reversible logic gate is an important optimization parameter. The quantum cost of a circuit is the minimum number of 2*2 unitary gates to represent the circuit keeping the output unchanged. The quantum cost of a 1*1 gate is 0 and that of any 2*2 gate is the same, which is 1.

F. Hardware Complexity

Hardware complexity refers to the total number of logical calculation (TC) in a circuit. The hardware complexity (HC) is determined by counting the number of EX-OR operations, number of AND operations number of NOT operations and number of OR operations.

To compute the hardware complexity of the reversible circuits; assuming:

α - no. of two input EX-OR gate operations

β - no. of two input AND gate operations

δ - no. of NOT gate operations

Ω - no. of OR operations

T - total logical operations.

The total logical calculation T be given as the sum of AND, OR, EX-OR and NOT calculations.

G. Total On-Chip Power

The power consumed internally within the FPGA, equal to the sum of device static power and dynamic power. It is also known as Thermal Power.

H. Device Static Power

The power from transistor leakage on all connected voltage rails and the circuits required for the FPGA to operate normally, post configuration. Device static power is a function of process, voltage and temperature. This represents the steady state, intrinsic leakage in the device.

I. Dynamic Power

The power consumed when all the inputs are active. It depends on voltage levels and logic and routing resources used.

J. LUT

A LUT (Look-Up Table) is a small asynchronous SRAM that is used to implement combinational logic. LUTs are usually read-only and their content can only be changed during FPGA configuration.

K. Nets and Leaf Cells

A net is a set of interconnected pins and wires. Leaf Cells could be standard cells from an ASIC library , or memories, macro cells, IP which would occupy space in the core area. These are the base cells that are used for further design/layout.

III. REVERSIBLE LOGIC GATES

There are several reversible logic gates in present. Some of the important reversible logic gates are,

A. NOT Gate

This is a 1*1 reversible logic gate with one input and one output. The input A is mapped to the output P=A’ as shown below in the figure 1.

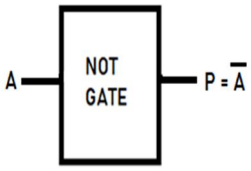


Fig. 1: NOT gate

Fig. 2: quantum representation of NOT gate

ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.429
Volume 8 Issue III Mar 2020- Available at www.ijraset.com

B. Feynman Gate

This is a 2*2 reversible gate with two inputs and two outputs. The inputs (A, B) mapped to the outputs (P=A, Q=A^B) is shown in the figure 3.

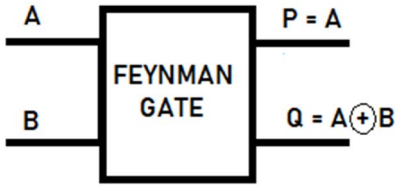


Fig. 3: Feynman Gate

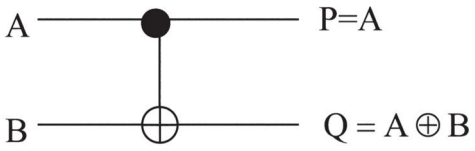


Fig. 4: quantum representation of Feynman gate

C. Fredkin Gate

This is a 3*3 Reversible gate with three inputs and three outputs. The inputs (A, B, C) mapped to the outputs (P=A, Q=A'B + A.C , R=A.B + A'.C) is shown in the figure 5.

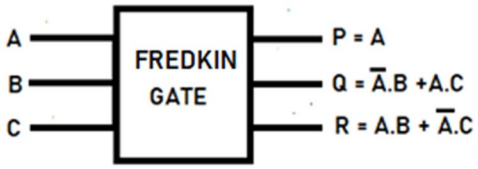


Fig. 5: Fredkin gate

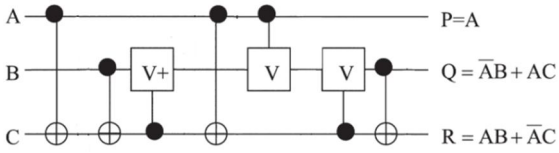


Fig. 6: quantum representation of Fredkin gate

D. Toffoli Gate

This is a 3*3 Reversible gate with three inputs and three outputs. The inputs (A, B, C) mapped to the outputs (P = A, Q = B, R = A · B ⊕ C) as shown in the figure 7.

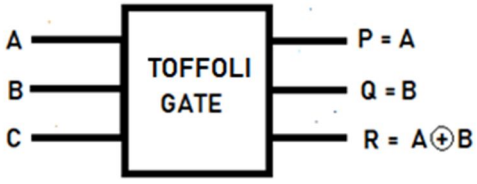


Fig. 7: Toffoli gate

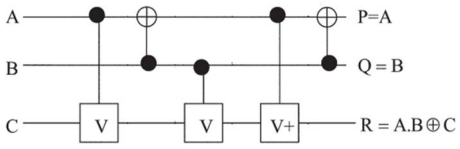


Fig. 8: quantum representation of Toffoli gate

E. Peres Gate

The Peres gate is a 3 inputs 3 outputs (3x3) reversible gate having the mapping (A, B, C) to (P=A, Q=A⊕B, R=(A.B)⊕C), where A, B, C are the inputs and P, Q, R are the outputs, respectively. It's also known as the New Toffoli Gate (NTG). It is constructed by one Toffoli and one Feynman gate. It has a quantum cost of 4.

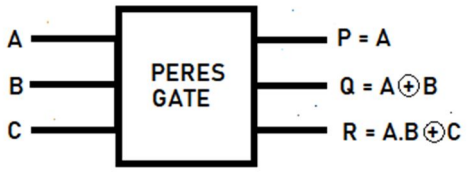


Fig. 9: Peres gate

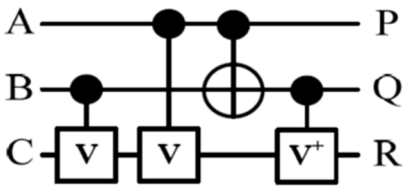


Fig. 10: quantum representation of Peres gate

F. DKG Gate

This is a 4*4 Reversible gate with four inputs and four outputs. The inputs (A, B, C, D) mapped to the outputs (P=B, Q=A'.C+ A.D' , R=A.^ B.C ^ D ^C.D, S=B^C*D) is shown in the Figure 11.

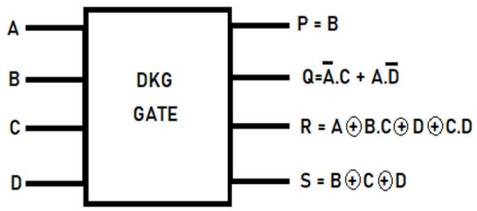


Fig. 11: DKG gate

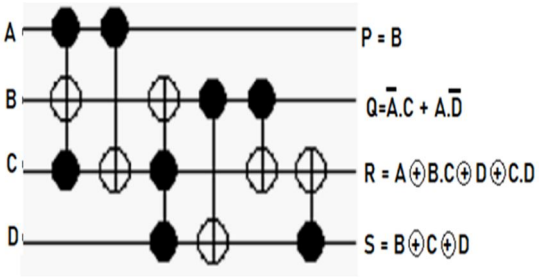


Fig. 12: quantum representation of DKG gate

ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.429
Volume 8 Issue III Mar 2020- Available at www.ijraset.com

G. WG Gate

This is a 4*4 Reversible gate with four inputs and four outputs. The inputs (A, B, C, D) mapped to the outputs (P=A, Q=A + B + D, R=A. + B + C, S=(A⊕D ⊕ B) .(A ⊕ D ⊕ C) ⊕ (A ⊕D)) is shown in the Figure 13.

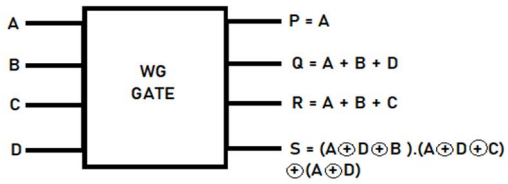


Fig. 13: WG gate

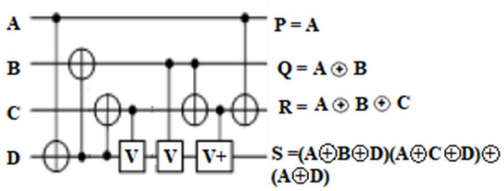


Fig. 14: quantum representation of WG gate

H. HNG Gate

This is a 4*4 Reversible gate with four inputs and four outputs. The inputs (A, B, C, D) mapped to the outputs (P=A, Q=B, R=A ⊕ (B ⊕ C), S=A ⊕ B .C ⊕A.B) is shown in the Figure 15.

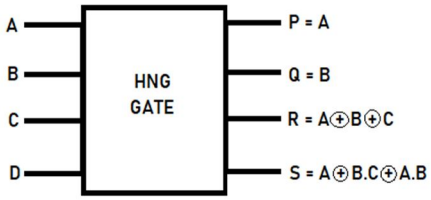


Fig. 15: HNG gate

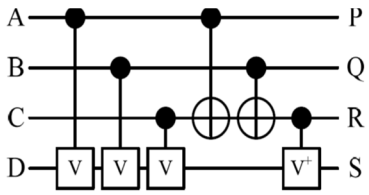


Fig. 16: quantum representation of HNG gate

I. TR Gate

This is a reversible gate that has 3 inputs and 3 outputs. The inputs (A, B, C) are mapped to the outputs (P=A, Q=A ⊕ B, R= (A.B') C).

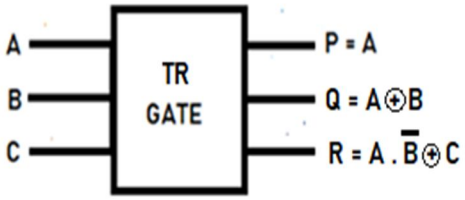


Fig 17: TR gate

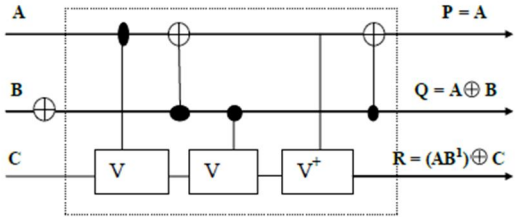


Fig. 18: quantum representation of TR gate

Table 1: Quantum cost and hardware complexity of reversible logic gates

GATE	QUANTUM COST	Hardware complexity
NOT	1	δ
FEYMAN	1	α
FREDKIN	5	4β+2 δ +2 Ω
TOFFOLI	5	α+β
PERES	4	2α+β
DKG	6	5α+4 β+2 δ+ Ω
HNG	6	4 α+2β
TR	6	2α+β+ δ
WG	7	6 α +4 Ω

IV. ALU

The basic component of an arithmetic and logic unit(ALU) is a parallel adder. By controlling the inputs to the parallel adder, we can perform different arithmetic operations like addition, subtraction, increment, decrement, etc. and logical operations like AND, OR, NOT, NOR, NAND, EXOR, and EXNOR. By cascading one-bit arithmetic and logic units, we can obtain ALUs of different bit lengths(8 bit, 16 bit, and so on). The generalized block diagram of a reversible logic ALU is shown in figure 19 which consists of a control unit and a full adder unit both constructed using reversible gates. A and B are operands on which the ALU performs operations and the outputs are F and Cout(Output Carry). The inputs Cin, S0, S1, and S2 are used to select different arithmetic and logic operations that the ALU can perform. C1,C2,… and C5 are either logic 1 or logic 0 that make the circuit to perform the desired operations and remain constant for a design.

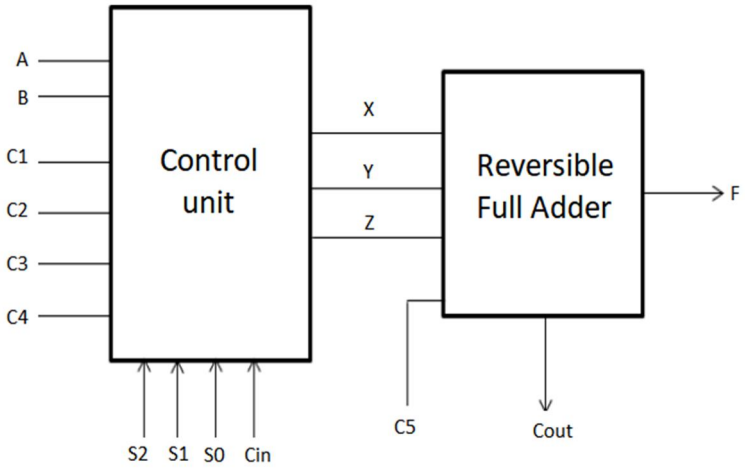


Fig 19: Block diagram of Reversible ALU

ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.429
Volume 8 Issue III Mar 2020- Available at www.ijraset.com

A. Existing Design

In this design, the control unit is constructed using a Fredkin gate, two Feynman gates and three Peres gates and the DKG gate is used as the full adder. The outputs S and R of the DKG gate as shown in figure 11 will produce the output F and carry Cout. One bit ALU is shown in figure 20. This design incurs a quantum cost of 26. There are five constant inputs and nine garbage outputs. It can perform eight arithmetic operations and seven logical operations as shown in table 2.

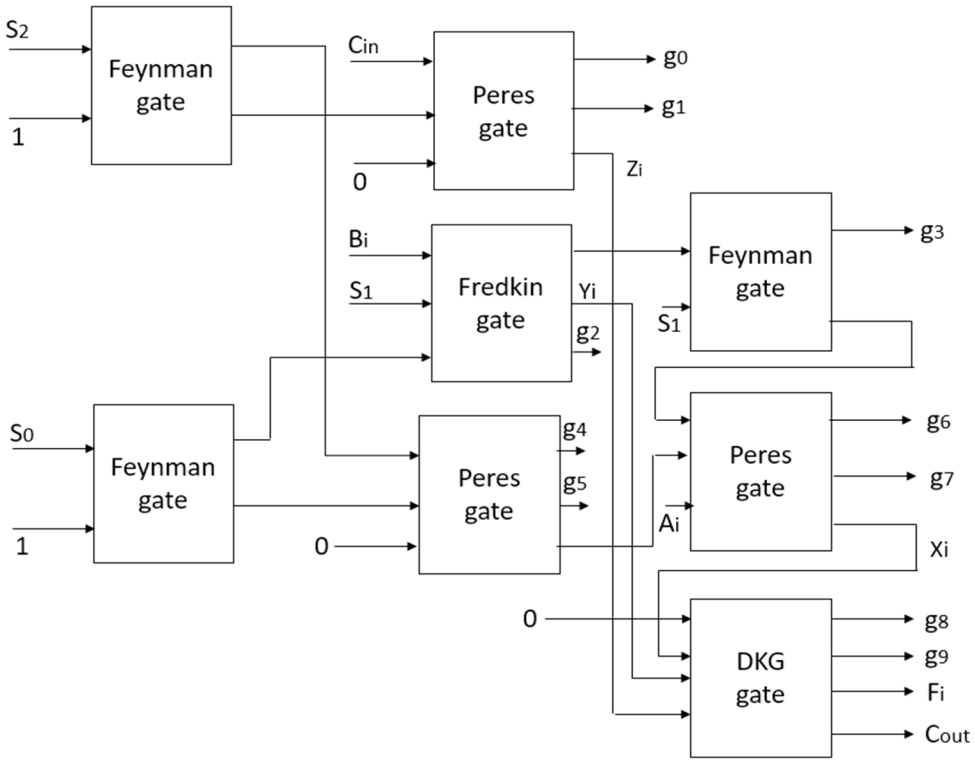


Fig. 20: Circuit diagram of existing design reversible ALU

Table 2: Arithmetic and logical operations of Existing design reversible ALU

S2	S1	S0	Cin	Output	Function
0	0	0	0	F = A	Transfer A
0	0	0	1	F = A + 1	Increment A
0	0	1	0	F = A +B	Addition
0	0	1	1	F = A + B +1	Addition with carry
0	1	0	0	F = A - B - 1	Subtraction with Borrow
0	1	0	1	F = A – B	Subtraction
0	1	1	0	F = A – 1	Decrement A
1	0	0	0	F = A | B	OR
1	0	0	1	F = (A+B)’	NOR
1	0	1	0	F = A ⊕ B	XOR
1	0	1	1	F = (A⊕B)’	XNOR
1	1	0	0	F = A & B	AND
1	1	0	1	F = (A&B)’	NAND
1	1	1	0	F = A’	NOT A
1	1	1	1	F = A	Transfer A

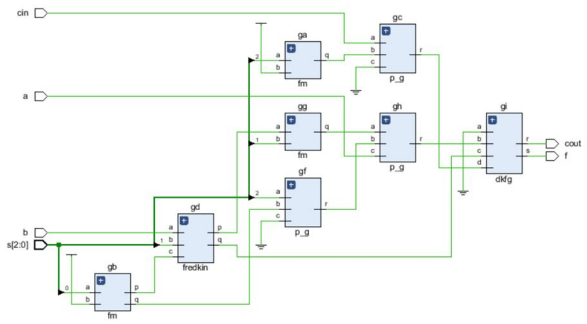


Fig. 21: RTL Schematic of 1 bit existing design ALU

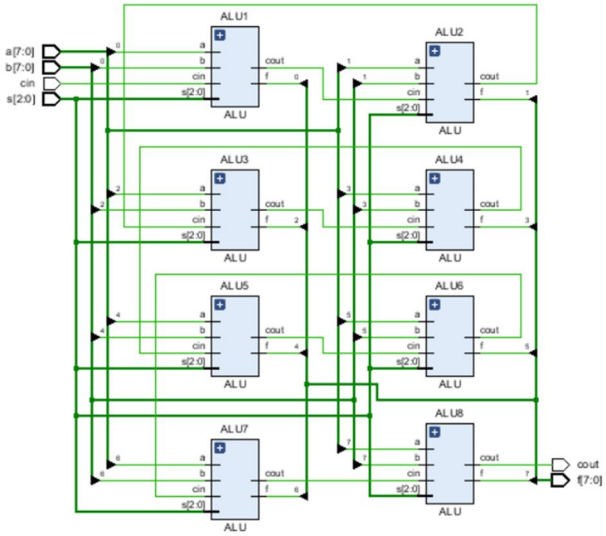


Fig. 22: RTL Schematic of 8 bit existing design ALU

B. Proposed Design

In this design, the control unit is constructed using a Feynman gate, a 4*4 Toffoli gate, and two Fredkin gates. HNG gate is used as the full adder unit. The outputs R and S of the HNG gate as shown in figure 15 will produce the output F and carry Cout. One bit ALU is shown in figure 23 . This design incurs a quantum cost of 22. There are three constant inputs and seven garbage outputs. It can perform eight arithmetic operations and seven logical operations as shown in table 3. Arithmetic operations are selected by setting S2 to logic 0 and by setting S2 to logic 1, logical operations can be performed.

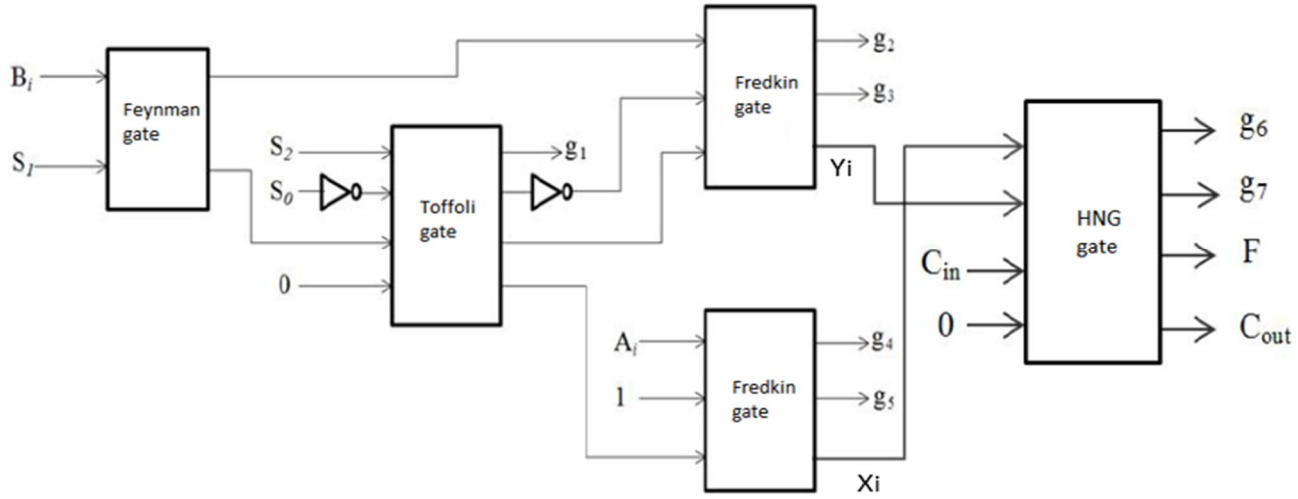


Fig. 23: Circuit diagram of proposed design reversible ALU

Table 3: Arithmetic and logical operations of Proposed design reversible ALU

S2	S1	S0	Cin	Output	Function
0	0	0	0	F = A	Transfer A
0	0	0	1	F = A + 1	Increment A
0	0	1	0	F = A +B	Addition
0	0	1	1	F = A + B +1	Addition with carry
0	1	0	0	F = A - B - 1	Subtraction with Borrow
0	1	0	1	F = A – B	Subtraction
0	1	1	0	F = A – 1	Decrement A
0	1	1	1	F = A	Transfer A
1	0	0	0	F = A | B	OR
1	0	0	1	F = (A+B)’	NOR
1	0	1	0	F = A’	NOT A
1	0	1	1	F = A & B	AND
1	1	0	0	F = (A&B)’	NAND
1	1	0	1	F = A ⊕ B	EXOR
1	1	1	0	F = (A⊕B)’	EXNOR

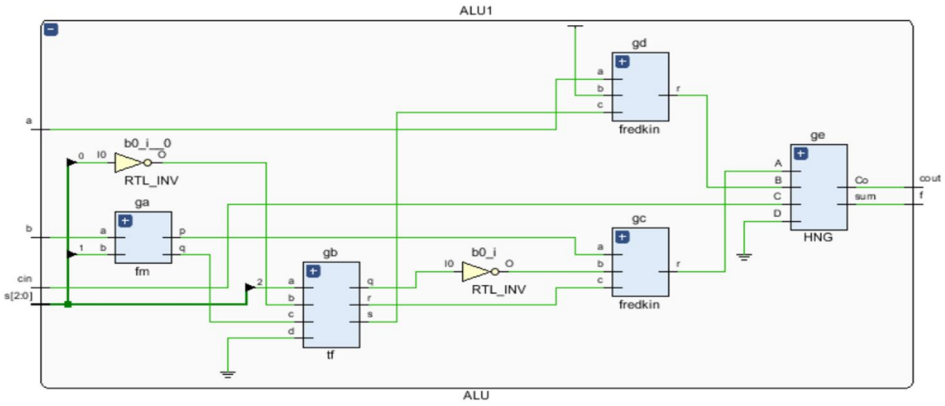


Fig. 24: RTL Schematic of 1 bit existing design ALU

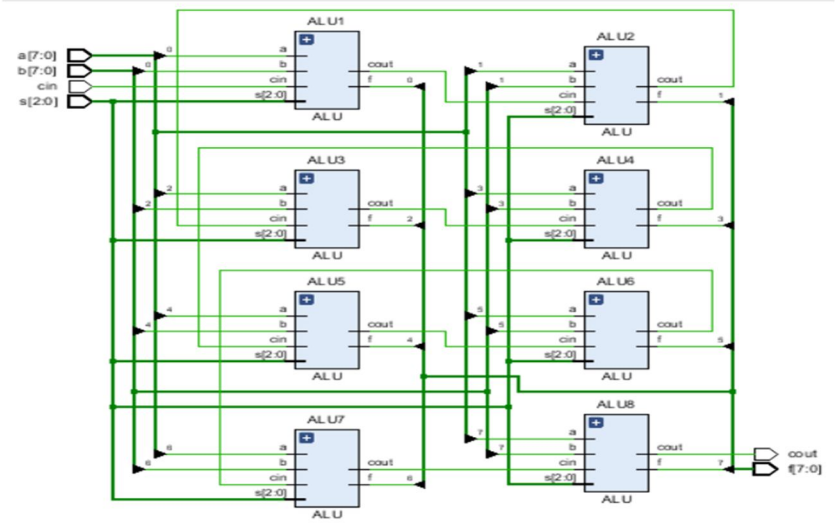


Fig. 25: RTL Schematic of 8 bit proposed design ALU

V. SIMULATION AND RESULTS

A. *Existing Design*

Table 4: Simulation results of different bit lengths of existing design reversible ALU from Xilinx Vivado tool

	1 bit	8 bit	16 bit	32 bit	64 bit
Gate Count	8	64	128	256	512
Garbage Output	9	72	144	288	576
Quantum Cost	26	208	416	832	1664
Total on-chip Power (In W)	0.105	0.108	0.112	0.12	0.136
Static Power (in W)	0.104	0.104	0.104	0.105	0.105
Dynamic Power (in W)	0.001	0.004	0.008	0.016	0.031
Logic Power (in W)	<0.001	<0.001	<0.001	<0.001	<0.001
Delay (in ns)	1.56	6.685	12.967	25.518	50.062
Nets	16	77	149	293	581
Leaf Cells	10	57	113	225	449
LUTs	2	22	46	94	190
Bonded IOBs	8	29	53	101	197

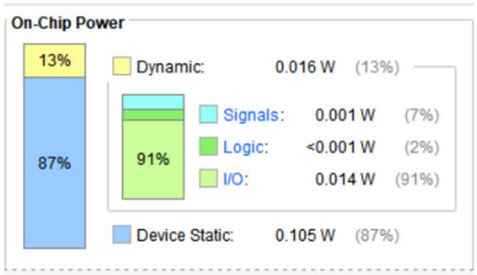


Fig. 26: Power report of existing design based 32 bit ALU

Fig. 27: FPGA utilization parameters for existing design based 32 bit ALU

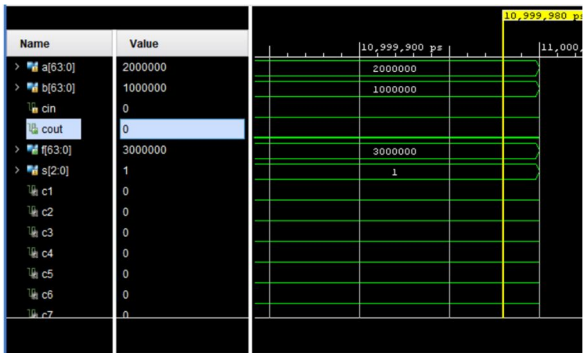


Fig. 28: Addition operation performed by 64 bit ALU on A and B by setting S2=0, S1=0, S0=1 and Cin=0

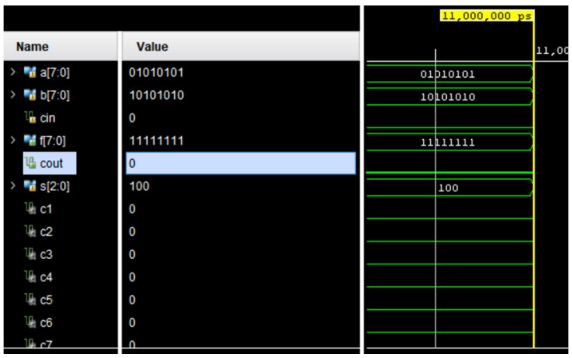


Fig. 29: OR operation on 64 bit inputs A and B by setting S2=1, S1=0, S0=0 and Cin=0

B. Proposed Design

Table 5: Simulation results of different bit lengths of proposed design reversible ALU from Xilinx Vivado tool

	1 bit	8 bit	16 bit	32 bit	64 bit
Gate Count	6	48	96	192	366
Garbage Output	6	48	96	192	366
Quantum Cost	22	176	352	704	1342
Total Onchip Power (in W)	0.105	0.107	0.109	0.114	0.122
Static Power (in W)	0.104	0.104	0.104	0.104	0.105
Dynamic Power (in W)	<0.001	0.002	0.004	0.009	0.017
Logic Power (in W)	<0.001	<0.001	<0.001	<0.001	<0.001
Delay (in ns)	1.197	6.2	11.858	22.133	45.197
Nets	16	83	162	299	594
Leaf Cells	10	63	126	231	462
LUTs	2	25	53	94	203
Bonded IOBs	8	29	53	101	197

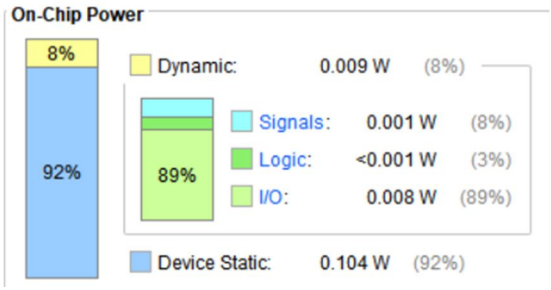


Fig.30: Power report of proposed design based 32 bit ALU

Fig. 31: FPGA utilization parameters for proposed design based 32 bit ALU

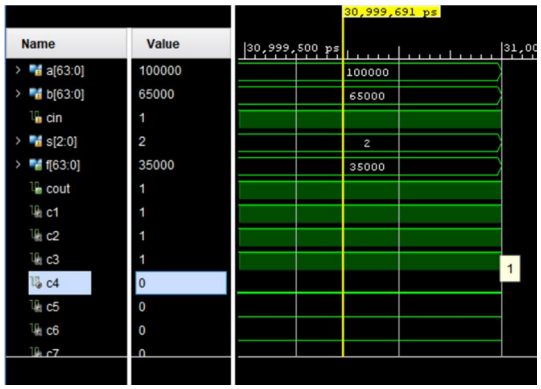


Fig. 32: Subtraction by 64 bit proposed design ALU by setting S2=0, S1=1, S0=0 and Cin=1

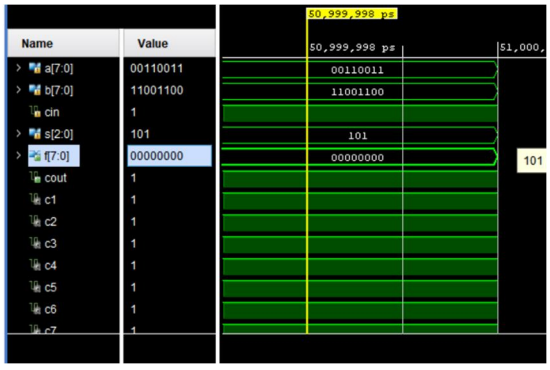


Fig. 33: AND operation by 64 bit proposed design ALU by setting S2=1, S1=0, S0=1 and Cin=1

Table 5: Comparison of gate count, number of garbage outputs and quantum cost of existing design and proposed design

	Gate Count	Garbage outputs	Quantum cost
Existing design	512	576	1664
Proposed design	366	366	1342

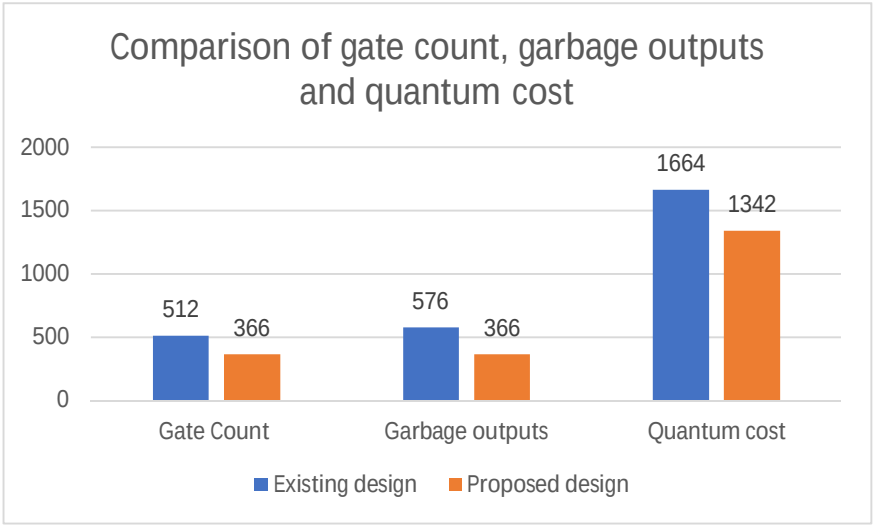


Fig. 34: Comparison chart of gate count, number of garbage outputs and quantum cost of existing design and proposed design

Table 5 shows the comparison between the existing design and the proposed design of the 64 bit reversible ALU. We can depict from the figure 34 and tables 3 and 4 that proposed design uses a fewer number of reversible logic gates, has fewer number of garbage outputs and incurs the least quantum cost in comparison with the existing design.

Table 6: Comparison of dynamic and total on-chip power of designs 1 and 2

	Dynamic power (in mW)	Total on-chip power (in mW)
Existing design	31	136
Proposed design	17	122

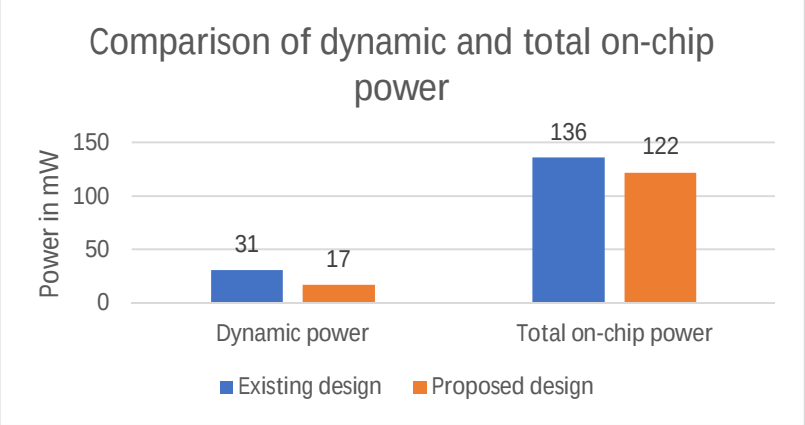


Fig. 35: Comparison of dynamic and total on-chip power of existing design and proposed design

Table 6 shows the comparison between existing design and proposed design of the 64 bit reversible ALU in terms of dynamic and total on-chip power consumed. It can be seen from tables 3, 4 that both static and logic power consumption of the designs remains fairly the same. It can be understood from the figure 35 that proposed design has the least dynamic power consumption in comparison with the existing design, as it uses a fewer number of gates. It can also be depicted that the total on-chip power of the proposed design is comparatively less than the existing design.

Table 7: Comparison of numbers of LUTs, nets and leaf cells required by existing design and proposed design

	Nets	Leaf cells	LUTs
Existing design	581	449	190
Proposed design	594	462	203

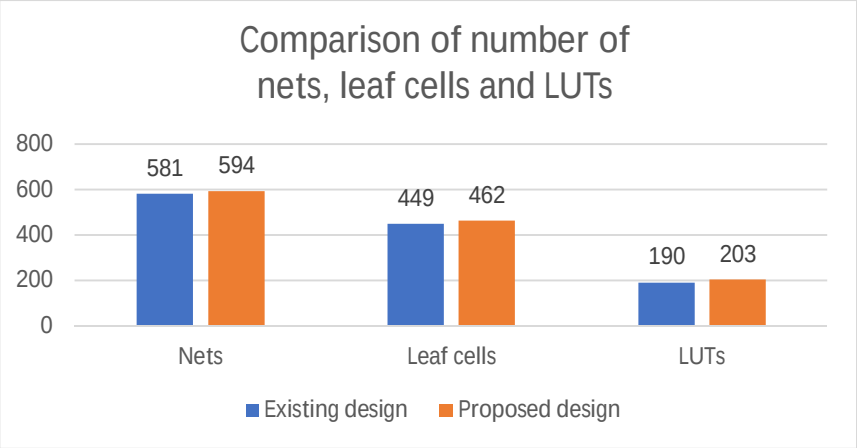


Fig. 36: Comparison chart of numbers of LUTs, nets and leaf cells required by existing design and proposed design

Table 7 shows the comparison between existing design and proposed design of the 64 bit reversible ALU in terms of the number of nets, leaf cells, and lookup tables required. It can be seen from Tables 3, 4 and 7 that existing design comparatively uses a lesser number of nets, leaf cells, and lookup tables. However, it is seen that the difference between the designs in the corresponding parameters is not so significant.

Table 8: Comparison of delay incurred for 1,8,64 bit ALUs of existing design and proposed design

	1 bit	8 bit	64 bit
Existing design	1.56	6.875	50.062
Proposed design	1.197	6.2	45.197

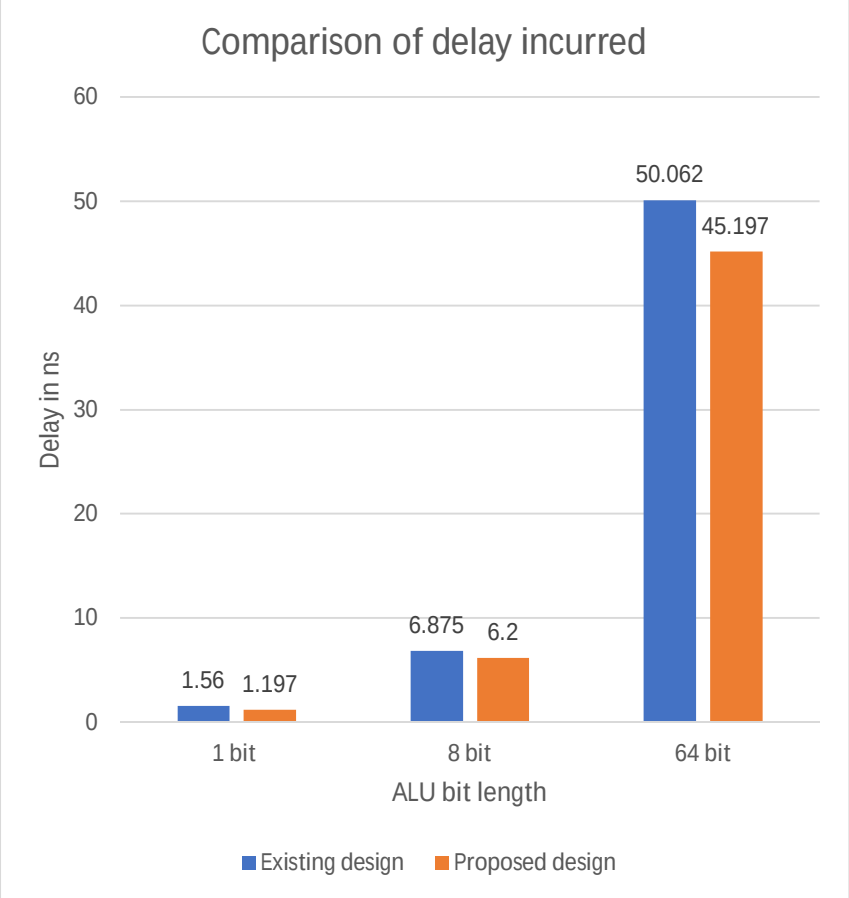


Fig. 37: Comparison chart of delay incurred for 1,8,64 bit ALUs of existing design and proposed design

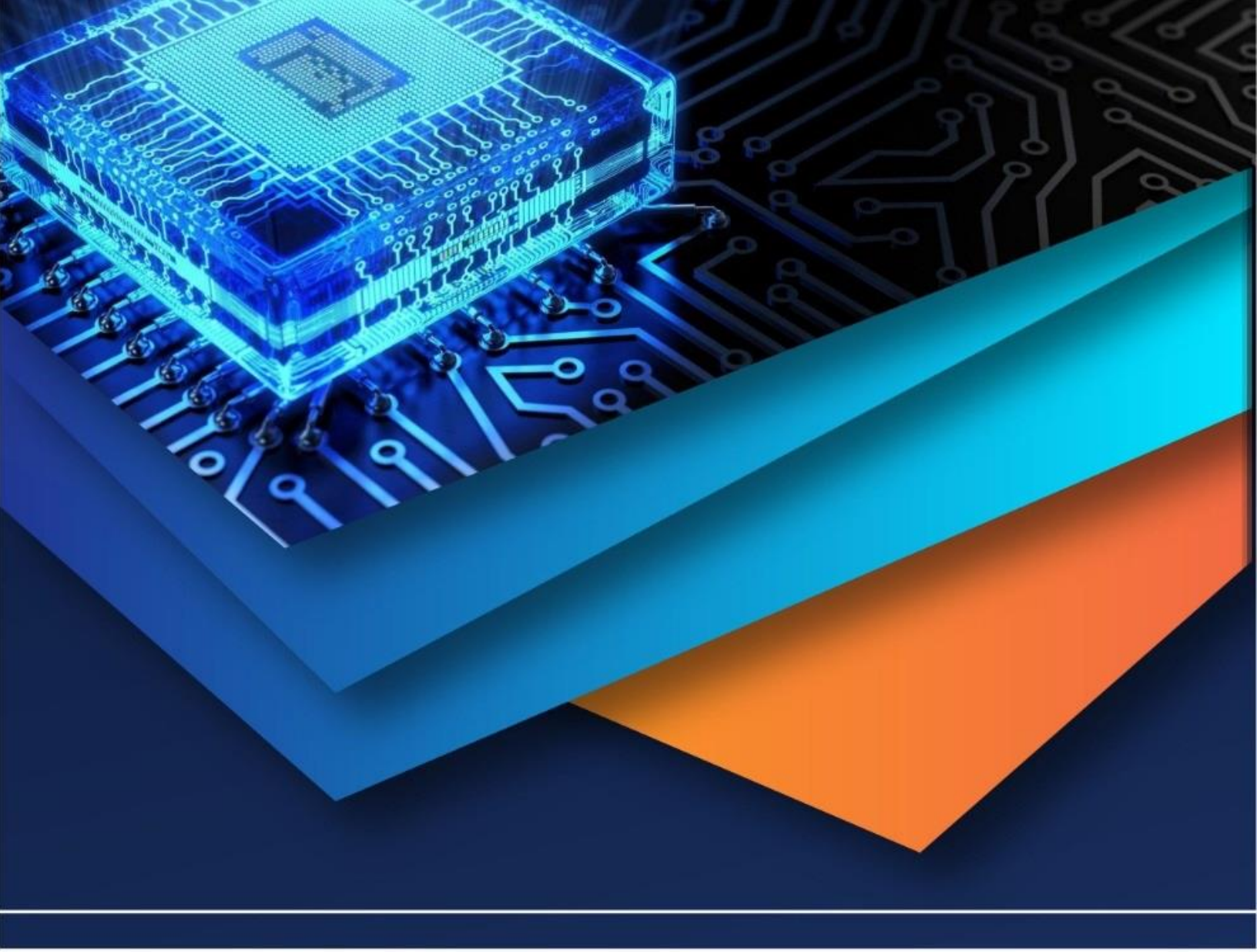
Based on Table 8, the comparison on delay between two designs of reversible ALU is made. Based on the result as shown in Fig. 37 and in tables 3,4 and 8, we can conclude that the proposed reversible ALU proposed design shows higher reductions in propagation delay as compared to the proposed existing design.

VI. CONCLUSION

In this paper, a novel reversible ALU design has been proposed. The proposed reversible ALU design is compared with an existing ALU design. Both the designs have been simulated, analysed, compared and verified using Xilinx Vivado tool. The simulation results illustrate that the proposed reversible ALU outperforms the existing design. A complete reversible computer architecture can be designed with the help of the proposed design in the near future.

REFERENCES

[1] R. Landauer, ”Irreversibility and heat generation in the computation process”, IBM journal of research and development, pp 183-191.
[2] C. H. Bennett, ”Logically reversibility of computation”, IBM journal of research and development pp 525-532, NOV 1973.
[3] C. H. Bennett, “Notes on the history of reversible computation,” IBM Journal of Research and Development, 32 (1988), pp.16-23.
[4] T. Toffoli., “Reversible Computing”, Tech memo MIT/LCS/TM-151, MIT Lab for Computer Science 1980.
[5] R. Feynman, “Quantum mechanical computers” Optics, News, 11, pp: 11-20, 1985.
[6] H. R. Bhagyalakshmi, M. K. Venkatesha, "An Improved Design of a Multiplier using Reversible Logic Gates," International Journal of Engineering Science and Technology, vol. 2, pp. 3838-845, 2010.
[7] H. V. Ravish Aradhya, K. N. Muralidhara, B.V. Praveen Kumar, ”Design of low power arithmetic unit based on reversible logic”, International Journal of VLSI and Signal Processing Applications, Vol. 1, Issue 1(30- 38),ISSN 2231-3133.
[8] Yvan Van Rentergen and Alexis De Vos ”Optimal design of a reversible full adder” International Journal of unconventional computing, Vol. 1, pp. 339–355.
[9] W. David Pan and Mahesh Nalasani. “Reversible logic.” *IEEE Potentials* 24 (2005): 38-41.
[10] K. Kirankumar, D. Ajay Kumar, “Designe Of Alu Using Reversible Logic Gates”, International Journal For Technological Research In Engineering, Volume 2, Issue 3, November-2014.
[11] M. Morrison and N. Ranganathan, "Design of a Reversible ALU Based on Novel Programmable Reversible Logic Gate Structures," *2011 IEEE Computer Society Annual Symposium on VLSI*, Chennai, 2011, pp. 126-131.
[12] Rangari, Monika, Richa Saraswat, Rita Jain, “Design of Reversible Logic ALU using Reversible logic gates with Low Delay Profile.”, International Journal of Advanced Research in Computer and Communication Engineering, Vol. 4, Issue 4, April 2015.
[13] Akanksha Dixit, Vinod Kapse, “Arithmetic & Logic Unit (ALU) Design using Reversible Control Unit”, International Journal of Engineering and Innovative Technology (IJEIT) Volume 1, Issue 6, June 2012.
[14] Zhijin Guan, Wenjuan Li, Weiping Ding, Yueqin Hang, and Lihui Ni, “An Arithmetic Logic Unit Design Based on Reversible Logic Gates|, Communications, Computers and Signal Processing (PacRim), 2011 IEEE Pacific Rim Conference on , pp.925-931, 03 October 2011.
[15] James Donald and Niraj K. Jha,” Reversible logic synthesis with Fredkin and Peres gates” , ACM Journal on Emerging Technologies in Computing Systems (JETC), vol. 4 issue 1, March 2008.



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY