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Low Pin Count and Test Time Reduction using Scan Compression

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***Abstract:** Nowadays, ASIC (Application Specific Integrated Circuit) Technology is shrinking to lower technology nodes. Testing of that device will be more difficult due to compact size. On the other hand, many advantages of lower technology nodes like requires less area, low pin count, less time for testing, etc. Testability includes two major factors controllability and observability. Low pin count reduces the number of test pins available in a small package size and test time is related to required time for testing of the device. In DFT (Design For Testability) flow first step is scan insertion that make design scannable which control and observe the each and every node of design. After that based on scan inserted design ATPG tool generate the test pattern and pattern simulation gives the result of patterns pass/fail.*

***Keywords:** Design for testability, Scan compression, Scan insertion, ATPG, Pattern simulation*

I. INTRODUCTION

This document is a template. This research work domain is Design for Testability (DFT), basically it will provide a method for testing of each and every node in the design. For this purpose nodes of the design should be controllable and observable.

Controllability is measure the difficulty of setting internal circuit nodes to 0 or 1 by assigning values to primary inputs (PI), and Observability is measure the difficulty of circuit observe at primary output node (PO). Design for testability includes many approach like Ad-hoc and structural. In structural approach Scan design, attempts to improve testability of a circuit by improving the controllability and observability of storage elements in a sequential design. This is accomplished by first converting selected storage elements in the design into scan cells and then stitching them together to form one or more shift registers, called scan chains.

The paper is organized in seven sections. Section II provides the problem definition of the paper. Section III provides the scan insertion in that compression logic added to in to the original design. Section IV provides the generation of test pattern which can detect the stuck at faults. Section V verifies the pattern for particular faults, which is called pattern simulation. Section VI provides the result and Section VII concludes the paper.

II. PROBLEM DEFINITION

A. *An Optimization of two Parameters*

1) *Pin Count:* numbers of parallel scan chain inserted in the circuit.
2) *Test Time:* Test time is time taken to detect the fault or testing time of the circuit.

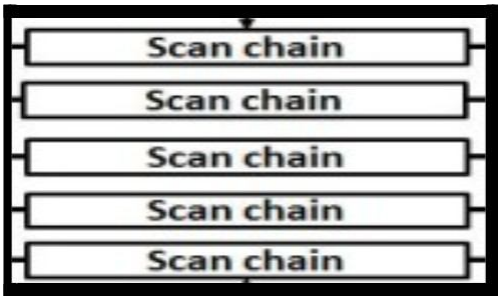


Figure 1. Bunch of Scan Chain

One of the technique for the solution is scan compression which is the process of dividing the scan chain and create more numbers of scan chain, using this method I am reducing the test time. Test time is depends on length of scan chain.

Test Time = Length of scan chain * Number of patterns

When I am compress the scan chain in more numbers of chain then pin count is increases, so in my dissertation work I have to optimize that both parameters pin count and test time.

III. SCAN INSERTION

Scan insertion is the process of replace all storage element with scan cell. In scan insertion three types of scan cell mainly used muxed D scan cell, clock scan cell, level sensitive scan design cell. Muxed D scan cell widely used for scan insertion because it will used D flip flop and muliplexer. All that scan cell stitching together and create a scan chain. It needs three pins, SI (scan data in), SE (scan enable), SO (scan data out). It will make a scannable design after scan insertion. DFT compiler tool is used for scan insertion.

1) *Scan-in:* Input for scan cell used for the scan insertion. Scan-out:Output of scan cell used for the scan insertion.
2) *Scan-enable:* Input of scan cell, which select the scan input passes through circuit or data input passes through circuit.

A. *Schematic of Design_1*

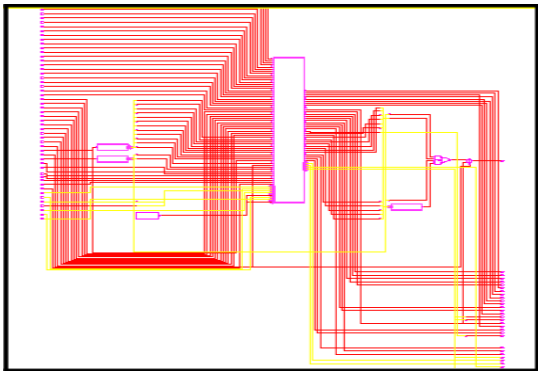


Figure 2. Schematic Diagram of Design_1

Figure 2 shows the schematic diagram of the original circuit.

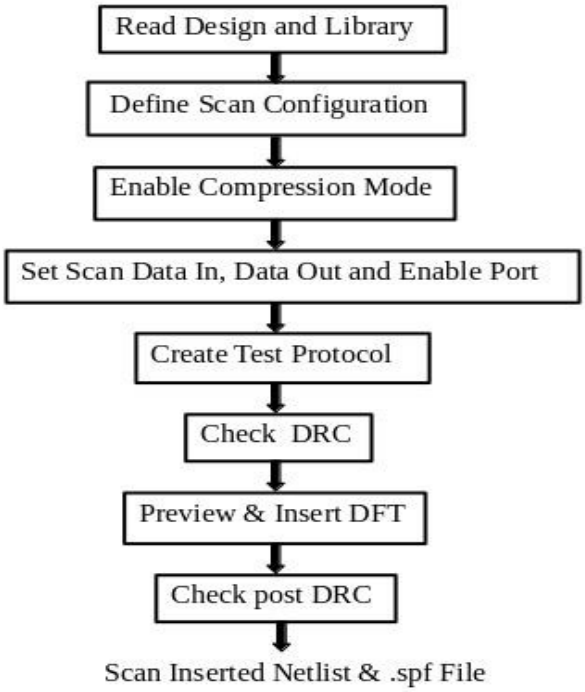


Figure 3. Flow of Scan Insertion in DFT Compiler

Figure 3 Shows the flow of scan insertion tool which is DFT compiler. First read the verilog design and libraries then enables the compression mode and add scan configuration. For set the test environment create test protocol. DRC is design rule check which is check the design as per design rule. Preview dft shows the information of inserted scan design. Insert dft is inserting the scan design in to the original design. Post drc is for check drc rule after inserting the scan design. Figure 4 and 5 shows the Pre drc and post drc report respectively.

```
Pre-DFT violations completed...
---------------------------------------------------------------

---------------------------------------------------------------
 DRC Report

 Total violations: 42
---------------------------------------------------------------

19 MODELING VIOLATIONS
     4 Cell has unknown model violations (TEST-451)
    15 Cell has no scan equivalent violations (TEST-120)

23 PRE-DFT VIOLATIONS
     4 Clock not able to capture violations (D8)
    19 Data path affected by clock captured by clock in trailing edge clock_port violations (D14)


Warning: Violations occurred during test design rule checking. (TEST-124)

---------------------------------------------------------------
 Sequential Cell Report

 104 out of 7819 sequential cells have violations

---------------------------------------------------------------

SEQUENTIAL CELLS WITH VIOLATIONS
      *  15 cells have test design rule violations
      *  70 cells are clock gating cells
      *  19 cells have capture violations
SEQUENTIAL CELLS WITHOUT VIOLATIONS
     *7715 cells are valid scan cells
```

Figure 4. Pre – DRC Report

```
---------------------------------------------------------------
 DRC Report

 Total violations: 25
---------------------------------------------------------------

4 MODELING VIOLATIONS
    4 Cell has unknown model violations (TEST-451)

21 CLOCK VIOLATIONS
    19 Trailing edge port captured data affected by new capture violations (C6)
     2 Clock connected to primary output violations (C17)


Warning: Violations occurred during test design rule checking. (TEST-124)

---------------------------------------------------------------
 Sequential Cell Report

 89 out of 7819 sequential cells have violations

---------------------------------------------------------------

SEQUENTIAL CELLS WITH VIOLATIONS
      *  70 cells are clock gating cells
      *  19 cells have capture violations
SEQUENTIAL CELLS WITHOUT VIOLATIONS
     *7730 cells are valid scan cells
```

Figure 5. Post – DRC Report

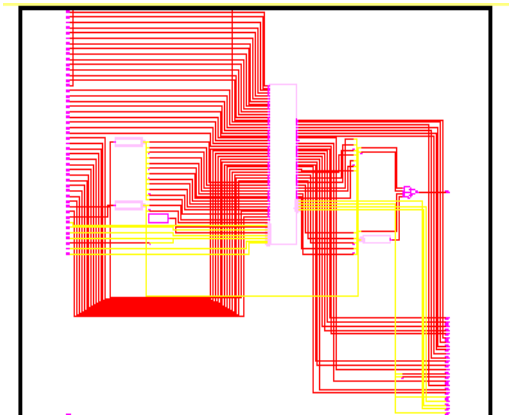


Figure 6. Preview DFT Without Scan Compression

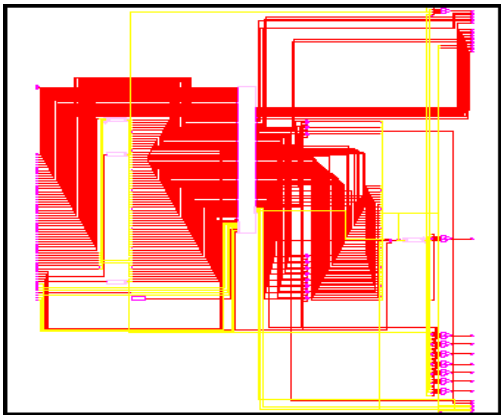


Figure 7. Preview DFT With Scan Compression

Figure 6 and figure 7 shows the Preview dft report of without scan compression and scan compression respectively.

Table I. Summary Report of Scan Insertion

Project Block : Design_1 : DFT Compiler		
Without Scan Compression	Pin Count	8
	Scan In/Out	8
	Total scan chain	8
	Length of Max Scan Chain	4767
With Scan Compression	Pin Count	50
	Scan In/Out	50
	Total scan chain	50
	Length of Max Scan Chain	171
Total Sequential Cell	7819	

IV. AUTOMATIC TEST PATTERN GENERATION

The objective of test generation is the task of producing a set of test vectors that will uncover any defect in a chip.[1] Automatic Test Pattern Generation is a method to generate a test input sequence which is distinguish between the correct circuit behavior and the faulty circuit behavior caused by defects. The patterns are used to test the circuit after manufacture and determining the cause of failure.

A. D Algorithm

1) Step1 : Target specific stuck at fault.
2) Step 2 : Drive fault site to opposite value.
3) Step 3 : Propagate error to primary output.
4) Step 4 : Record pattern, drop detected faults.

Let's take one example, here input A is stuck at 1 in AND gate. To detect this fault we must test the gate with appropriate test vector.

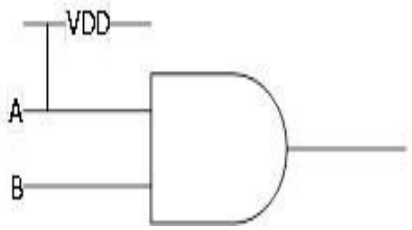


Figure 8. Stuck At 1 Fault[4]

TABLE II. TRUTH TABLE OF STUCK AT 1 CIRCUIT

A	B	O
0	0	0
0	1	1
1	0	0
1	1	1

Table 2 shows faulty operation of this AND gate. Here in 2nd row, expected output was 0 but due to stuck-at 1 fault it generated 1. Hence to detect stuck at 1 fault a node 'A' we must apply A=0 and B=1. (A, B) = (0,1) is test vector for stuck at 1 fault at A.

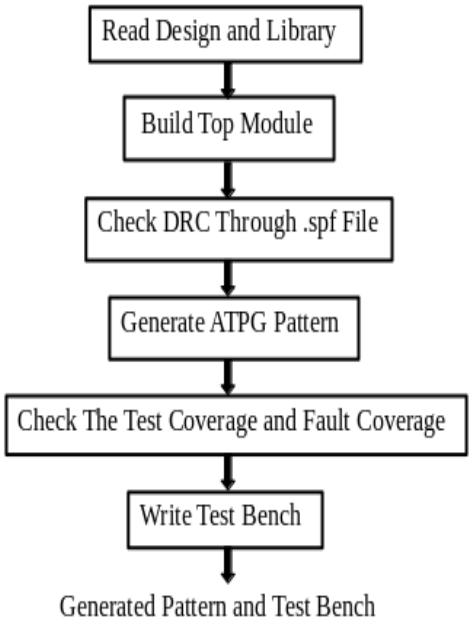


Figure 9. Flow of ATPG in Tetramax

Figure 9 shows the flow of ATPG, First read the verilog libraries and scan inserted design, build top module of the design, check drc using standard procedure file and generate the patterns for stuck at faults and write the test bench.

Table- III. Summary Report of ATPG

Project Block : Design_1 : Tetramax		
Without Scan Compression	Pin Count	8
	Pattern Count	385
	Test Coverage (Stuck At Fault)	84.13%
	Fault Coverage (Stuck At Fault)	76.51%
With Scan Compression	Pin Count	50
	Pattern Count	599
	Test Coverage (Stuck At Fault)	86.25%
	Fault Coverage (Stuck At Fault)	85.88%

V. PATTERN SIMULATION

Pattern simulation consists of generating a test bench to simulate the patterns around our design. In case of a mismatch the patterns simulation tool will show the failing cycle as well as the type of mismatch i.e. zero or one mismatch.

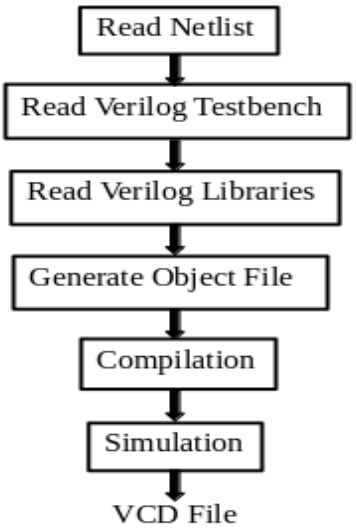


Figure 10. Flow of Pattern Simulation in VCS

Figure 10 shows the flow of pattern simulation, read libraries, test bench, netlist then generate object files and compile the design and simulate the design.

```
XTB: Simulation of 385 patterns completed with 0 mismatches

V C S   S i m u l a t i o n   R e p o r t
```

Figure 11. Simulation Without Compression

```
XTB: Simulation of 599 patterns completed with 0 mismatches

V C S   S i m u l a t i o n   R e p o r t
```

Figure 12. Simulation With Compression

Pattern simulation can simulate the pattern and it checks the mismatch of patterns are there are not. As shown in figure 11 and 12, simulation without compression and with compression with 0 mismatches respectively.

VI. RESULT

Table- IV. Report of Pin Count And Test Time

Project Block : Design_1		
Without Scan Compression	Pin Count	8
	Pattern Count	385
	Length of Max Scan Chain	4767
	Test time = No. Patterns * Length of Max Scan Chain	1835295 cycles
With Scan Compression	Pin Count	50
	Pattern Count	599
	Length of Max Scan Chain	171
	Test time = No. Patterns * Length of Max Scan Chain	102429 cycles

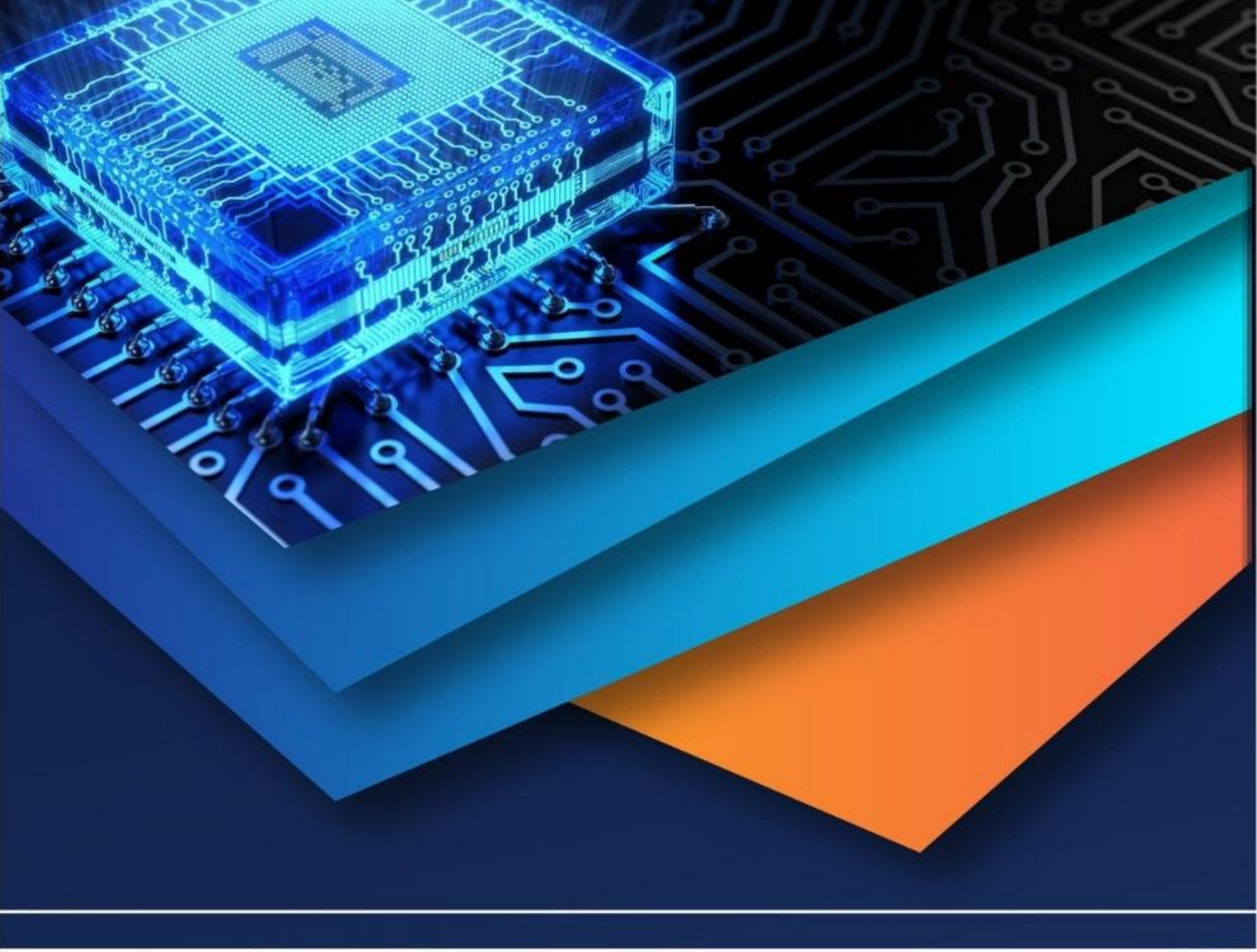
Scan compression is use for reduce the test time so, as per shown in table 4. Two iteration is there one is without scan compression and with scan compression. In this table parameters are listed pin count, pattern count, length of max scan chain and test time.

VII. CONCLUSION

In this research work optimizing the pin count and test time using scan compression methodology. In design_1 compares pin count and test time without compression and with compression scan insertion. In compression technique pin count is compressed by 50. The output of scan insertion is input to the ATPG and compare the results of without compression and with compression for test coverage are 84.13% & 86.25% respectively and fault coverage are 76.51% & 85.88% respectively. ATPG generates the pattern and testbench so verifying that pattern for stuck at faults by using VCS tool and it shows the 0 mismatch of the pattern. Test time is also compares in the result section, using compression technique test time is also reduce.

REFERENCES

[1] Laung-Terng Wang, Cheng-Wen Wu, Xiaoqing Wen, “Vlsi Test Principles and Architectures Design For Testability”, 2006.
[2] Naman Gupta, “Overview and Dynamics of Scan Chain Testing”,accessed on 28th nov 2019,http://anysilicon.com/overview-and-dynamics-of-scan-testing/
[3] Mudasir S. Kawoosa, Rajesh K. Mittal, Maheedhar Jalasuthram and Rubin A. Parekhji, “Towards Single Pin Scan for Extremely Low Pin Count Test”,IEEE International Conference on VLSI Design and Embedded systems, 2018.
[4] Ms. Janki Chauhan, Mr. Chintan Panchal, Prof. Haresh Suthar, “Scan Methodology and ATPG DFT Techniques at Lower Technology Node”,IEEE International Conference on Computing Methodologies and Communication, 2017.
[5] Binod Kumar, Boda Nehru, Brajesh Pandey, Jaynarayan Tudu, “Skip-Scan: A Methodology for Test Time Reduction”, IEEE International Symposium on VLSI Design and Test, 2016.
[6] S. Praveen , Siva Yellampalli , Ashish Kothari, “Optimization of Test Time and Fault Grading of Functional Test Vectors using Fault Simulation Flow”,IEEE International Conference on Electronics, Communication and Computational Engineering, 2014.
[7] Jay Jahangiri, Nilanjan Mukherjee, Wu-Tung Cheng, Subramanian Mahadevan, and Ron Press, “Achieving High Test Quality with Reduced Pin Count Testing”,IEEE Asian Test Symposium, 2005.
[8] Mohan PVS, Rajanna K.M, “Implementation of scan insertion and compression for 28nm design technology”, International Journal of Engineering Development and Research, 2017.
[9] Dragan Topisirović, “The advantages of combining low pin count test with scan compression of vlsi testing”, ETRAN Conference, 2012.
[10] Synopsys, “DFT Overview User Guide for DC Compiler”, 2013.
[11] Somasekhar Prabhakaran, Darshal Patel, Darshan Patel, “ATPG Challenges at Lower Technology Nodes”,accessed on 28th nov 2019,,https://www.design-reuse.com/articles/39857/atpg-challenges-at-lower-technology-nodes.html



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