iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 3 **Issue:** VI **Month of publication:** June 2015

DOI:

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)

Analysis of 64-Bit Sram Architecture in 90nm Technology Using Dual Threshold Voltage

K.Vinothini[1], P.Thiruvalar selvan[2]
[1]*M.E.Student*, [2]*Professor, Department of Electronics and communication Engineering,*
TRP Engineering college (SRM group), Affiliated to Anna University
Irungalur, Mannachanallur Taluk, Tiruchirappalli District, Tamil Nadu, India

Abstract- Static Random Access Memory (SRAM) is a type of memory that is used for high speed and low power applications. As the technology is scaling down, the noise margin of the SRAM cells decreases with the scaling of power supply. The leakage power in the SRAM cells is further increased due to the reduced noise margin. The main objective of this paper is to deal with the power dissipation which occurs normally in the Static Random Access Memory (SRAM) cells during the read and write operation. The 64-bit SRAM architecture is designed using 5T SRAM cell in 90nm technology. The performance of this architecture with its power dissipation and delay are calculated. This is simulated in Cadence Virtuoso Schematic Composer and the Spectre as the simulator.

Keywords - 5T SRAM cell, delay, power dissipation, read and writes operation.

I. INTRODUCTION

Nowadays the devices are being scaled down to reduce the silicon area and to achieve high speed and performance. To reduce the power dissipation, supply voltage and threshold voltage should be scaled down for high performance. When the threshold voltage reduces, the sub threshold leakage current is exponentially increased. This increases the static power dissipation also. Static power dissipation is mainly contributed by leakage current [1].The major source of power dissipation in the processor is the leakage power of cache [2]. The total leakage power in a SRAM cell can be determined by the contribution of each transistor leakage currents of a SRAM cell. In this paper, 64-bit SRAM architecture is designed using 5T SRAM cell by using dual-threshold voltage (dual-V_t) technique in GPDK 90 nm technology using Cadence tool.

II. CIRCUIT DESIGN AND ANALYSIS

A. *Five Transistor (5t) Sram Cell Design*

The 5T SRAM cell has only one access transistor NM1 and a single bit line BL. The data storage node Q is directly accessed through the bit-line transistor (NM1) during a read operation is shown in Fig. 1 with its layout shown in Fig. 2. The word line (WL) is maintained at V_{dd}, while writing 1 or 0 into the 5T cell by driving the bit line (BL) to V_{dd}(1V) or V_{ss}(0V) respectively. If the access transistor(NM1) is accessed through the bit-line, the input data is written in the cell[5]. To start a read operation, the word-line is asserted to V_{ss}. The previously written data in the cell can be read by charging bit-line (BL).

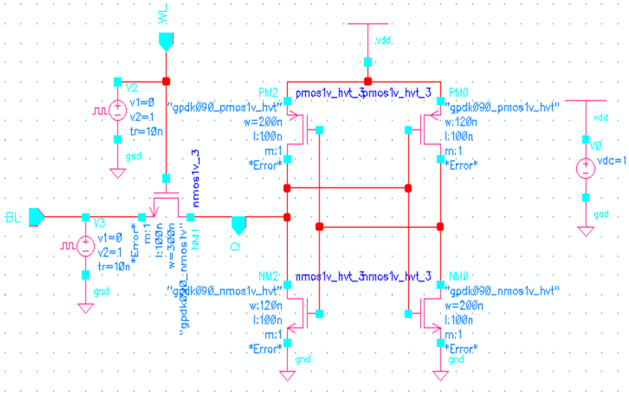


Fig. 1 5T SRAM cell design

Volume 3 Issue VI, June 2015
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

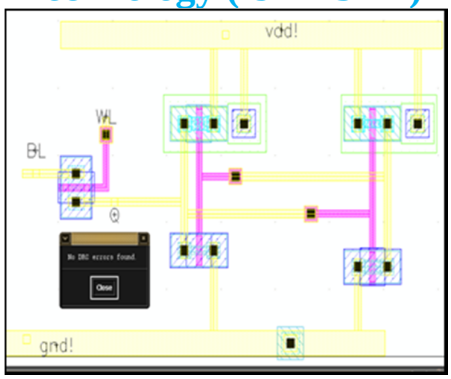


Fig. 2 5T SRAM cell layout

B. 64-Bit Sram Architecture Design Using 5t Sram Cell

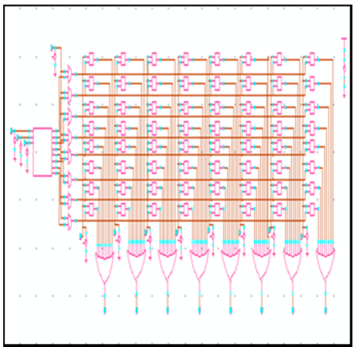


Fig. 3 64-bit SRAM architecture design

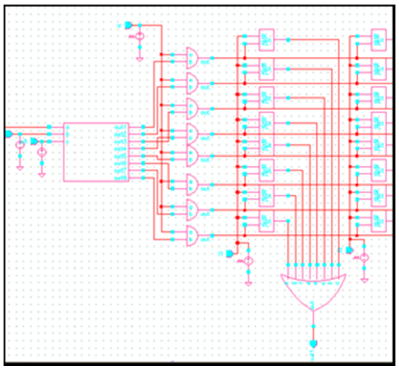


Fig. 4 Enlarged view of single column 64-bit SRAM architecture

C. Address Decoder

Address decoder is used to decode the given input address and to enable a particular word line (WL). In particular dynamic NAND CMOS decoder is used. For an n-word memory, an **m: n** dynamic NAND CMOS decoder is used where $m=\log 2^n$. The schematic of 3:8 dynamic NAND CMOS decoder is shown in Fig 5. According to selection of input we can enable particular word line(WL) row of SRAM structure.

Volume 3 Issue VI, June 2015
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

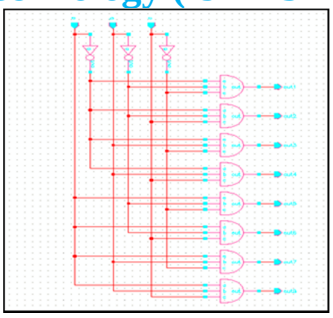


Fig. 5 3x8 Decoder

D. 2 Input AND Gate

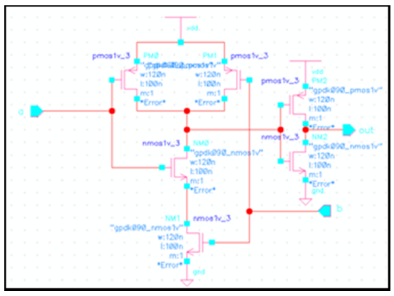


Fig. 6 2 input AND Decoder

E. 8 Input OR Gate

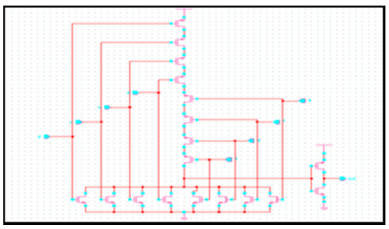


Fig. 7 8 input OR Decoder

F. 64-Bit SRAM Architecture Output

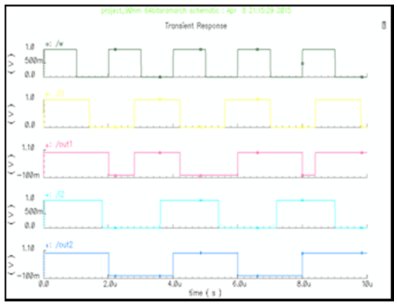


Fig. 8 64-bit SRAM Architecture Output

The fig. 8 shows the output of the 64-bit SRAM architecture in which the address is given to address decoder and data "1" is written first and then "0" is written to the architecture when the word-line (WL) is pulsed to V_{dd}. The data "0" written to the cell previously can be read by keeping word-line (WL) to low. Similarly, all the data inputs are written and read.

G. Voltage Scaling (Voltage Vs Power)

Scaling the power supply voltage enables a quadratic reduction in dynamic power dissipation with a reduction in Performance which can be partially compensated by scaling the threshold voltage. There are difficult manufacturing limitations when scaling

threshold voltages (mainly due to intra- and inter-chip variations) but the general view seems to be that continuous voltage scaling would be beneficial if manufacturing allowed it.

.

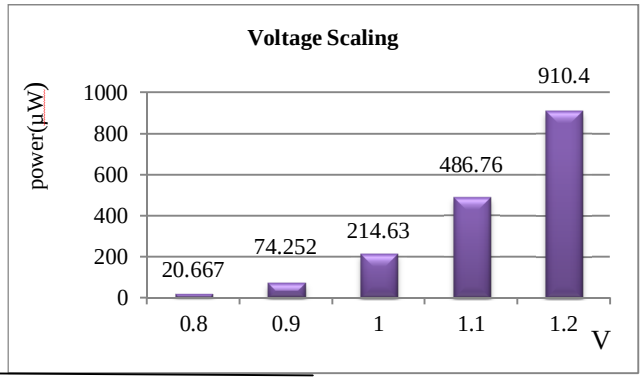


Fig. 9 Voltage Scaling (voltage vs power)

Thus, the voltage scaling (voltage vs power) shown in fig. 9 shows that the supply voltage increases the power also increases.

H. Voltage Scaling (Voltage Vs Delay)

Scaling the power supply voltage enables a quadratic reduction in dynamic power dissipation with a reduction in Performance which can be partially compensated by scaling the threshold voltage. There are difficult manufacturing limitations when scaling threshold voltages (mainly due to intra- and inter-chip variations) but the general view seems to be that continuous voltage scaling would be beneficial if manufacturing allowed it.

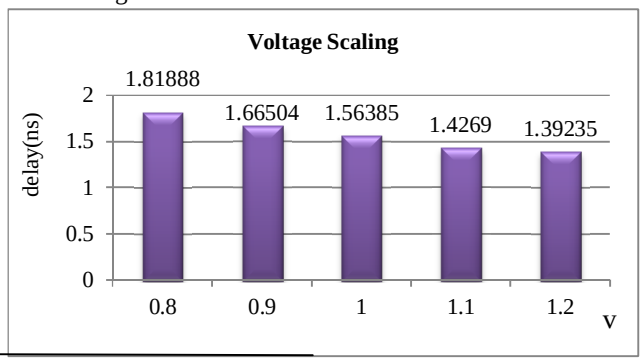


Fig. 10 Voltage Scaling (voltage vs delay)

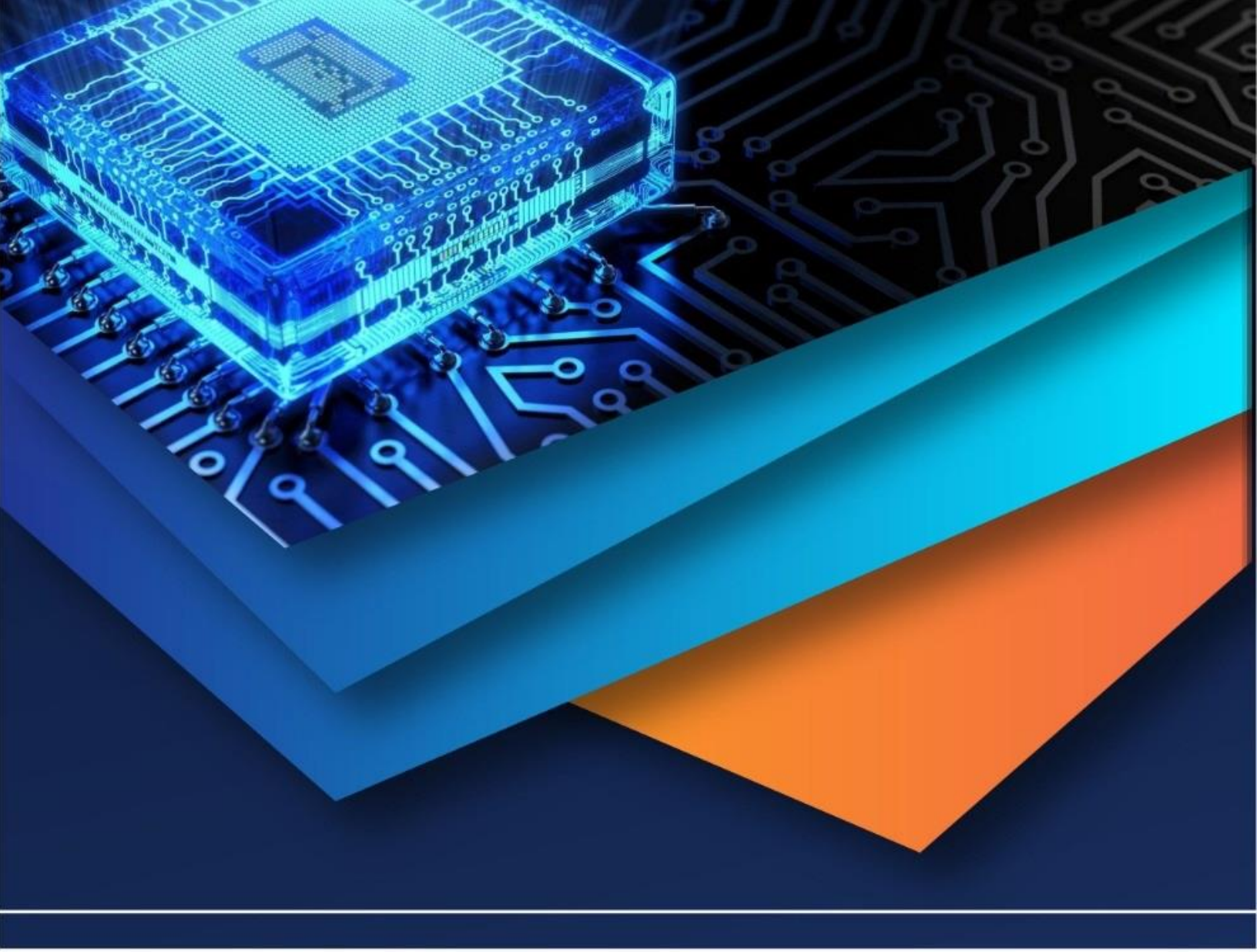
Thus, the voltage scaling (voltage vs delay) shown in fig. 10 shows that the supply voltage increases the delay decreases.

III. CONCLUSION

Thus, the 64-bit SRAM architecture with five transistor (5T) SRAM cell structure using dual-threshold voltage technique have been designed for better performance with reduced power dissipation. In future, the number of transistors can be reduced for making the SRAM cell and the architecture can be done with that SRAM cell by using triple-threshold voltage technique to get better performance and reduced power consumption.

REFERENCES

[1]Piguet C, Low power electronic design, CRC press, 2005.
[2]K. Dhanumjaya, M. Sudha, Dr.M.N.Giri Prasad, Dr.K.Padmaraju(2012),“ Cell stability analysis of conventional 6T dynamic 8T SRAM cell in 45nmtechnology,” International Journal of VLSI design and Communication Systems(VLSICS) Vol.3, No.2, April 2012.
[3]Hong Zhu and Volkan Kursun(2014), "A Comprehensive Comparison of Data Stability Enhancement Techniques with novel nano scale SRAM cells under parameter fluctuations", IEEE Transactions on Circuits and Systems— I : regular papers, vol. 61 , no.5, pp.1473-1484, May 2014.
[4]Sagar Joshi and SarmanHadia, "Design and Analysis for Low power CMOSSRAM cell in 90nm technology using cadence tool",International Journal of Advanced Research in Computer and Communication EngineeringVol.2,Issue 4, pp.1814-1817,April 2013.
[5] Z. Liu and V. Kursun,“Characterization of a novel nine transistor SRAM cell,” IEEE Trans. Very Large Scale Integr .(VLSI) Sys, vol.16, no.4, pp.488–492, April 2008.



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY