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Novel Switched-Capacitor Inverter Using Series/Parallel Conversion For 11-Level

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Abstract*—In this paper Switched capacitor (SC) inverter is employed to amend high output voltage than the input voltage with minimal number of switches. A new series/parallel topology is proposed this require switches and capacitors only, without any inductors in the circuit. Here maximum output can be attained based on capacitor number. Switched-capacitor inverter on the whole enforced in electric vehicles, dispersed generation system. In this paper the operating principle, the simulation results with MATLAB/SIMULINK are shown for seven-level and eleven-level SC inverter.
Keywords*— Charge pump, Multicarrier PWM, Multilevel inverter, Marx inverter, Switched Capacitor (SC).

I. INTRODUCTION

In recent years electrical energy systems like electric vehicles (EVs), dispersed generation (DG) systems, are concentrated because of global environmental issues. Thus electric vehicles (EVs) are studied all over the world [1]-[6]. Grid connected DG systems and EVs requires an inverter to converter dc to ac. This SC inverter need not have any use of inductor which can make system smaller than the conventional two-stage unit which comprises of a boost converter and an inverter bridge. Boost converters or transformers are most often used in these systems, whenever the input voltage is smaller than that of the output voltage. Though the transformer or an inductor in boost converter makes the system large, the transformer and the inductor must have large and heavy magnetic cores to affirm heavy high power [5]. By planning against the issue a charge pump where the inductors are not present is employed to such systems [7]. With respect to switched capacitors a charge pump outputs a higher voltage than input voltage. Here when capacitors and input voltage sources are in parallel then the capacitors are charged and if several capacitors are connected in series with the input voltage source then capacitors gets discharged. Charge pump outputs the addition of voltages of the capacitors and the input voltage sources. But a charge pump comprises of more number of switching devices so that the system becomes complex. Due to complexity of the charge pump system switched capacitor have been used. The functioning of SC is similar to that of charge pump. A switched-capacitor (SC) inverter outputs multilevel voltages based on switched capacitor [8][9]. For reducing still more switches a new topology Marx inverter is used compared to SC inverter was proposed [10]. Based on the operation principle of Marx inverter it can be considered as SC inverter. This can overcome the limitations of most common multilevel inverter such as diode-clamped, capacitor-clamped and cascaded-inverter. SC inverter in this paper consists of a Marx inverter structure and an H-bridge due to which it gives larger output voltage than the input voltage by switching capacitors in series and in parallel. The harmonics of proposed inverter are reduced than that of multilevel inverter output.

II. SWITCHED CAPACITOR INVERTER

Switched capacitor (SC) power converters are a subset of power converters with the help of only switches and capacitors this can efficiently convert one voltage to another voltage. SC comprises of different topologies, but topology employed here is series/parallel topology. Principle of this topology is based on capacitors, that is when several capacitors are in parallel with the input voltage source then the capacitors get charged and when they are in series with the input voltage source capacitors get discharged. Based on this principle the output voltage is increased than the input voltage.

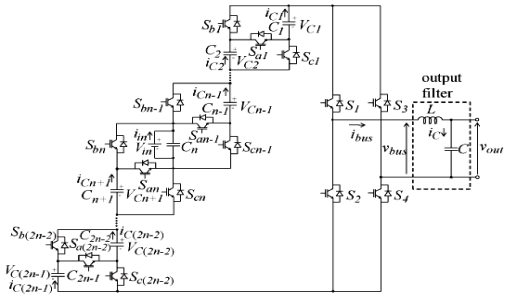

Fig.1 Circuit topology of switched-capacitor inverter using series/parallel conversion for n-Level

Circuit Description

Fig.1. represents circuit for n-level SC inverter. Whereas S_{ak}, S_{bk}, S_{ck} and (k=1,2,…2n-2) are switching devices and capacitors C_k (k = 1,2,3,…2n-1). Inverter bridge has the switches S_1 – S_4 also it has voltage source V_{in} as the input voltage source. It also consists of a low-pass filter is compiled of an inductor *L* and capacitor *C*. It comprises of 2n-1 number of capacitors and 4n-1 output voltage levels where (n=1,2,3…). Based on number of output levels the number of capacitor and switches are calculated.

A. Operation Modes Of 7-Level Inverter

1) *Zero Voltage Level:* This mode of operation referrers zero voltage level. Here switches S_2 and S_4 are turned on so that no current flows through the capacitors, due to this the voltage appear here is zero volts.
2) *V_{in} Voltage Level:* Switches turned on in this mode are S_1, S_4, S_{b1}, S_{c1}, S_{b2}, S_{c2}. As all the capacitors C_1, C_2 and C_3 are in parallel with voltage source, the capacitors are charged and store the energy. Appeared voltage level in this mode is V_{in}.
3) *2Vin Voltage Level:* Switches which are turned on in this mode are S_1, S_4, S_{a1}, S_{b2} and S_{c2}. Here C_1 is in series with voltage source so that it gets discharged and C_3 is in parallel with voltage source and is charged.
4) *3Vin Voltage Level:* In this mode of operation the switches turned on are S_1, S_4, S_{a1} and S_{a2}. Here the capacitors C_1, C_2 and C_3 are connected in series with the voltage source so that the capacitors start discharging and goes to off state.

There are number of modulation methods to drive multilevel inverters, they are multicarrier pulse width modulation (PWM) [3],[11], hybrid modulation [1],[3], space vector modulation, selective harmonic elimination method [3],[12]. Here, multicarrier PWM method is employed in proposed inverter.

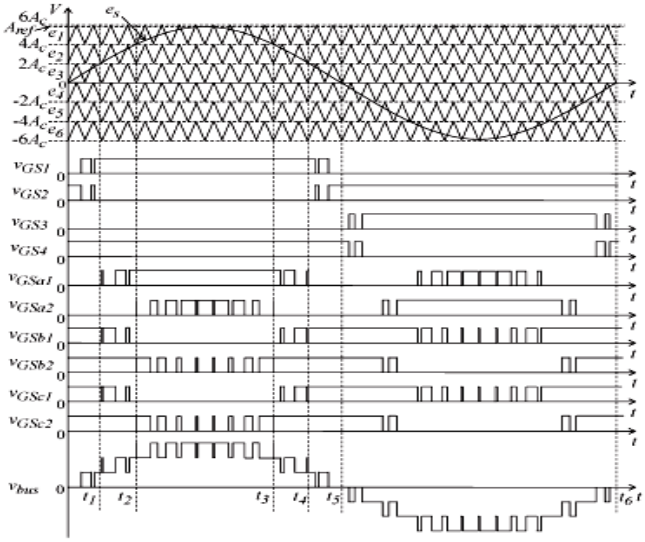

Fig.2 Modulation method for the seven-level inverter

Operation modes for the seven-level inverter (n=2) is described above and modulation method is shown in Fig.2. The switches S_1 and S_2 are driven by gate source voltage v_{GS1} and v_{GS2} respectively when time *t* satisfies $0 \leq t < t_1$ from Fig.2. When the switches S_1 and S_2 are turned on alternately and other switches are maintained ON or OFF as shown in Fig.2. Thus, the states are switched alternately and bus voltage v_{bus} takes 0 or $V_{in.}$ from Fig.2. The switches Sa1, Sb1 and Sc1 are driven by the gate source voltages V_{GSa1}, V_{GSb1}, V_{GSc1} respectively which the time t satisfies $t1 \leq t < t2$. When the switches Sa1, Sb1 and Sc1 are switched alternatively the other switches are maintained ON or OFF state as shown in Fig.2. Thus, the states V_{in} and $2V_{in}$ are switched alternatively. The capacitor C1 is charged by the current $-i_{C1}$, then the proposed inverter can output the bus voltage V_{bus} . The V_{bus} voltage in the state of V_{in} is given as

$$V_{bus} = V_{in} + V_{C1} \quad (1)$$

Where, V_{C1} is the voltage of capacitor C1.

From fig.2, the switches Sa2, Sb2 and Sc2 are driven by VGSa2, VGSb2 and VGSc2 respectively when the time t satisfies $t2 \leq t < t3$. The switches Sa2, Sb2 and Sc2 are switched alternately the other switches are maintained ON or OFF state. Thus, the states $2V_{in}$ and $3V_{in}$ are switched alternately. The capacitor C3 is charged by the current –iC3. The bus voltage V_{bus} in the state $3V_{in}$ is given as

$$V_{bus} = V_{in} + Vc1 + Vc3 \quad (2)$$

Where, V_{C3} is the voltage of capacitor $C_{3.}$

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After *t = t3*, all the four states explained above are repeated in turn.

TABLE 1: LIST OF ON-STATE SWITCHES ON EACH STATE FOR 7-LEVEL

Relationship between e_s and e_k	On state switches	Ideal bus voltage
es > e1	S1, S4, Sa1, Sa2	3Vin
e1 ≥ es > e2	S1, S4, Sa1, Sb2, Sc2	2Vin
e2 ≥ es > e3	S1, S4, Sb1, Sc1, Sb2, Sc2	Vin
e3 ≥ es > e4	S2, S4, Sb1, Sc1, Sb2, Sc2	0
e4 ≥ es >e5	S2, S3, Sb1, Sc1, Sb2, Sc2	-Vin
e5 ≥ es > e6	S2, S3, Sb1, Sc1, Sa2	-2Vin
e6 ≥ es	S2, S3, Sa1, Sa2	-3Vin

Here, Table 1 represents the list of on-state switches for the seven-level inverter (n=2) is driven with modulation method as shown in Fig.2. From Table 1 ideal bus voltage intends bus voltage on each state when $V_{C1} = V_{C3} = V_{in}$. Like conventional SC inverter, proposed inverter consists of full bridge which is connected to high voltage. Thus, device stress of the switches $S_1 - S_4$ in full bridge is higher than that of other switches.

III. 11-LEVEL SWITCHED-CAPACITOR INVERTER

A. *Proposed Topology*

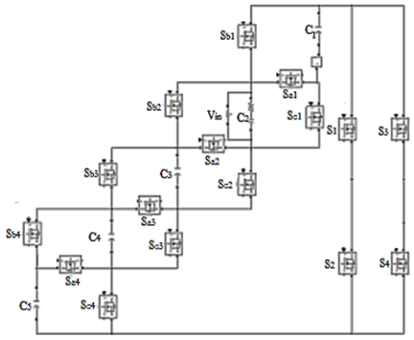

Fig.3 Circuit diagram of 11-level switched capacitor inverter

Compared with seven-level inverter the eleven-level inverter consists of 4 blocks in the circuit as shown in Fig.3. Here it consists of 16 switches and 5 capacitors so that output voltage is still higher than that of seven-level. The list of on state switches is tabulated as shown in Table2. Operation of 11-level SC inverter for each voltage for positive cycle is described.

B. *Modulation Technique*

The employed modulation technique is that phase disposition pulse width modulation (PDPWM). In this PWM technique all the carriers are picked out of same phase. Carrier wave is represented from e1 to e10 and the reference wave is represented as e_s as shown in Fig.4. Based on number of levels the carriers are decided. As the proposed inverter is of eleven-level, 10 carriers are considered with a reference wave. The PDPWM is widely used strategy for multilevel inverters as it provides load voltage and current with lower harmonic distortion. The drive signals of all the switches are obtained by comparing the sinusoidal reference wave with respective triangular carriers.

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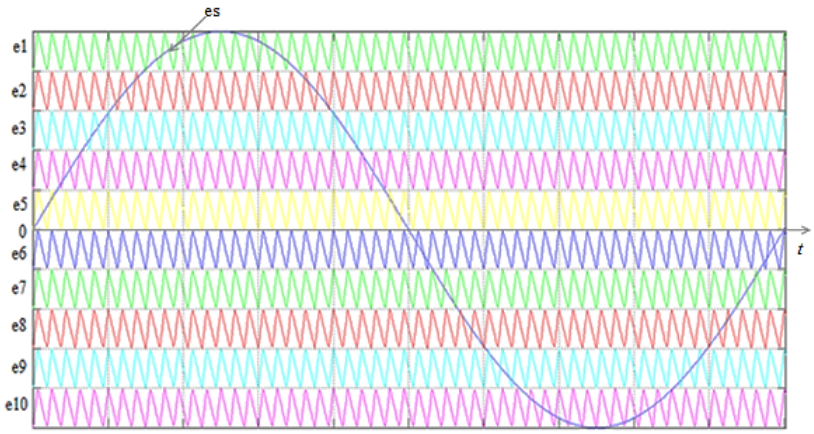


Fig.4 PDPWM Modulation Technique

C. Operation Modes Of 11-Level Inverter

1) *Zero voltage level:* It represents the zero voltage level here the on-state switches are S_2, S_4, S_{b1}, S_{c1}, S_{b2}, S_{c2}, S_{b3}, S_{c3}, S_{b4}, S_{c4}. But in this mode of operation the switches S_2 and S_4 are to be turned so that these two switches get short circuited and the current doesn't flow thus the voltage becomes zero.
2) *V_{in} voltage level:* Switches which are turned on in this mode are S_1, S_4, S_{b1}, S_{c1}, S_{b2}, S_{c2}, S_{b3}, S_{c3}, S_{b4}, S_{c4}. Here all the capacitors are connected in parallel with the voltage source. Here all the capacitors are in parallel to voltage source so the capacitors are charged.
3) *$2V_{in}$ voltage level:* Here switching sequences are S_1, S_4, S_{a1}, S_{b2}, S_{c2}, S_{b3}, S_{c3}, S_{b4}, S_{c4}. C_1 is connected in series with the voltage source and capacitors C_2, C_3, C_4, C_5 are connected in parallel with the voltage source.
4) *$3V_{in}$ voltage level:* The switching sequences are S_1, S_4, S_{a1}, S_{a2}, S_{b3}, S_{c3}, S_{b4}, S_{c4}. Here capacitors C_1, C_3 are connected in series and C_4, C_5 are in parallel with respect to voltage source.
5) *$4V_{in}$ voltage level:* The switching sequences are S_1, S_4, S_{a1}, S_{a2}, S_{a3}, S_{b4}, S_{c4}. Here, the capacitors C_1, C_3, C_5 are in series with voltage source and the capacitor C_4 is in parallel. So here the discharge time is more than the charging time.
6) *5Vin voltage level:* The switches which are in on state are S_1, S_4, S_{a1}, S_{a2}, S_{a3}, S_{a4}. Here all the capacitor i.e. C_1, C_2, C_3 and C_4 are in series with respect to voltage source. So that in this mode of operation complete discharge of capacitor takes place.

TABLE 2
LIST OF ON-STATE SWITCHES ON EACH STATE FOR 11-LEVEL

Relationship between e_s and e_k	On state switches	Ideal bus voltage
es > e1	S1 S4 Sa1 Sa2 Sa3 Sa4	5Vin
e1 ≥ es > e2	S1 S4 Sa1 Sa2 Sa3 Sb4 Sc4	4Vin
e2 ≥ es > e3	S1 S4 Sa1 Sa2 Sb3 Sc3 Sb4 Sc4	3Vin
e3 ≥ es >e4	S1 S4 Sa1 Sb2 Sc2 Sb3 Sc3 Sb4 Sc4	2Vin
e4 ≥ es >e5	S1 S4 Sb1 Sc1 Sb2 Sc2 Sb3 Sc3 Sb4	Vin
e5 ≥ es > e6	Sc4	0
e6 ≥ es > e7	S2 S4 Sb1 Sc1 Sb2 Sc2 Sb3 Sc3 Sb4	-Vin
e7 ≥ es > e8	Sc4	-2Vin
e8 ≥ es > e9	S2 S3 Sb1 Sc1 Sb2 Sc2 Sb3 Sc3 Sb4	-3Vin
e9 ≥ es > e10	Sc4	-4Vin
e10 ≥ es	S2 S3 Sb1 Sc1 Sb2 Sc2 Sb3 Sc3 Sa4	-5Vin
	S2 S3 Sb1 Sc1 Sb2 Sc2 Sa3 Sa4	
	S2 S3 Sb1 Sc1 Sa2 Sa3 Sa4	
	S2 S3 Sa1 Sa2 Sa3 Sa4	

Based on the 4n-1 output level waveform, the number of switching devices for proposed inverter of 7-level and 11-level are 10 and 16 switching devices respectively. Need of switching devices for the conventional SC inverter for 7-level are 20 and for 11-

level are 28. The conventional cascaded H-bridge (CHB) need 12 switching devices for 7-level and for 11-level it need 20 switching devices, whereas all the dc sources take the same voltage. So that proposed inverter has less number of switching devices than the conventional multilevel inverters.

IV. SIMULATION REULTS

In this work SC is modelled and simulated using the MATLAB software with its Simulink library and sim power system tool box. The MATLAB model of switched-capacitor with inverter connected system is shown in Fig.5 depending upon the low power and the high power. Switching device MOSFET is used for the low power and the device IGBT is used for high power. Here the simulation circuit is shown for the low power and the high power also similar to it i.e. replacing IGBT instead of MOSFET. Simulation parameters are given below for both conditions i.e. low power and high power which are same for 7-level and11-level.

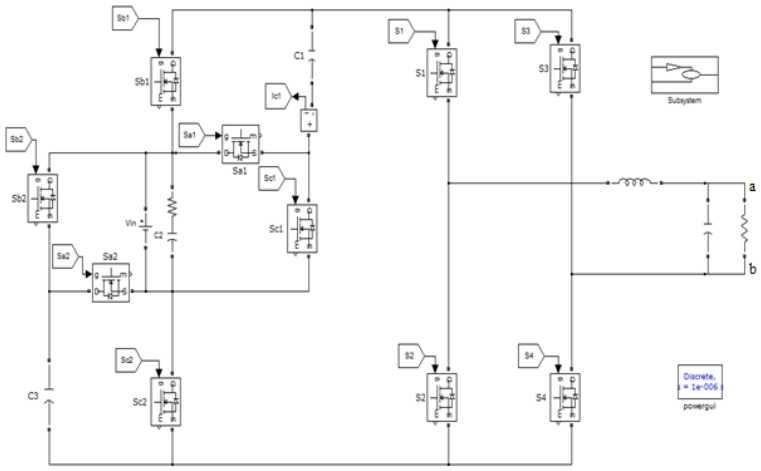


Fig.5 Simuation circuit for low power 7-level SC inverter

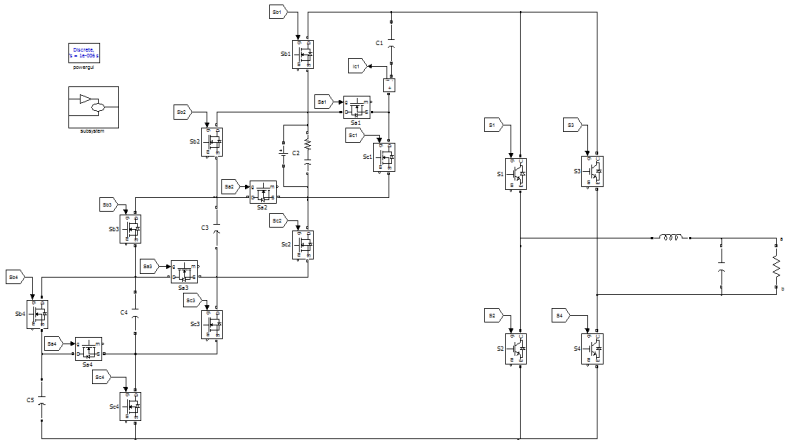


Fig.5 Simuation circuit for low power 11-level SC inverter

A. *Simulation Parameters*

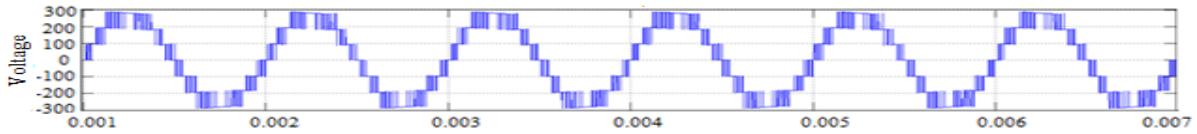
The low power inverter simulation was executed with MATLAB/SIMULINK under the following conditions. Where the MOSFET model internal resistance R_{on} = 0.54 [Ω], the snubber resistance R_s =10^5 [Ω] are used as switching devices. The input voltage V_{in} =8.00 [V], output resistance R = 50.0 [Ω], filter capacitance C and filter inductance L are C =0.45 [µF] and L =1.13 [mH], switching frequency f = 40.0 [kHz], reference waveform frequency f_{ref} =1.00 [kHz] and capacitance value C_k =143 [µF].

The high power inverter simulation was executed under the following conditions. Where the IGBT model internal resistance R_{on} = 65.0 [mΩ], snubber resistance R_s = 10^5 [Ω] are used as switching devices. The input voltage V_{in} = 100 [V], output resistance

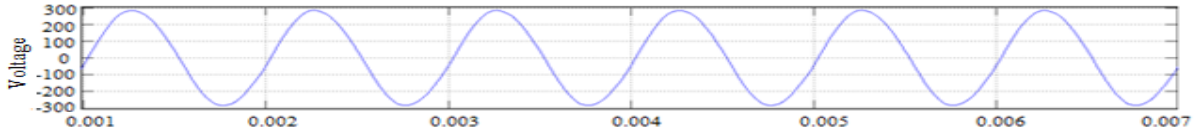
R = 10.0 [Ω], filter capacitance C and filter inductance L are C = 2.25 [μF], L = 225 [μH], switching frequency f = 40.0 [kHz], reference waveform frequency f_{ref} =1.00 [kHz] and capacitance C_k = 712 [μF]

B. Result Analysis

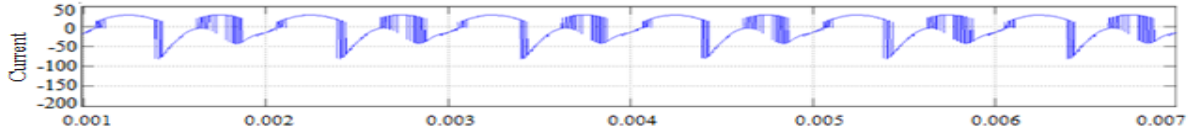
The performance of switched-capacitor is demonstrated for different voltages for 7-level, here results shown below are for high power and for low power. For high power the input voltage given is 100v and the output voltage is 300v as shown in Fig. 6(a). The input voltage given for the low power is 8v but the output voltage is 24v as shown in Fig. 7(a).



6(a)

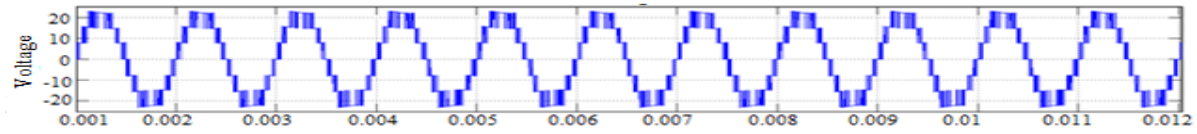


6(b)

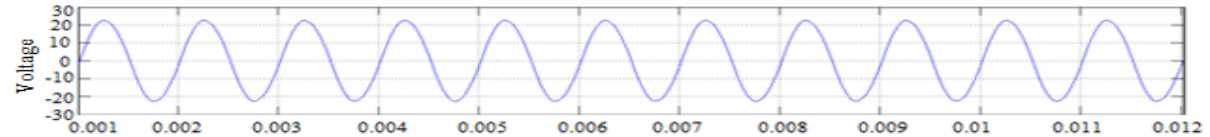


6(c)

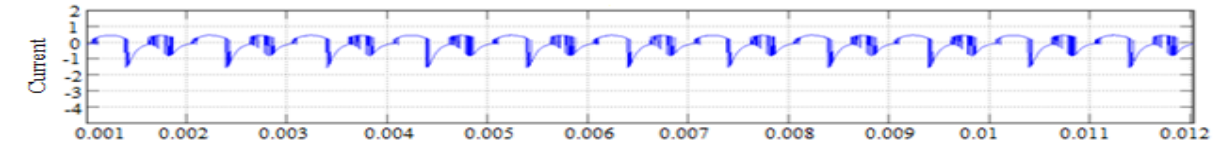
Fig.6 Simulation results for high power 7-level SC inverter, 6(a) shows the voltage before filters, 6(b) shows the output voltage after filters, 6(c) shows the current through capacitor



7(a)



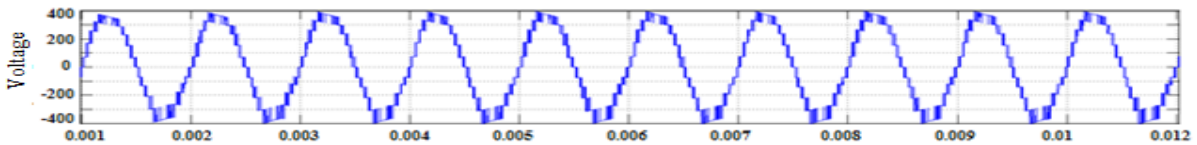
7(b)



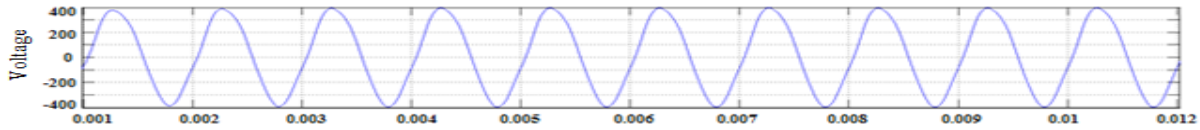
7(c)

Fig.7 Simulation results for low power 7-level SC inverter, 7(a) shows the voltage before filters, 7(b) shows the output voltage after filters, 7(c) shows the current through capacitor

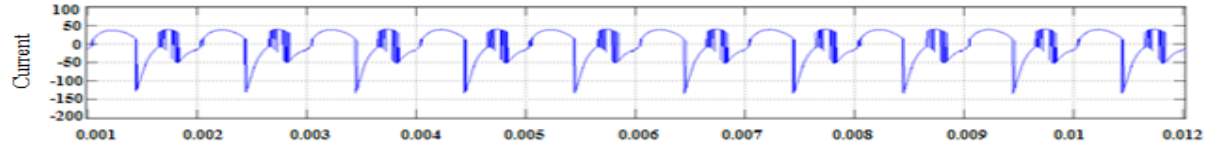
The performance of switched-capacitor is demonstrated for different voltages for 11-level, here results shown below are for high power and for low power. For high power the input voltage given is 100v and the output voltage is 400v as shown in Fig.8(a). The input voltage given for the low power is 8v but the output voltage is 30v as shown in Fig. 9(a).



8(a)

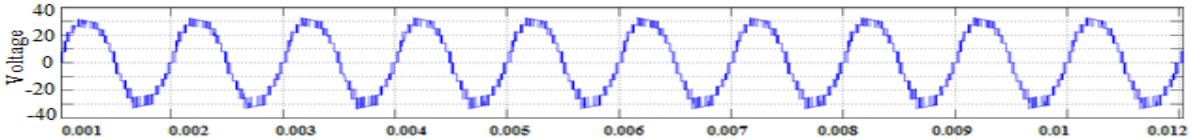


8(b)

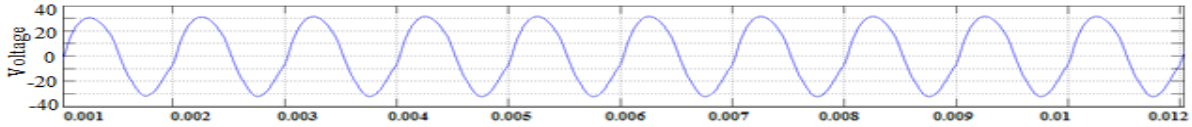


8(c)

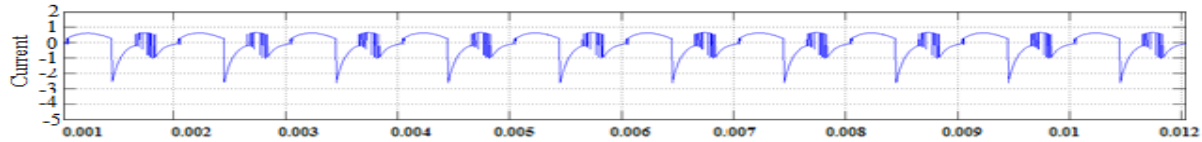
Fig.8 Simulation results for high power 11-level SC inverter, 8(a) shows the voltage before filters, 8(b) shows the output voltage after filters, 8(c) shows the current through capacitor



9(a)



9(b)



9(c)

Fig.9 Simulation results for low power 11-level SC inverter, 9(a) shows the voltage before filters, 9(b) shows the output voltage after filters, 9(c) shows the current through capacitor

THD values are obtained using FFT analysis during harmonic disturbances in the system. The below figures represent the inverter output voltage and Harmonic spectrum at different values and levels are analysed.

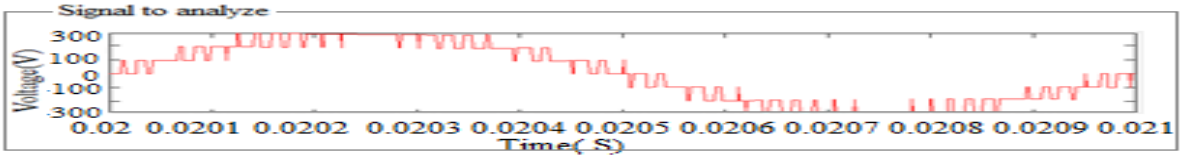


Fig. 10(a)

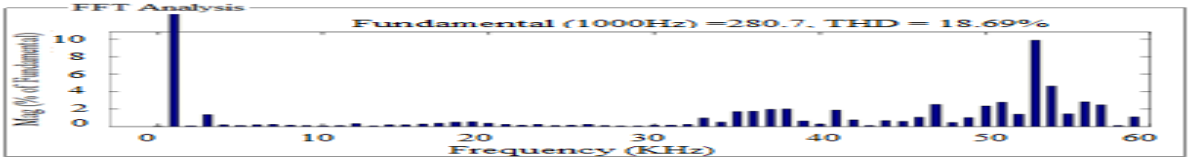


Fig. 10(b)

Fig. 10 Output Voltage and Harmonic Spectrum before filters for high power 7-level, Fig. 10(a) Inverter output voltage, Fig. 10(b) FFT Analysis

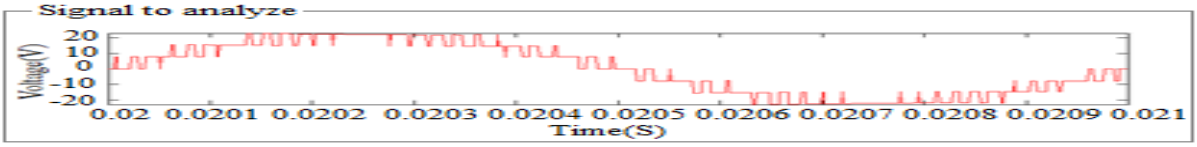


Fig. 11(a)

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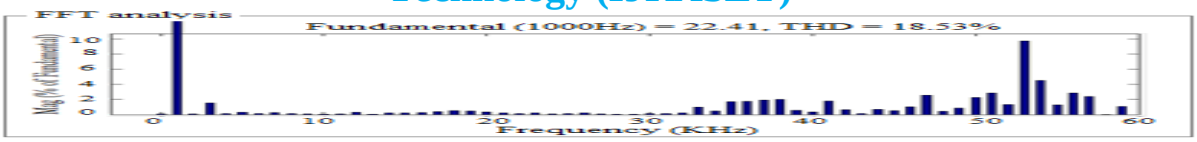

Fig. 11(b)

Fig. 11 Output Voltage and Harmonic Spectrum before filters for low power 7-level, Fig. 10(a) Inverter output voltage, Fig. 10(b) FFT Analysis

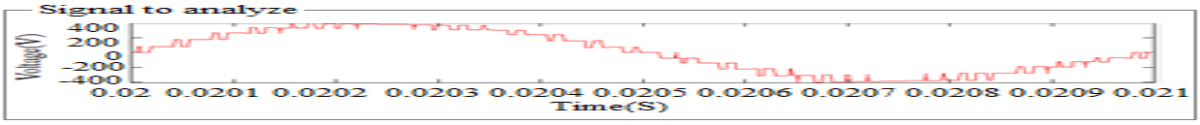

Fig. 12(a)

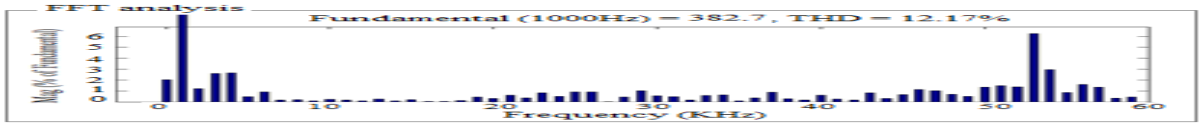

Fig. 12(b)

Fig. 12 Output Voltage and Harmonic Spectrum before filters for high power 11-level, Fig. 12(a) Inverter output voltage, Fig. 12(b) FFT Analysis

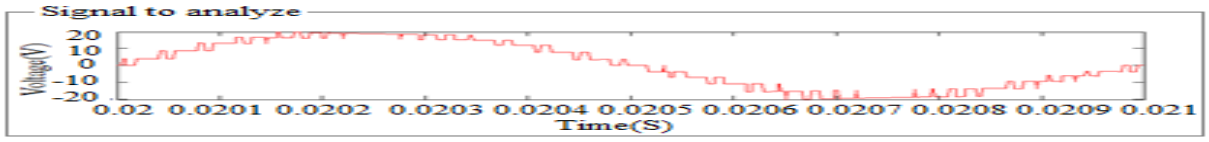

Fig. 13(a)

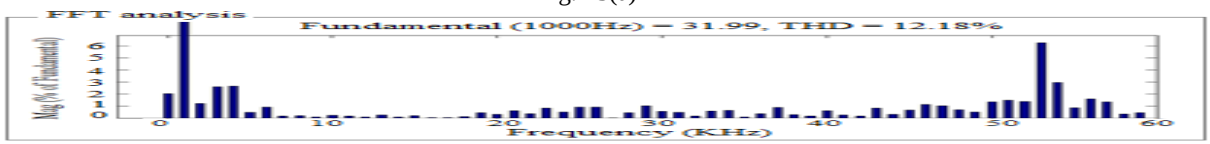

Fig. 13(b)

Fig. 13 Output Voltage and Harmonic Spectrum before filters for low power 11-level, Fig. 13(a) Inverter output voltage, Fig. 13(b) FFT Analysis

TABLE 3
COMPARING VOLTGAE & THD OF BOTH LEVELS

	Input Voltage (Volts)	**Output Voltage (Volts)**	**THD%**
7-Level SC inverter	100	300	18.69
	8	24	18.53
11-Level SC inverter	100	400	12.17
	8	30	12.18

V. CONCLUSION

In this work the operation of SC with different conditions are explained using series/parallel topology. The modulation method for the proposed inverter is shown. The circuit operation of the proposed inverter is altered by the simulation results with resistive load. The proposed inverter outputs larger voltage than the input voltage by switching capacitors in series and in parallel with less number of switches. The structure of the inverter is simple without any inductors in the circuit. By comparing both the levels total harmonic distortion of the inverter output waveform is reduced.

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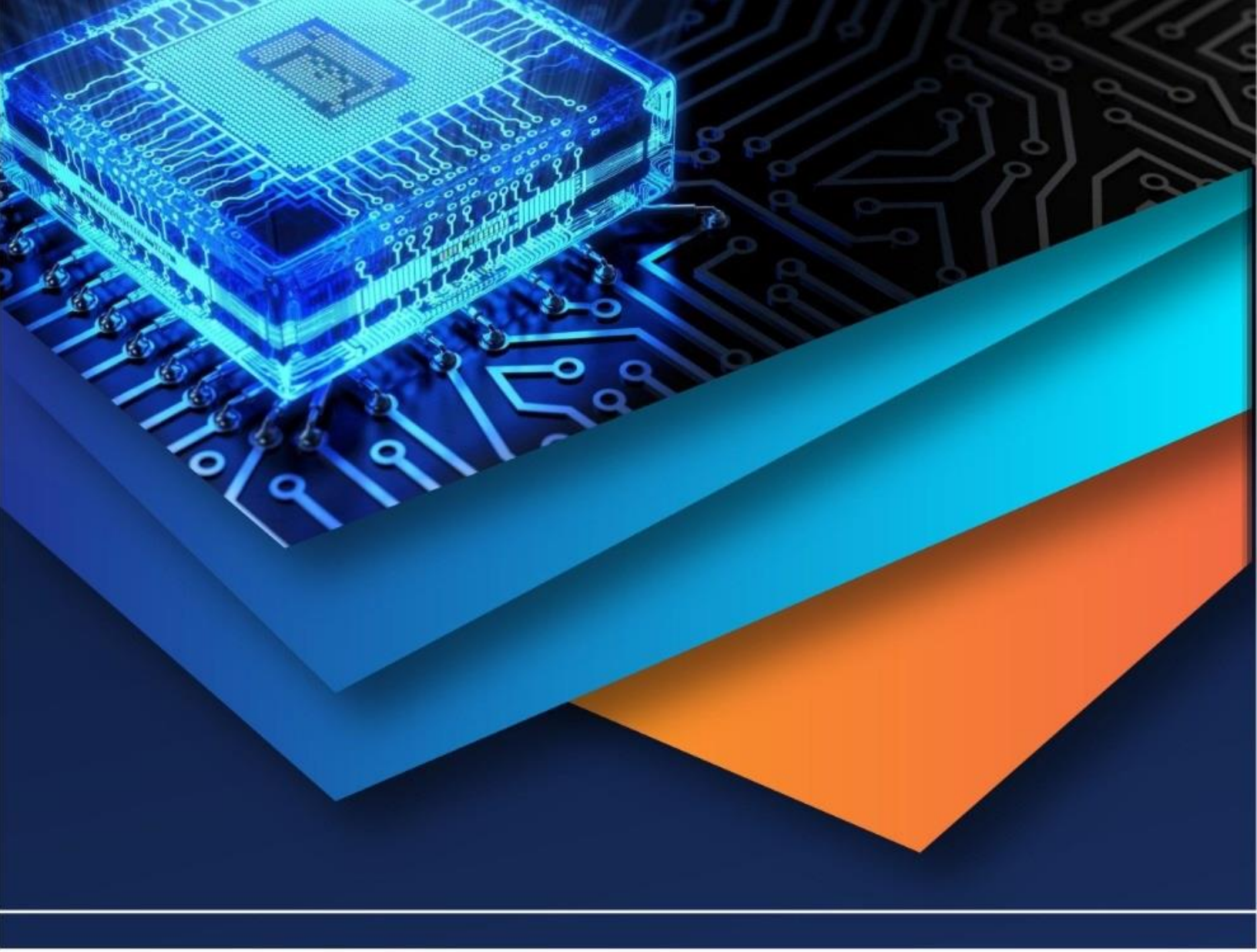

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