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Ultra Low Power Design of Full Adder Circuit using Adiabatic Logic Techniques

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Abstract: ***In many applications where there are a certain set of factors in which they play a major role in the overall development of the device. In the field of electronics, particularly in the field of VLSI, the integration of several devices like transistors and other CMOS circuits can be integrated on a single chip by considering all the required features to get a low power device. There are several techniques for the low power design of logic circuits; adiabatic logic technique is one of the best. The main theme of adiabatic logic is to reuse the energy like thermodynamic processes. The power dissipation and delay factors are very less compared to the designs using CMOS technology. By designing this type of circuit, we can use it in many of the applications where we specially require low power circuits including decoders, multiplexers, encoders and other logical circuits. By considering a circuit, like full adder (includes sum and carry) which is one of the most commonly used circuits in many applications, can be designed by using various adiabatic logic techniques and can be compared by considering various parameters and other non-adiabatic logics.***

Keywords: Integration, VLSI, adiabatic logic, full adder, low power circuit, thermodynamic process.

I. INTRODUCTION

In the current running world, there are many technologies which are developed on the basis of customer needs. As the world is heading towards a better future, many things are automated with the help of electronic equipment. These electronic materials include silicon chips which are fabricated using the integration of many electronic devices with a proper selection. There are many levels of integration which are required on the basis of the logic that is applied to design a particular application. As the advancement of transistors excluded the usage of diodes and vacuum tubes, similarly VLSI made the advancement of increase in many logics that were built around to develop the circuit.

Even though the increase in the regular devices has made the growth to an extent. But there is a shortage of many issues and hence, programmers are fixing the bugs to resolve many actions. Logical techniques such as XOR, AND, OR, CMOS, adiabatic are developed in order to solve the power issues and to raise the gain. Adiabatic logic is one of the efficient logic in preparing the circuit to become an efficient one.

Any circuit can be designed using adiabatic logic, but the purpose of selecting the full adder implies that the usage of this circuit in the many applications brings the need to develop it efficiently.

Addition is the one of commonly used fundamental arithmetic operations in many VLSI systems. Other almost the same math operations are address calculation, multiplication, division subtraction etc. Using binary things that add, the 1-bit full adder performance plays an important role in VLSI circuits. Different varieties of full adders implemented which are completely different logic designs and technologies, and they unremarkably aim at increasing speed and reducing power dissipation of the circuit. To improve the performance of full adder there are two methods. One of the methods is the ‘system level viewpoint’ method and the second method is the 'critical style view point’. In system level viewpoint method it consists of finding the longest signal path in the ripple adders and reduce the trail so that as to scale back the full signal path delay. The longest signal path is where the carry out bit of the most significant bit has to be calculated.

II. LITERATURE SURVEY

TIME DELAY (td) of a digital circuit mostly depends on the load capacitance value (C_L) and the driving current value. C_L comprises the output capacitance of the forcing gate, the input capacitance of the compelled gates, and the capacitance of interconnect.

PROPAGATION DELAY is the time lapse between application of an input change and change in output that propagates through the circuit. Each logic gate (AND, OR, Inverter etc.) has its own propagation delay. For single gates this delay is of less value around nanoseconds or shorter. However, this value may become significant as the circuit size increases and components are increased.

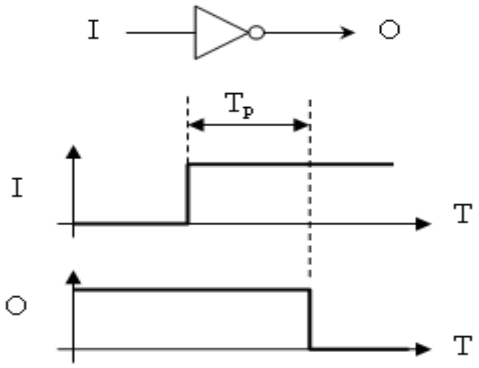


Fig 2.1 Propagation delay effect of an inverter

POWER-DELAY PRODUCT (PDP) is the product of power dissipation and delay of device.
PDP = power dissipation *delay
POWER CONSUMPTION is generated in dc condition is called quiescent power steady state power consumption. Power consumption is directly proportional to the power supply voltage (VDD) and power dissipation capacitance (Cpd).

$$PT=Cpd*f*VDD^2$$

Power consumption mainly depends on load capacitance (C_L). Power dissipation commonly occurs when load capacitance is charging low to high transition through PMOS transistor and the capacitor is discharging high to low transition through NMOS transistor.

$$PL=CL*f*VDD^2$$

The overall power dissipation is the sum of internal power dissipation along with load capacitance.

$$PD= PT + PL$$

STATIC POWER is the power dissipated when the circuit is inactive.
DYNAMIC POWER is the power dissipated when the circuit is active.
POWER DISSIPATION is the unwanted power that is produced out in the form of heat.

III. PROPOSED SYSTEM

A. Introduction To Adiabatic Logic

Adiabatic circuits use low power hardware circuits which utilizes "reversible logic" to save energy. In perfect adiabatic logic, every charge could be recycled (reused) a limitless number of times. So that a huge power dissipation lessening would be conceivable. Progressively figuring, such a perfect process can't be accomplished as a result of the nearness of dissipative components like resistances in a circuit.
There are established ways to deal with decreasing the dynamic power, for example, lessening supply voltage, diminishing physical capacitance and decreasing switching activity. Adiabatic logic chips are idea of switching circuit in which decreases the power by giving put away energy back to the supply. There are a few rules that are shared by all of these low power adiabatic systems. These turning switches are on when there is no potential difference exist over them, just turning switches off when no current is flowing through them, and utilizing a power supply that is prepared to do recouping or reusing vitality as electric charge.
In literature, there are two types of adiabatic circuits presented one is full adiabatic and other is quasi-adiabatic or partial adiabatic circuits. In most these practical cases two major types of power dissipation occurs in adiabatic circuit these are adiabatic loss and non-adiabatic loss. Adiabatic loss occurs in switching resistances when a current flow through the transistor and the non-adiabatic loss occurs due to threshold voltage.

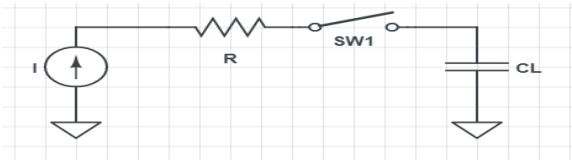


Figure 3.1: Adiabatic logic circuit

Here the load capacitance is charged by the constant current source while in conventional CMOS constant voltage source is used. Here R is the resistance of PMOS. A constant charging current flows along with a linear voltage ramp.
Assume the capacitor voltage is, at first, zero.
The Voltage across the switch = IR

$$P(t) = I^2R \quad \ldots\ldots\ldots\ldots (1)$$

Energy during charge $E = (I^2R)T$

Also $Q = C_L V_{dd}$, $I = \frac{C_L V_{dd}}{T}$ …… (2)

$$E = (I^2R)T = (\frac{RC_L}{T})C_L V_{dd}^2 \ldots\ldots\ldots (3)$$

Where E is the energy dissipated during the charge time.
Q is the charge transferred to the load,
C is the value of the load capacitance,
R is the on resistance of the PMOS switch,
V is the final value of the voltage at the load,
T is the charging time.
Theoretically the energy dissipation is nearly zero when the switching time of the driving voltage is long. When goes from HIGH to LOW discharging process takes place through the NMOS. The energy dissipation can be minimized by increasing the switching time. The energy dissipation is proportional to R. Thus, by decreasing the on-resistance of PMOS network will decrease the energy disappearing.

B. Adiabatic Logic Families

Adiabatic logics are classified into two types:

1) *Partially Adiabatic Logic (PAL):* It is a logic having non- adiabatic Loss present i.e. there is non-zero VDS across the transistor when it is being turned ON. It doesn't depend upon frequency. It is classified as shown below:

a) *Efficient Charge Recovery Logic (ECRL):* Efficient charge recovery logic (ECRL) proposed by Moon and Jeong. The below figure shows the Cross-coupled PMOS transistors are used in this design. An AC power supply is used for energy recovery purposes. With the help of out and outbar a constant load capacitance is derived by the power clock. Due to the use of cross-coupled PMOS full output swing is found in both pre charge recovery phase. When the voltage on the supply clock reaches to |Vtp| the PMOS transistor gets off and due to this the recovery path is disconnected which results in incomplete recovery. The ECRL circuits work on the principle of pipelining with four phase power clocks. The main disadvantage of ECRL is occurrence of coupling effect.

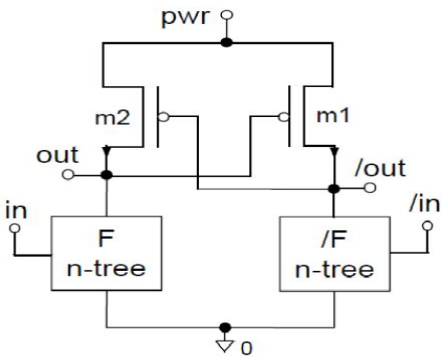


Fig 3.2 Schematic diagram of ECRL

Each power-clock cycle as shown in below figure consists of four intervals. In the evaluate (E) interval, the outputs are evaluated from the stable input signals. During the hold (H) interval, outputs are kept stable. Energy is recovered in the interval called recover (R). And for symmetry reasons, a wait (W) interval is inserted, as symmetric signals are easier and more efficient.

b) *Positive Feedback Adiabatic Logic (PFAL):* The partial energy recovery circuit named Positive Feedback Adiabatic Logic (PFAL) has been used, since it shows the most very little energy consumption.

i) *Modified Positive Feedback Adiabatic Logic (Modified PFAL):* The circuit diagram for modified PFAL adiabatic circuit is shown in figure implements basic Inverter functionality. It uses an additional drain gate connected NMOS transistor, in between the source and ground terminal of PFAL cross coupled inverters to reduce the power dissipation more than PFAL inverter design.

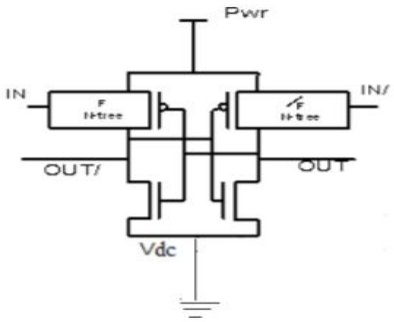


Fig 3.3 Modified Positive Feedback Adiabatic Logic (PFAL)

c) *2N-2N-2P logic:* To reduce the coupling effect in 2N-2P a new technique 2N2N2P was introduced. In 2N-2P structure the latch is designed only by two PMOSFETs while in 2N-2N-2P technique two PMOSFETs and two NMOSFETs are used. The more cross coupled N-MOS switches results a non-floating output of the recovery phase. The schematic representation of 2N-2N2P inverter is shown in the figure below. In this technique four phase clocking is used i.e. ``evaluation ‘, 'hold ‘, 'recover ‘and' wait

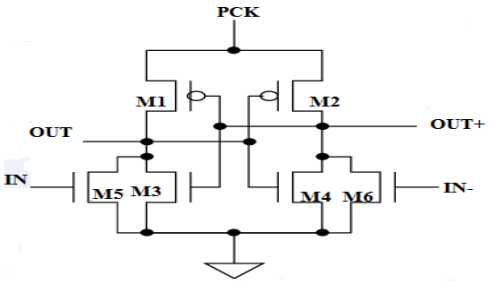


Fig 3.4 Schematic of 2N-2N-2P inverter

d) *Clocked Adiabatic Logic (CAL):* Clocked Adiabatic Logic is dual rail logic which can be operates from a single-phase AC power clock signal. The on-chip switching and small external inductor circuits are used to create the power clock supply waveform in adiabatic mode. The schematic of basic CAL gate inverter is shown in below figure. It consists of cross coupled inverters to provide memory function. An extra timing control clock signal CX has been used. This has been introduced to control the transistors that are connected in series with the logic trees represented by the functional blocks F and F’. The clocked enable devices that allow the operation with a single power clock signal.

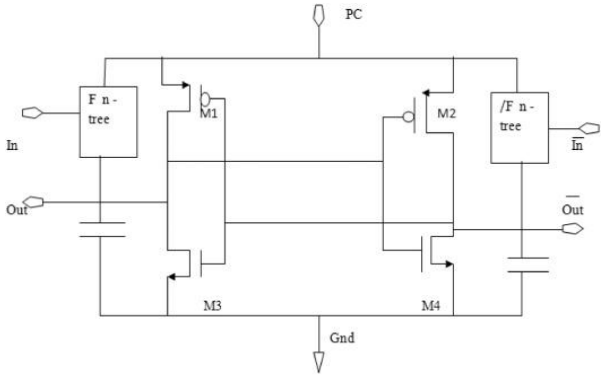


Fig 3.5 Clocked Adiabatic Logic (CAL)

2) Fully Adiabatic Logic: Fully adiabatic logic is a logic having non -adiabatic loss absent. It depends upon frequency.
It can be classified as shown below:

a) Pass Transistor Logic (PTL)
b) Split Rail Charge Recovery Logic (SCRL)

i) Pass Transistor Logic (PTL): The below shows the description about pass transistor logic.

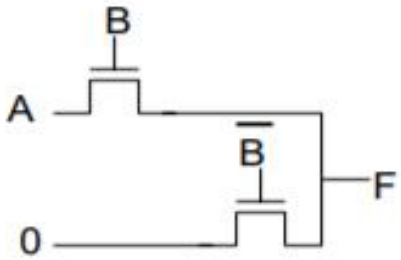


Fig 3.6 Pass Transistor Logic (PTL)

In ordinary logic families, input signal is applied to the gate terminal of the transistor but in PTL it is applied to source or drain terminal. These circuits act as switches and are use either NMOS transistors or parallel pairs of NMOS and PMOS transistor called transmission gate.
Here, the width of PMOS is taken and it is equal to NMOS so that both transistors can pass the signal at the same time in parallel.
The main advantage of PTL is it has fewer devices to put into use the logical functions as compared to CMOS.

IV. FULL ADDER IMPLEMENTATION BLOCK DIAGRAMS OF THE LOGICS IN THIS METHODS

A. Partial Feedback Adiabatic Logic (PFAL) Full Adder Circuit

The below shows the block diagram representation of PFAL full adder.

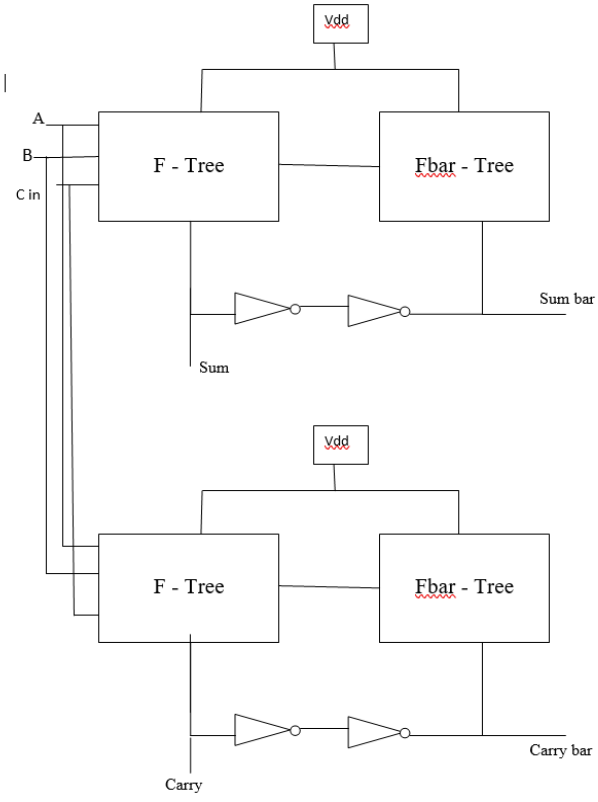
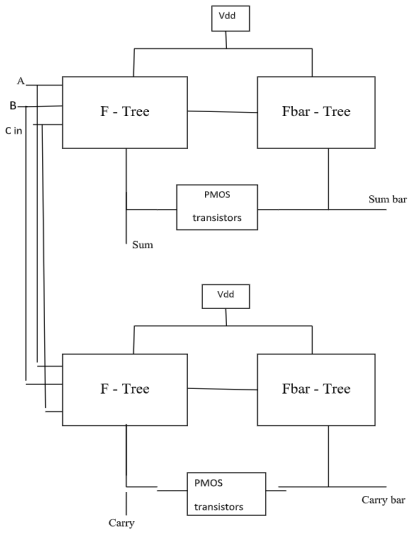


Fig 4.1 Block diagram of PFAL FA

B. Efficient Charge Recovery logic (ECRL) full Adder Circuit

The below shows the block diagram representation of ECRL full adder.



4.2 Block diagram of ECRL FA

C. Pass Transistor Logic (PTL) full adder Circuit

The below shows the block diagram of PTL full adder.

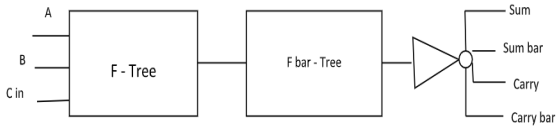


Fig 4.3 Block diagram of PTL FA

V. SIMULATION RESULTS

In order to know the usage of adiabatic logic, we have to consider a circuit and apply that logic to that particular circuit and have to analyse it by giving the proper inputs.

The below shows the schematic and simulation analysis of various adiabatic logics and also for a conventional CMOS logic of a full adder circuit. They various logics are listed below:

A. Conventional CMOS Full Adder

1) Schematic analysis and Simulation analysis of conventional CMOS FA

The below figure shows the schematic analysis and Simulation analysis of conventional CMOS full adder (FA).

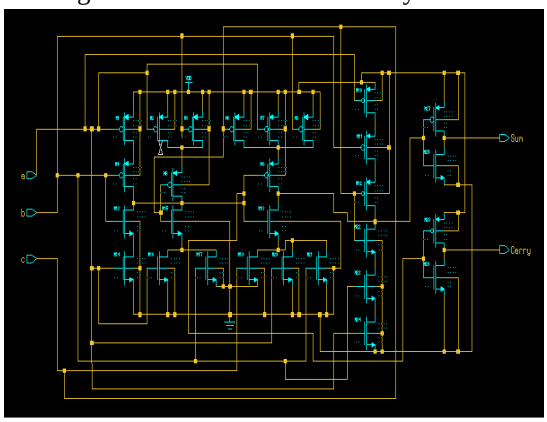


Fig 5.1 Schematic analysis of conventional CMOS FA

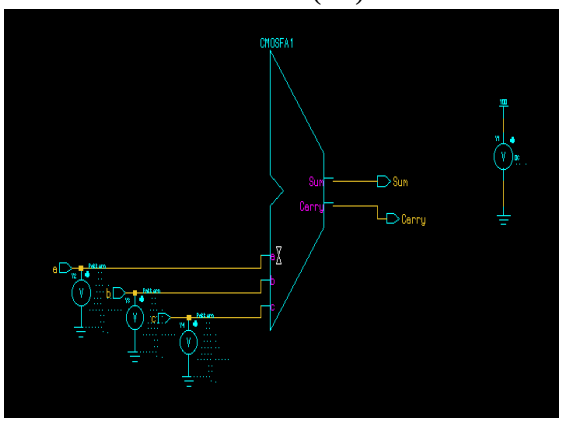


Fig 5.2 Simulation analysis of conventional CMOS FA

The below shows the inputs A, B, C and the outputs sum (S) and carry (C) given to CMOS FA

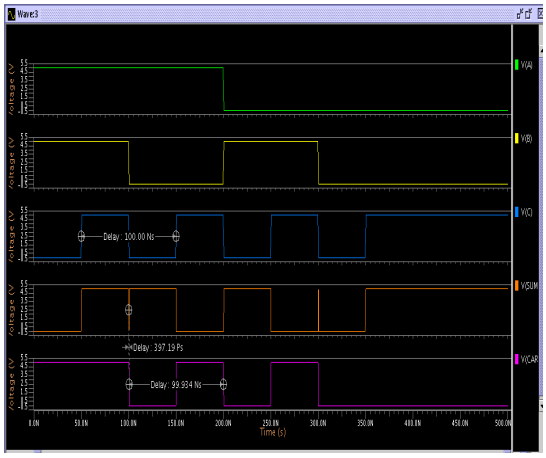


Fig 5.3 Parameter Analysis of conventional CMOS FA (inputs and outputs)

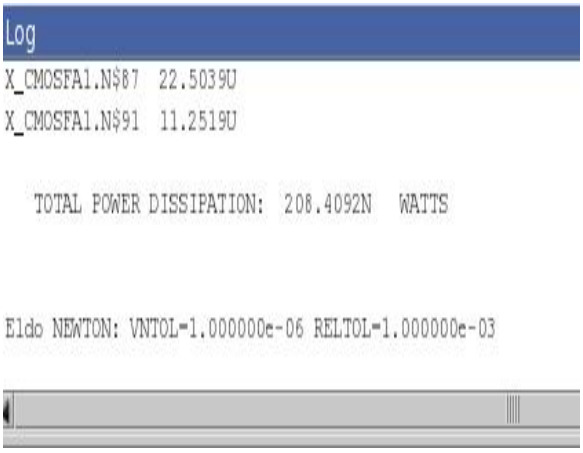


Fig 5.4 Parameter analysis

B. Partial Feedback Adiabatic LOGIC FA (PFAL FA)

1) Schematic analysis and Simulation analysis of PFAL FA

The below shows the schematic analysis of PFAL FA

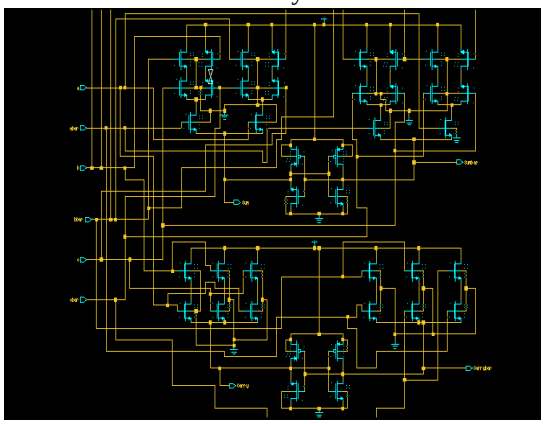


Fig 5.5 Schematic analysis of PFAL FA

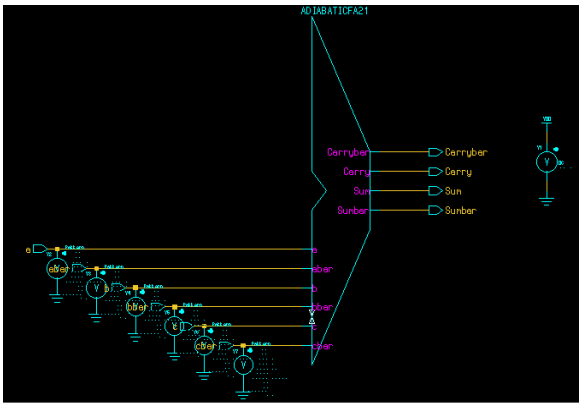


Fig 5.6 Simulation analysis of PFAL FA

2) Simulation results of PFAL FA

The below shows the inputs A, B, C and Abar, Bbar, Cbar and Sum, Carry and Sumbar, Carrybar given to PFAL FA

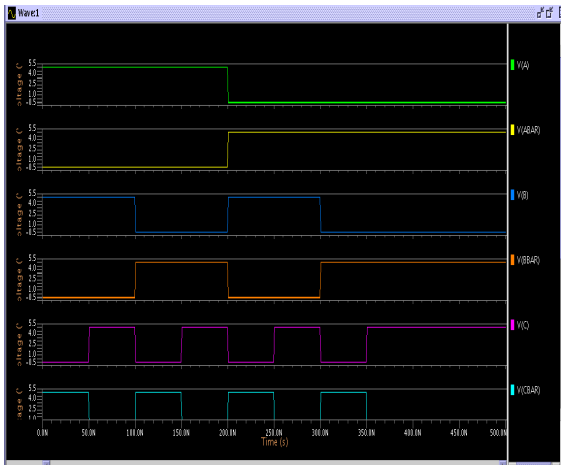


Fig 5.7 Simulation waveform of PFAL FA (inputs)

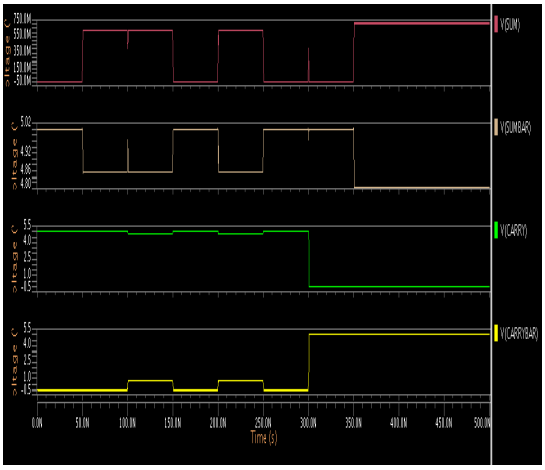


Fig 5.8 Simulation waveform of PFAL FA (outputs)

3) Analysis of parameters from PFAL FA

The below figures shows the parameter analysis of PFAL FA (Delay and power dissipation).

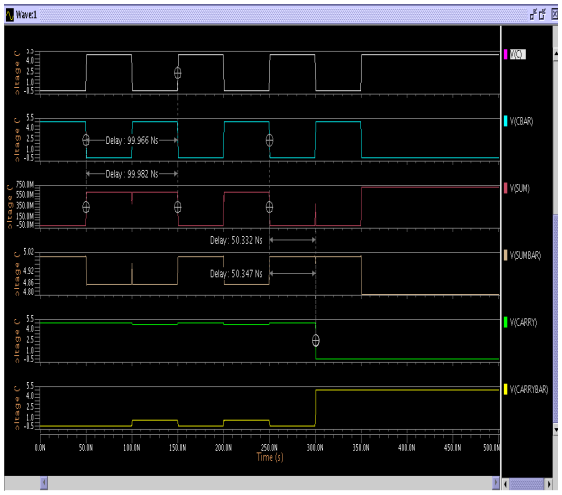


Fig 5.9 Parameter analysis of PFAL FA (Delay)

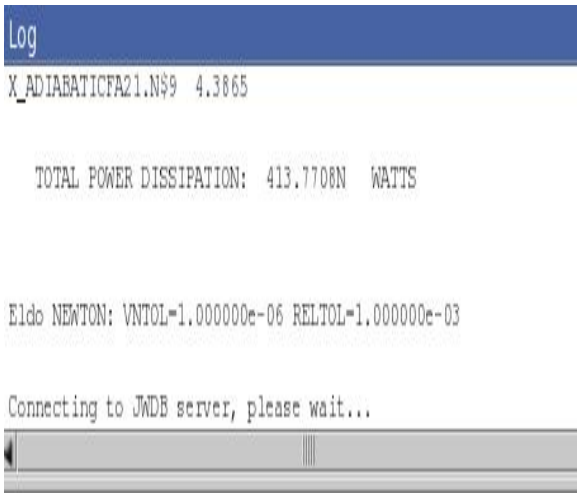


Fig 5.10 Parameter analysis of PFAL FA (Power dissipation)

C. Efficient Charge Recovery logic FA (ECRL FA)

1) Schematic analysis and Simulation analysis of ECRL FA

The below shows the schematic analysis and simulation analysis of ECRL FA

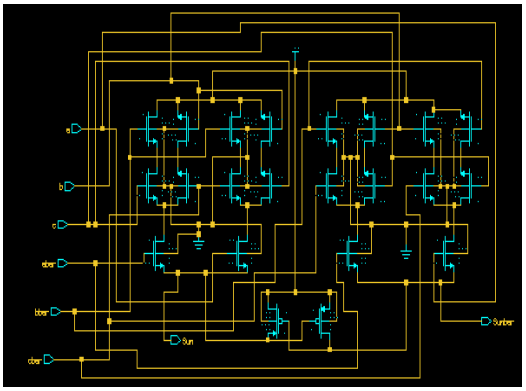


Fig 5.11 Schematic analysis of ECRL FA (Sum)

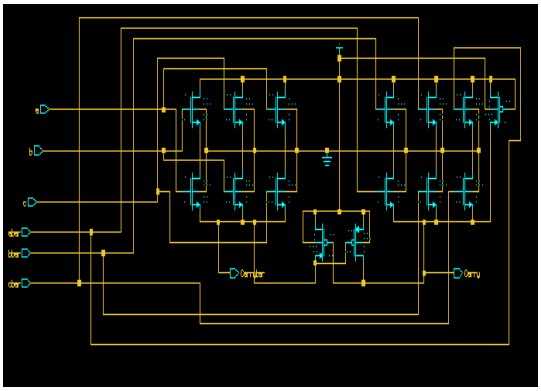


Fig 5.12 Schematic analysis of ECRL FA (Carry)

2) Simulation analysis and Simulation results of ECRL FA

The below shows the simulation analysis and inputs A, B, C and Abar, Bbar, Cbar given to ECRL FA of ECRL FA

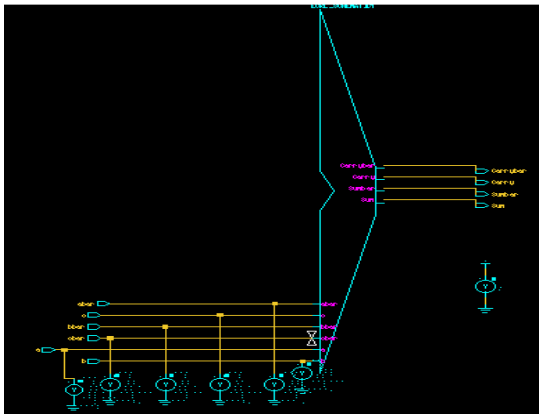


Fig 5.13 Simulation analysis of ECRL FA

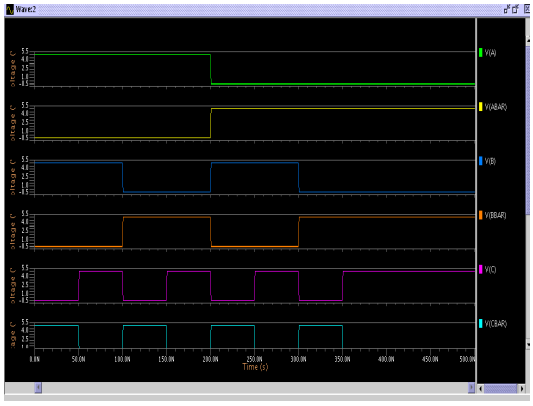


Fig 5.14 Simulation waveform of ECRL FA (inputs)

The below shows the outputs Sum, Carry and Sumbar, Carrybar and analysis parameter of ECRL FA

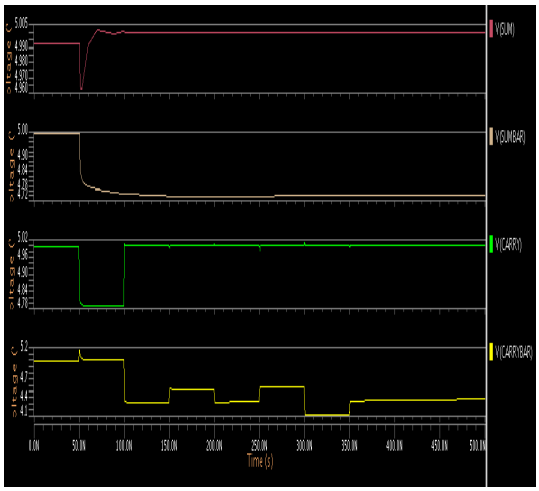


Fig 5.15 Simulation waveform of ECRL FA (outputs)

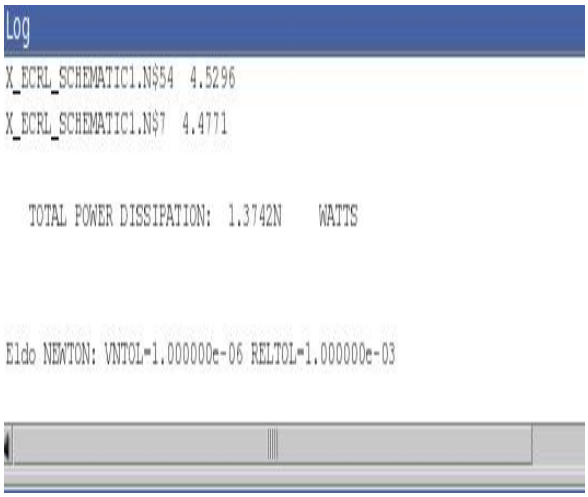


Fig 5.16 Parameter analysis of ECRL FA (Power dissipation)

D. Pass Transistor Logic FA (PTL FA)

1) Schematic analysis and Simulation analysis of PTL FA

The below shows the schematic analysis and simulation analysis of PTL FA

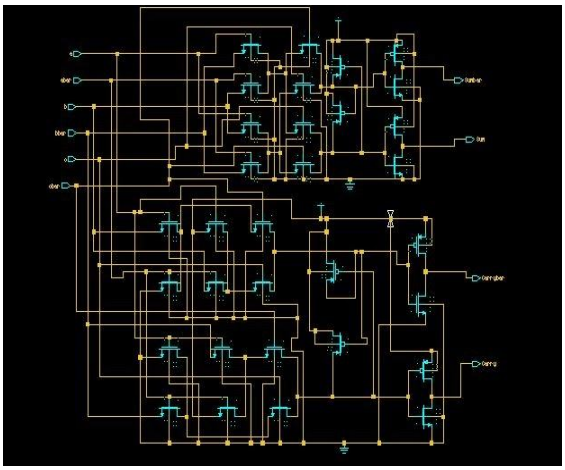


Fig 5.17 Schematic analysis of PTL FA

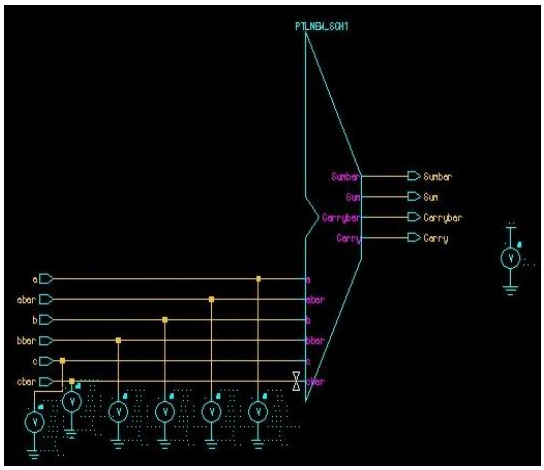


Fig 5.18 Simulation analysis of PTL FA

2) Simulation results of PTL FA

The below shows the inputs A, B, C and Abar, Bbar, Cbar and outputs Sum, Carry and Sumbar, Carrybar of PTL FA

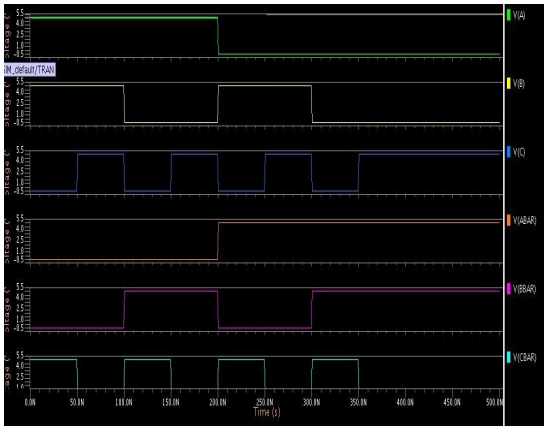


Fig 5.19 Simulation waveform of PTL FA (inputs)

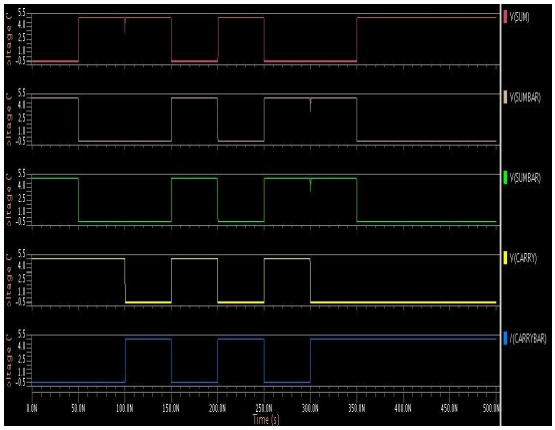


Fig 5.20 Simulation waveform of PTL FA (outputs)

3) Analysis of parameters from PTL FA

The below figures shows the parameter analysis of PTL FA (Delay and power dissipation).

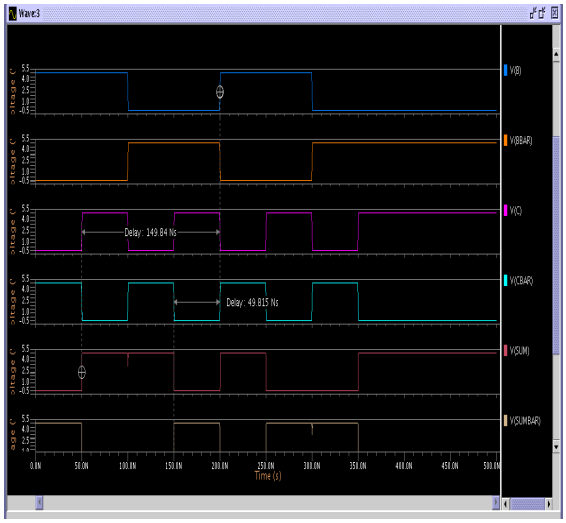


Fig 5.21 Parameter analysis of PTL FA (Delay)

```
Log
K_PTLNEW_SCH1.N$71  5.0000
K_PTLNEW_SCH1.N$74  4.4630
K_PTLNEW_SCH1.N$77  4.6180
K_PTLNEW_SCH1.N$90  208.1105P
K_PTLNEW_SCH1.N$92  12.0755U

   TOTAL POWER DISSIPATION:  488.0298N   WATTS


Eldo NEWTON: VNTOL=1.000000e-06 RELTOL=1.000000e-03
```

Fig 5.22 Parameter analysis of PTL FA (Power dissipation)

VI. COMPARISON TABLE OF VARIOUS PARAMETERS

The below shows the comparison table of various parameters for the below mentioned logics:

A. Conventional CMOS FA
B. PFAL FA
C. ECRL FA
D. PTL FA

The below table shows the comparison table of different parameters between various adiabatic logics.

S.no.	Parameter	Conventional CMOS	PFAL	ECRL	PTL
1	Type	General CMOS	PAL	PAL	FAL
2	Technology	130nm	130nm	130nm	130nm
3	No. of PMOS	14	4	5	5
4	No. of NMOS	14	36	32	24
5	Total (P+N)	28	40	37	32
6	Area	Less	More	Less compared with PFAL	Less compared with ECRL
7	Complexity	Less	More	Less compared with PFAL	Less compared with ECRL
8	W / L	P - 0.52:0.13 N - 0.26:0.13	P - 0.52:0.13 N - 0.26:0.13	P - 0.52:0.13 N - 0.26:0.13	P - 0.52:0.13 N - 0.26:0.13
9	Delay	99.707ns	50.059ns	47.235ns	49.815ns
10	Power dissipation	208.4092nw	413.770nw	1.3443nw	488.0298nw
11	Cross-couple	No	PMOS - 1 NMOS - 1	PMOS - 1	No
12	Reuse of energy	No	50-70%	50-70%	55-75%
13	Applications	General	Effective	More Effective	Effective

VII. CONCLUSION

A good electronic device is that, it has to have good battery backup, high gain, long term of usage and other. To maintain these factors, a particular circuit can be developed by a specified logic and hence, the particular output can be attained. Adiabatic logic is one of the developed logic in which a lot of power can be consumed. A large amount of dissipated power can be used back for reusing it with the help of proper logical circuits. Full adder is one of the most commonly used circuits in many of the applications. Hence, full adder is designed by using these adiabatic logic techniques and compares various parameters among these logics with a conventional CMOS full adder.

REFERENCES

[1] M.Shyam Sundar, Yashpal Singh, "Ultra low power design of sequential logic circuits using adiabatic logic," IJVDCS., vol. 4, Issue 3, pp. 0235-0238, March 2016.
[2] Baljinder Kaur , Narinder Sharma , Gurpreet Kaur, "An efficient adiabatic full adder design approach for low power," IJARSE., vol. 5, Issue 5, pp. 121-127, May 2016.
[3] Mehar Sharma , Neeraj Gupta , Rashmi Gupta, "Power reduction techniques in VLSI," IJETMR., vol. 5, Issue 2, pp. 123-129, Feb. 2018.
[4] Satyendra Kumar, Ram Raksha Tripathi, "Adiabatic Logic Circuits for Low Power, High Speed Applications," IJSTE., vol. 3, Issue 10, pp. 121-128, April 2017.
[5] S.Dhivya, A.Nithya, "Design and analysis of power efficient full adder in 30nm technology," IJPAM., vol. 118, Issue 20, pp. 763-771, Special Issue.
[6] M.A.H.Sowmya , P.Sharmila Rani, "Static loss reduction analysis on full adder using power gating technique," IJESC., vol. 1, Issue 1, pp. 569-574, May 2014.
[7] Ankammarao Gudi Seva, "Reduction of leakage power in full adder using power gating analysis," IJRSSET., vol. 2, Issue 12, pp. 32-37, Dec 2015.
[8]]Bhakti Patel, Poonam Kadam, "Comparative Analysis of Adiabatic Logic Techniques",IJCA,Sept.2015.
[9] S. Kim, C. H. Ziesler, and M. C. Papaefthymiou, "Charge-recovery computing on silicon," IEEE Trans. Computers, vol. 54, no. 6, pp. 651–659, June 2005.
[10] J. Marjonen, and M. Aberg, "A single clocked adiabatic static logic – a proposal for digital low power applications," J. VLSI Signal Processing, vol. 27, no. 27, pp. 253–268, Feb. 2001.
[11] V. I. Starosel'skii, "Adiabatic logic circuits: A review," Russian Micro- electronics, vol. 31, no. 1, pp. 37–58, 2002.
[12] Renuka Verma, Rajesh Mehra, Area Efficient Layout Design Analysis of CMOS Barrrel Shifter, EATHD-2015 Conference Proceeding, 14-15 March, 2015.

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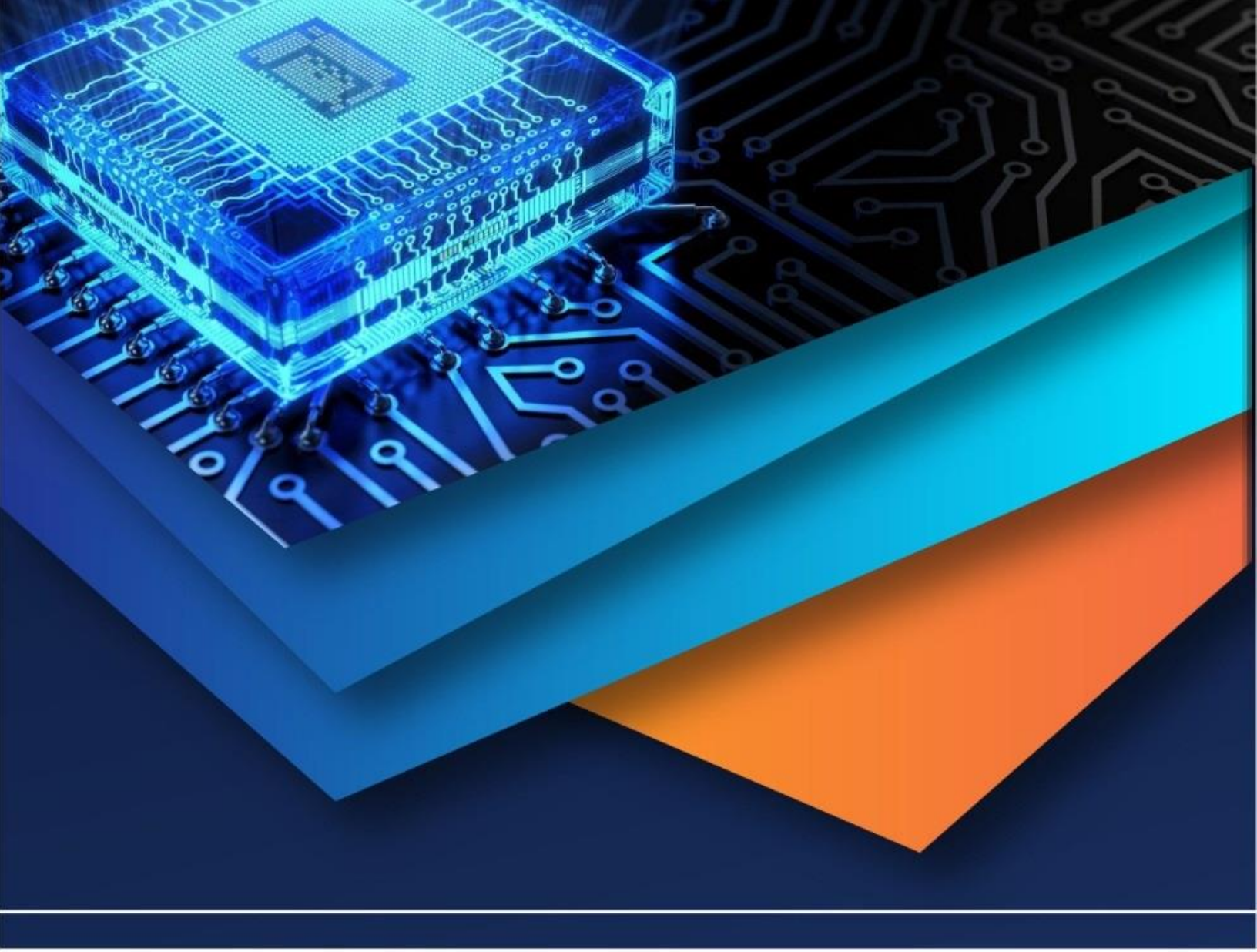

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