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Comparison of CNTFET Inverter with CMOS Inverter

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Abstract: ***In the world of VLSI circuits, CMOS has lost its importance while scaling below 32nm due to high power consumption and high leakage current. Scaling down of CMOS devices causes short channel effects which cause an exponential increase in the leakage current and power dissipation and are difficult to suppress. These are the major short comes of CMOS transistors. CNT-FET have a better control over a thin silicon body which overcomes these limitations. Enormous progress has been made to scale transistors to even smaller dimensions to reduce time delay in operation that will help to obtain fast switching transistors and also reduce the overall power consumption. Although the device characteristics are improved; the high active leakage problem is still not solved. CNT-FET is a better substitute to bulk CMOS technology because of less short channel effect and similar fabrication steps to that of the existing standard CMOS technology. CNTFET device has better controllability, resulting in high on/ off ratio. CNTFET devices can be used to enhance the performance by reducing the leakage current and average power dissipation. The figure of merit of CNTFET is better than CMOS technology. This research covers the characteristics of CNTFET inverter being modelled in HSPICE software using CMOS structures and CNT-FET structure, are compared and their performances like power consumption and speed are analysed.***

Keywords: **Short channel effects, CMOS, CNTFET, Figure of Merit, HSPICE**

I. INTRODUCTION

Silicon-based microcircuit technology is approaching its physical limit because of the device dimensions scale to the nanometre regime. In the post-silicon era, nanotube FET (CNTFET) may be a promising candidate for future integrated circuits due to its excellent properties like near ballistic transport, high carrier mobility (10^3–10^4 $cm^2/V{\cdot}s$) in semiconducting carbon nanotube (CNTs) and easy integration of high-k dielectric material resulting in better gate electrostatics. CNTs are basically hollow cylinders of rolled-up graphene sheet composed of 1 or more concentric layers of carbon atoms during a honeycomb lattice arrangement. Depending on the direction during which the nanotubes are rolled (chirality), they will be either metallic or semiconducting. In a nanotube, low bias transport is often nearly ballistic across distances of several hundred nanometres and it's attractive for nano electronic applications thanks to its excellent electrical properties. CNTFET has gained global attention as an alternative to nanoscale CMOS technology. Due to the similar I-V characteristics of CNTFET as that of MOS devices, qualitatively most of the CMOS circuits are often implemented using CNTFET. Carbon Nano Tube field-effect transistors (FETs) overcome these problems due to tighter control of the channel potential by using gate-all-around CNTFETs, gates wrapped around the body. Amongst FETs, CNTFETs have emerged because of the best candidate structures from a fabrication perspective. In our research work, we have used HSPICE model for CNTFET. The VLSI circuits like Inverter circuit, logic levels are represented in terms of voltage value for computation. The work emphasis on I-V characteristics of CNTFET. The CNTFET model is implemented in Verilog and simulated in Hspice for the circuit simulation of inverter circuit and therefore the performances are evaluated. The simulation results depict an excellent performance on power and speed of operation.

II. V-I CHARACTERISTICS OF CNTFET INVERTER

The circuit suitable model of CNTFET has been successfully executed in Verilog. In order to demonstrate the flexibility of this model, we employed it to style basic logic gate inverter. This CNTFETs behaviour is mostly the same as the traditional MOSFET. The p-type characteristics are obtained when the polarity-gate voltage is about to -0.2V and therefore the n-type characteristics are obtained when the polarity-gate voltage is about to +0.2V. These CNTFETs are used to design circuits replacing the normal MOS transistors. To implement the simulation of those circuits we randomly decided to use 900 mV power supply and supposed that the flat-band voltages are adequate to +450 mV and -450 mV for n-type and p-type CNTFETs.

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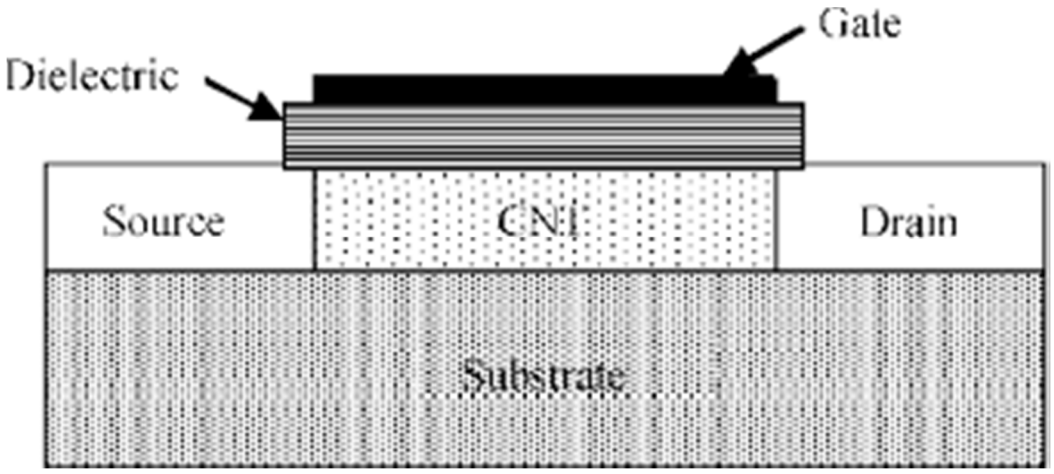

Fig (a)

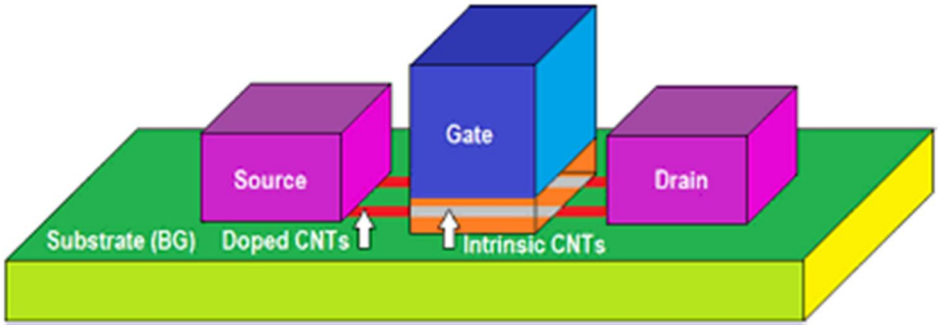

Fig (b)

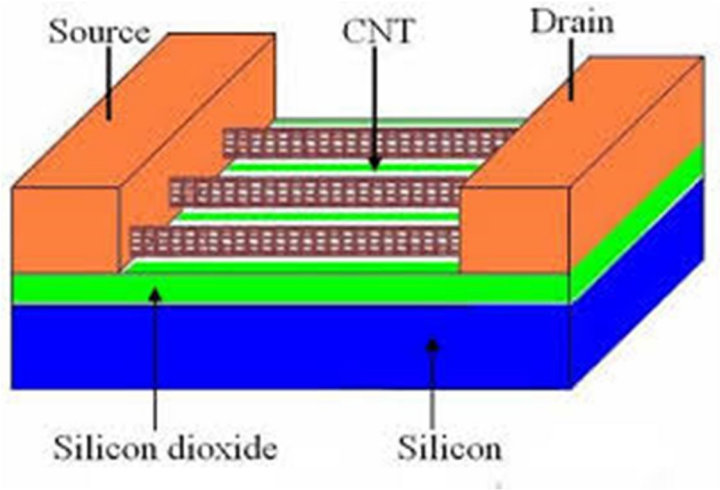

Fig (c)

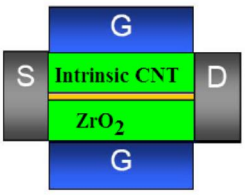

Fig (d)

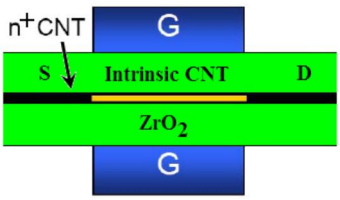

Fig (e)

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III. TYPES OF CNTFET

Carbon Nanotube FETs (CNTFETs): The Carbon nanotube field effect transistor (CNTFET) is one of the most promising candidates for next generation electronics and sensors. The first carbon nanotube field effect transistors were announced in 1998. They were normal devices fabricated by adding single wall CNTs (synthesized by laser abscission) from solution onto oxidized Silicon wafers which were first treated with gold or platinum electrodes. The electrodes acted as source and drain, connected through the nanotube channel, and the doped Silicon substrate acted as the gate. CNTFET's can be classified into: Back-gated CNTFET's, Top-gated CNTFET's, Wraparound gate CNTFET's, Suspended CNTFET's, Multi-Wall CNTFET's and Vertical CNTFET's. The CNT fabricated device that is highly explored is the carbon nanotube field effect transistor (CNTFET), composed of single wall CNTs (SWCNTs) as the active element between two metal source and drain contacts. Although there are many advantages to the CNTFET, such as size, high sub-threshold slope, and low power consumption. There are two main methods for CNT creation: CVD Growth & CNT Solution Deposition.

Single-Wall CNTFET's: There are a few types of architecture of Single-wall Carbon Nanotube FET - (SWNTFET): Back-gated CNTFET's, Top-gated CNTFET's, Wrap-around gate CNTFET's, Suspended CNTFET's, Vertical CNTFET, Local-gated single-walled CNTFET.

Multi-Wall CNTFET's: The multiwall carbon nanotubes structure is complex therefore they are not studied in detail. Every multiwall carbon nanotubes are metal or semiconductor with distinct chirality.

IV. CNTFET MATERIAL CONSIDERATIONS

There are some general decisions to be made when considering what materials to use when fabricating a CNTFET. Semiconducting single-walled carbon nanotubes are preferred over metallic single-walled and metallic multi-walled tubes since they're ready to be fully transitioned, a minimum of for low source/drain biases. A lot of efforts have been made into finding an appropriate contact material for semiconducting CNTs; the simplest material so far is Palladium, because its work function matches closely with that of nanotubes and it adheres to the CNTs quite well.

V. PROJECT IMPLEMENTED USING WRAP AROUND GATE CNFET'S

Wrap-around gate CNTFETs as shown in Fig. (f), also known as gate-all-around CNTFETs were developed and are a further improvement upon the top-gate device geometry. In this device, the entire circumference of the nanotube is gated instead of gating just the part of the CNT that is closer to the metal gate contact. This improves the electrical performance of the CNTFET, reducing leakage current and improving the device on/off ratio.

The first step of device fabrication is wrapping CNTs in a gate dielectric and gate contact using atomic layer deposition. Then these wrapped nanotubes are solution-deposited on an insulating substrate, where the wrappings are partly etched off, leaving the ends of the nanotube exposed. Then the source, drain and gate contacts are deposited onto the CNT ends and the outer metallic gate wrapping.

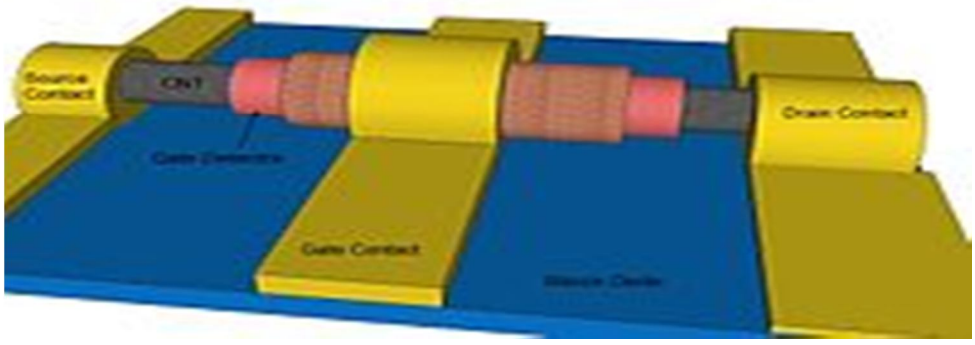

Fig (f)

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VI. COMPARISON TO MOSFETS

CNTFETs have different characteristics compared to MOSFETs in their performance. The on-current advantage is because of the high gate capacitance and improved channel transport. The compatibility with high- k gate dielectrics becomes a definite advantage for CNTFET's since the effective gate capacitance per unit width of CNTFET is approximately double that of p-MOSFET. The carrier velocity of CNTFET's is about two times higher than MOSFET's, which comes from the increased mobility and the band structure. In addition, CNTFET's have around four times higher transconductance.

Despite its double gate structure, the CNTFET is closed to its root, i.e. the conventional MOSFET in layout and fabrication. The Wrap-All Around gate Stanford CNTFET model is used for simulation purpose & model files are for a Wrap-All Around gate CNTFET device.

VII. INVERTER USING CMOS & CNTFET

The figures of CMOS inverter Fig (g) & Inverter using CNTFET Fig (h1 & h2) are shown below.

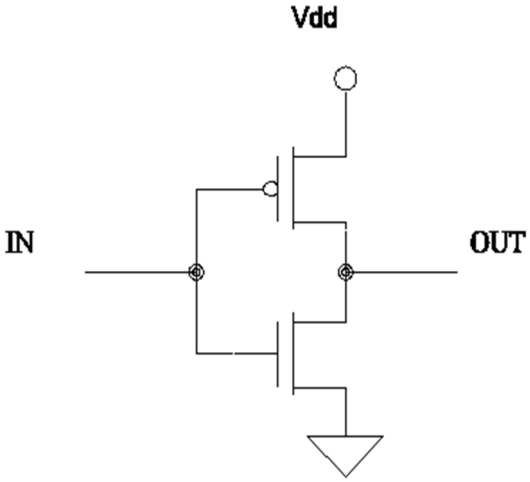

Fig (g) CMOS inverter

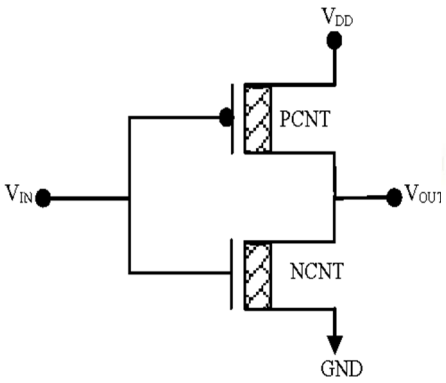

Fig (h1) CNTFET inverter

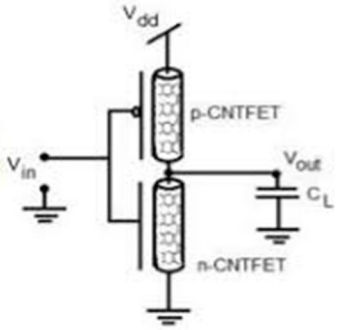

Fig (h2) CNTFET inverter

CMOS inverters are the most widely used inverters utilized in chip design. They operate with little power loss and at relatively high speed. The CMOS inverter has good logic buffer characteristics and its noise margins in both low and high states are large. A CMOS inverter contains a PMOS transistor and an NMOS transistor (See Fig g). It is important to note that the CMOS doesn't contain any resistors, which makes it more power efficient that a normal resistor-MOSFET inverter. As the input voltage of the CMOS device varies between 0 to VDD, the operation of the NMOS and PMOS varies accordingly. If we model each transistor as an easy switch activated by VIN, the inverter's operations are often seen very easily: The CMOS inverter provides fast switching operation with less delay time, high buffer margins, and less power dissipation. These are important features of any circuit (in this case inverter) in VLSI design. Fig h1 & h2 shows Inverter using CNTFETs. Its performance in terms of average power dissipation and speed (less time delay) is better than CMOS inverter. The table given below proves it.

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VIII. RESULT: GRAPHS AND TABLES

Name of circuit: Comparison of Inverter using CNTFET and Inverters using different CMOS models

MODELS	Total Power dissipation (watts)	Leakage power dissipation (watts)	Average Power dissipation	Time delay (sec)	PDP(J)
CNTFET	3.094e-08	1.547e-16	3.647e-08	1.187e-12	4.329e-20
IBM	1.235e-05	6.175e-14	1.698e-05	6.493e-11	11.025e-16
TSMC	5.603e-07	2.802e-15	3.027e-06	1.104e-11	3.342e-17
PTM	1.992e-05	9.959e-14	3.688e-05	1.516e-11	5.591e-16

Table no.1

A. CNTFET Inverter

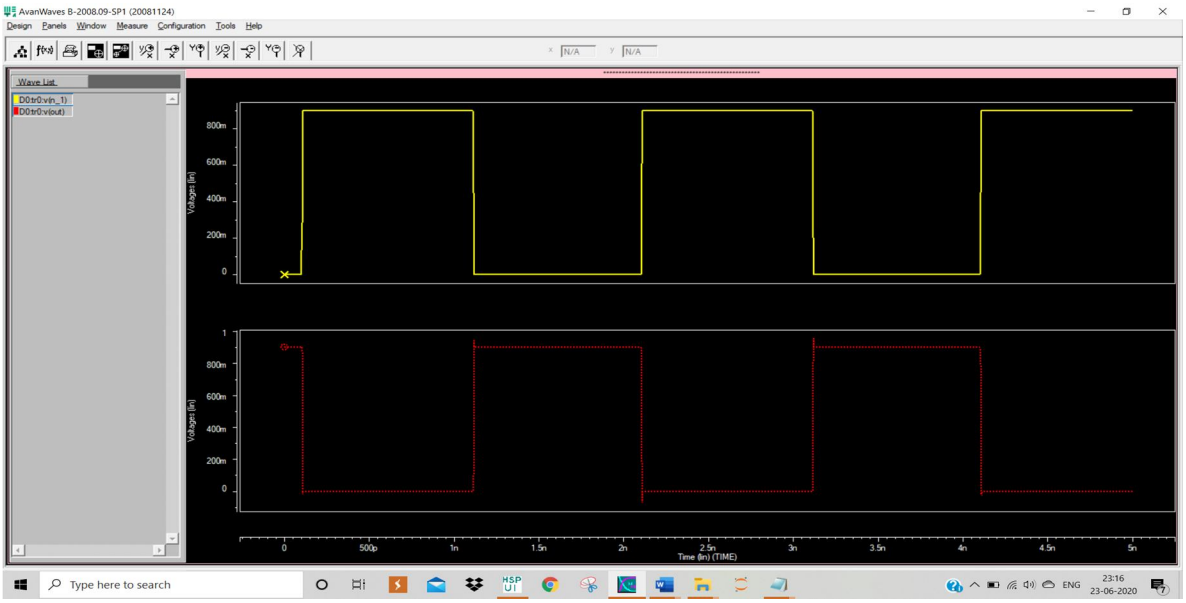


Fig (i) Simulations results Inverter logic of CNTFET Inverter

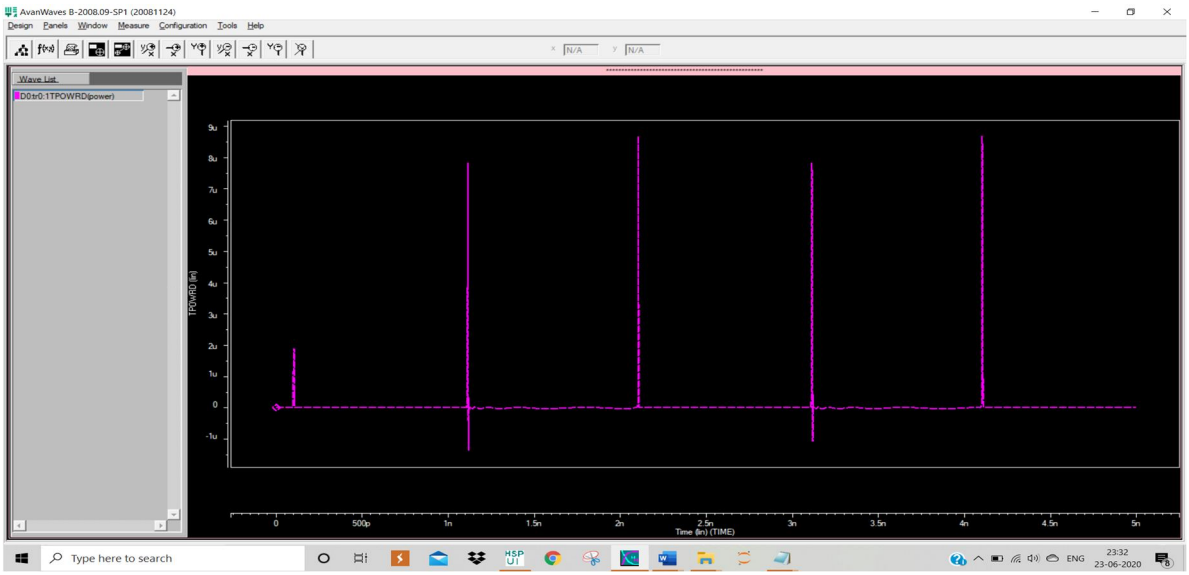


Fig (j) Simulations result of switching power dissipation of CNTFET Inverter

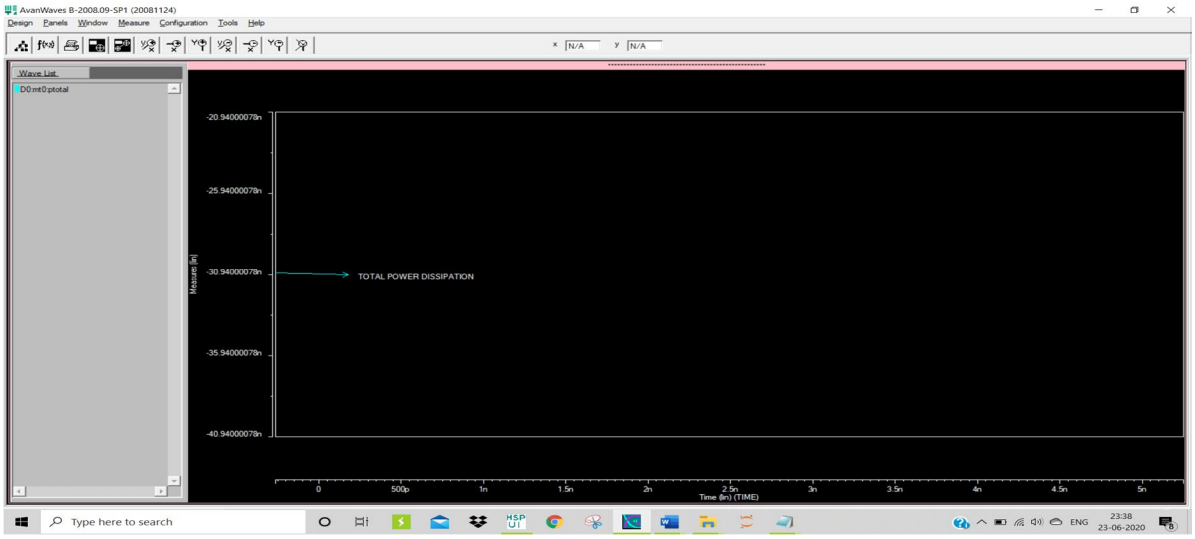


Fig (k) Simulations result of total power dissipation of CNTFET Inverter

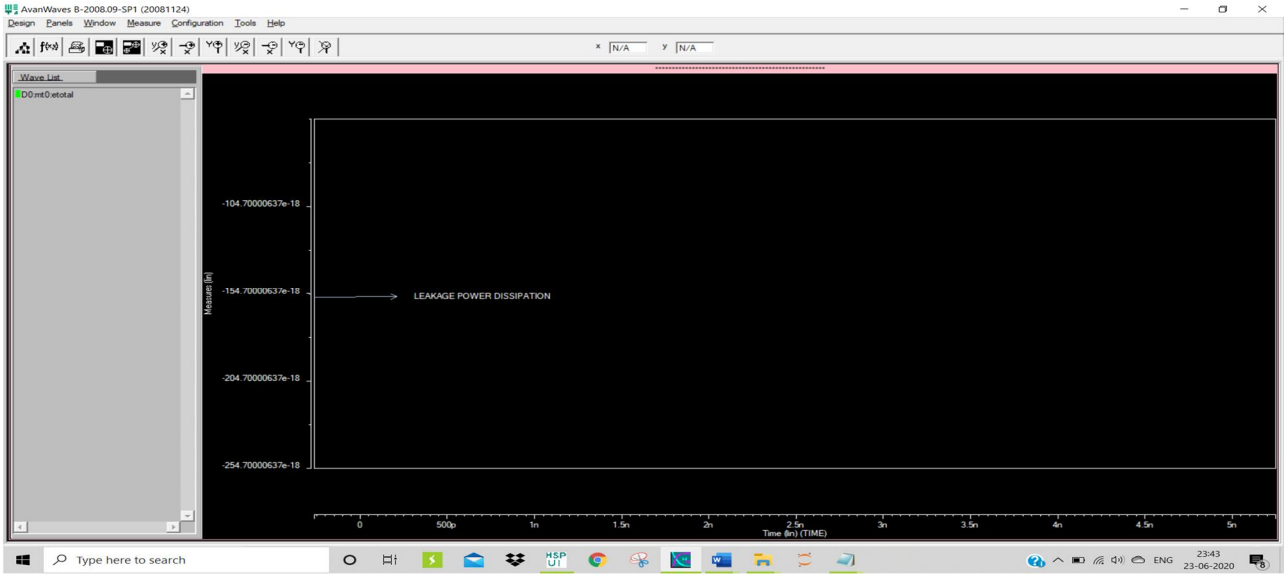


Fig (l) Simulations result of leakage power dissipation of CNTFET Inverter

B. Inverter 22nm PTM Model

Fig (m) Simulations results Inverter logic of CMOS PTM model Inverter

C. Inverter TSMC Model

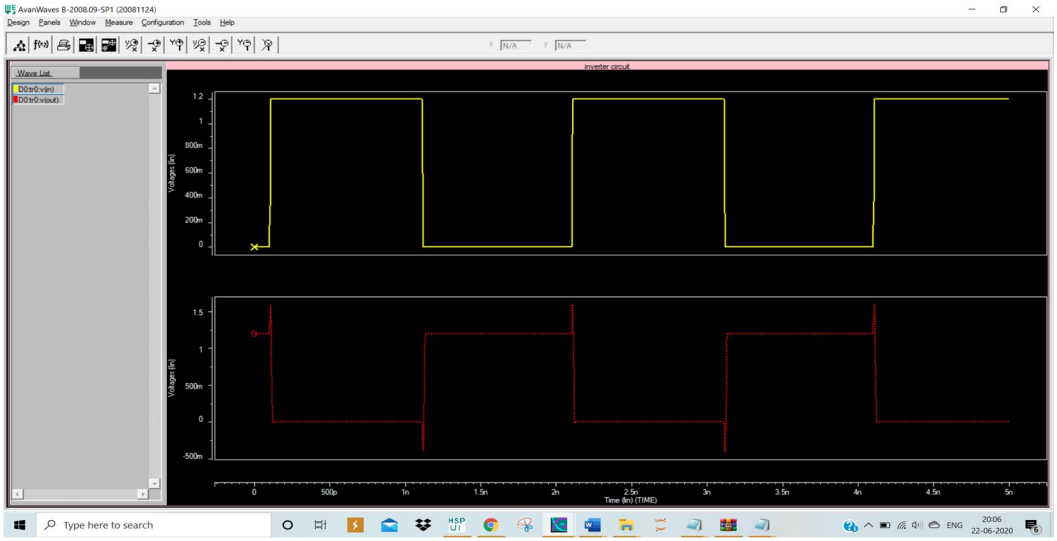


Fig (n) Simulations results Inverter logic of CMOS TSMC model Inverter

D. Inverter IBM Model

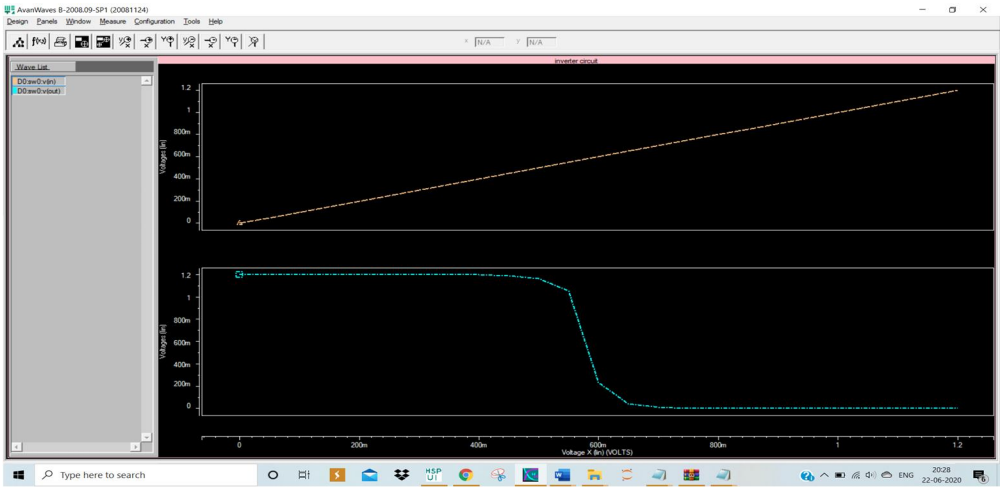


Fig (o) Simulations results Inverter logic of CMOS IBM model Inverter

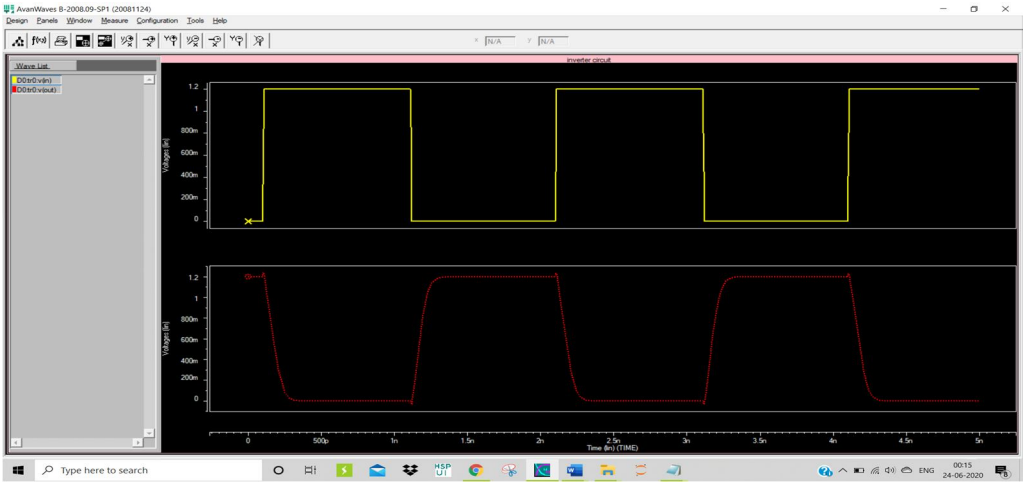


Fig (p) Simulations results Inverter logic of CMOS IBM model Inverter

IX. KEY ADVANTAGES

A. Electron mobility is high
B. Current density is high
C. Transconductance is high
D. Better control over channel formation
E. Better subthreshold slope
F. Better threshold voltage

X. APPLICATION

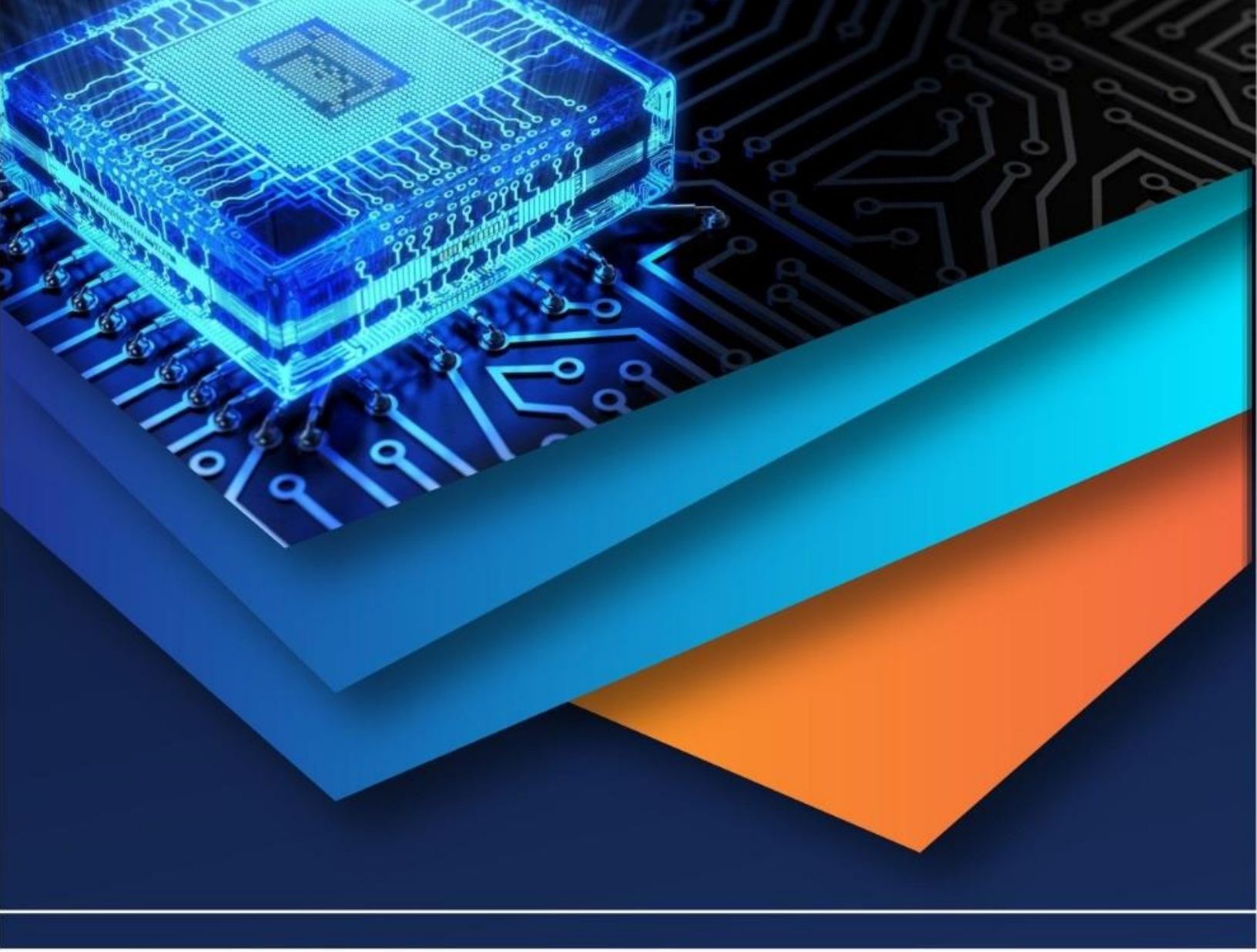
A. High mobility for near-ballistic transport
B. High carrier velocity for fast switching
C. Better electrostatic control due to the quasi one-dimensional structure of CNTs
D. High-speed transistors
E. Optoelectronics devices
F. Biosensors

XI. CONCLUSIONS

From the above simulated waveforms & table we observe that by using CNTFETs in VLSI circuits power dissipation can be reduced and speed can be improved. Using CNTFETs total power dissipation & time delay are least compared to other CMOS models. As shown in the last column of table no.1 after comparison of CNTFET with other CMOS models the figure of merit of CNTFET is better than all CMOS models. Thus, CNTFETs are used to upgrade the performance of VLSI circuits.

REFERENCES

[1] Hong Li, Chuan Xu, Navin Srivastava, and Kaustav Banerjee, “Carbon Nanomaterials for Next-Generation Interconnects and Passives: Physics, Status, and Prospects”, IEEE Trans. Electron Devices, vol. 56, no. 9, Sep, 2009.
[2] Ali Javey, Jing Guo, Qian Wang, Mark Lundstrom, and Hongjie Dai, “Ballistic carbon nanotube field-effect transistor,” Nature, vol. 424, pp. 654-657, 2003.
[3] S. Das, S. Bhattacharya and D. Das, “Modelsing of carbon nanotube-based device and interconnect using VERILOG-AMS”, Proc. Int. Conf. on Advances in Recent Technologies in Communication and Computing, pp. 51-55, Sep. 2011.
[4] Busi, R., Swapna, P., Babu, K., Srinivasa, R., "Carbon Nanotubes Field Effect Transistors: A Review", International Journal of Electronics & Communication Technology, Vol.2, SP-1, Dec.2011, pp. 204-208.
[5] Andrew, D., Ervin, M. "Effects of Differing Carbon Nanotube Field-effect Transistor Architectures", Army Research Laboratory, July 2009.
[6] Chen, Zhihong; Farmer, Damon; Xu, Sheng; Gordon, Roy; Avouris, Phaedon; Appenzeller, Joerg (2008). "Externally Assembled Gate-All-Around Carbon Nanotube Field-Effect Transistor". IEEE Electron Device Letters 29(2)183.
[7] Javey, Ali; Guo, Jing; Wang, Qian; Lundstrom, Mark; Dai, Hongjie (2003)."Ballistic carbon nanotube field-effect transistors". Nature 424 (6949): 654-7.
[8] S.Rasmita et al, "Simulation of Carbon Nanotube Field Effect Transistors," International Journal of Electronic Engineering Research, 117–125 Vol.1, No.2 (2009)
[9] Jing Guo; Datta, S.; Lundstrom, M.; Brink, M.; McEuen, P.; Javey, A.; Hongjie Dai; Hyoungsub Kim; McIntyre, P. (2002). "Digest. International Electron Devices Meeting". p. 711
[10] Digital Design Textbook by M.Morris Mano-Applied Electronics Engineering
[11] J. Guo, A. Javey, H. Dai, and M. Lundstrom, “Performance analysis and design optimization of near ballistic carbon nanotube FETs,” IEDM Tech. Digest, pp. 703-706, 2004.
[12] R. Saito, G. Dresselhaus, and M. S. Dresselhaus, “Physical Properties of Carbon Nanotubes.” London: Imperial College Press, 1998.



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