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Design of Low-Power Reconfigurable LNA for Multi-Standard Receiver

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Abstract: ***In this paper a low-noise-amplifier is presented which is operating for multi-standard wireless application which includes GSM (DCS1800) 3G (UMTS) band applications. By employing forward-body-biasing technique along with current-reuse technique our proposed design is working at very low bias voltage while maintaining high gain. The LNA shows an excellent standard of gain with low dissipation of DC power and minimal noise figure. Low noise figure and high gain is achieved by employing positive feedback in transformer coupled source follower configuration. 0.18 µm CMOS process is used to design proposed LNA. The simulated result shows that re-configurability of LNA is from 1.86 GHz to 2.1 GHz. It achieves a power-gain of 14.46 dB to 4.43 dB at 1.86 GHz and from 24.68 dB to 7.49 dB at 2.10 GHz, minimum noise figure of 2.14 dB, DC power dissipation of 1.43 mW and maximum IIP3 of -6.27 dBm.***

Index Terms: ***Common Gate (CG), positive feedback, Low Noise Amplifier (LNA), reconfigurable, third intercept point (IIP_3), noise figure (NF), multi-standard.***

I. INTRODUCTION

In the last few decades there is huge advancement can be seen in the field of wireless communication, With the ongoing headways in wireless communication and IoT new standards of communications have developed to meet various prerequisites. To increase the battery life of gadget we need a transmitters and receivers having low dissipation of DC power. LNA is one of the most integral parts of a receiver. For the minimization of power dissipation we are using some techniques like forward body-bias [1]-[2] and current reuse [1]-[3], and for the purpose of gain enhancement we are using gain-boosting technique [1], [2], [4]. For improvisation of stability and NF of our proposed LNA without effecting the input/output matching we employed dual-feedback technique [5], [6]. As we know that some years back we employ parallel structure to design the LNA for multi-band, multi-standard applications but this approach has some disadvantages which are high power dissipation and can consume more chip area, so this lead to the formation of idea of a reconfigurable LNA. The various techniques used to design reconfigurable LNA is depicted in [1], [5]-[14]. Here a LNA having the power dissipation very low i.e. in the range of few mW is accounted.

The paper is organised in following manner: Steps followed to design of the proposed reconfigurable LNA for multiband applications is under the Section II, Results of simulation is illustrated in Section III, and the conclusion are drawn in Section IV.

II. CIRCUIT DESCRIPTION

In the proposed LNA we are using Common Gate (CG) amplifier configuration because it has various advantages over the common-source (CS), and these advantages are elite input/output matching, better stability, good noise performance i.e. very low NF [1], [6]. One disadvantage of this configuration is low gain and this is overcome using gain-boosting technique [10]. Here we opted the passive devices over active devices because by using the transformer feedback the overall gain performance of circuit is improvised while the active devices adversely effects the noise factor and stability, the proposed LNA is shown in figure 1 and the device value are given in Table I. To minimize the power dissipation in our proposed design we are employing current-reuse and forward body biasing techniques [1]-[2]. The proposed LNA is operating at the 0.65 V DC voltage supply.

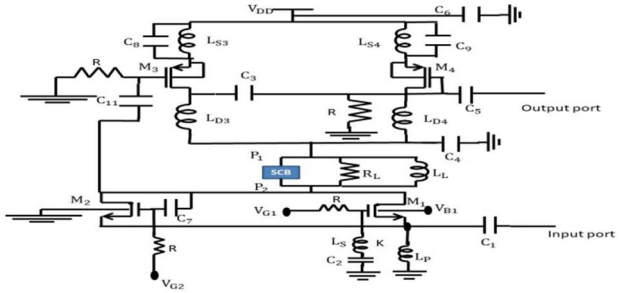

Figure 1: Schematic of the proposed low power Reconfigurable LNA

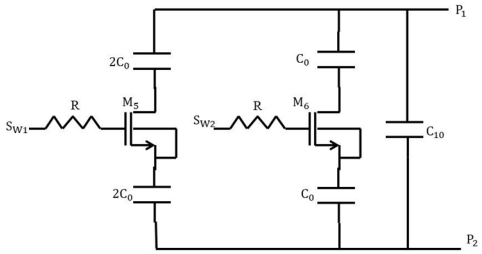

Figure 2: Switched Capacitor Bank (SCB) for proposed LNA where control signal are denoted by S_{W1} and S_{W2} which are used for tuning.

As we are employing forward-body-bias in gm-boosted CG input stage the gain is improvised while the power dissipation of the circuit is minimized. The V_{th} of input transistor M_1 is varied by varying the V_{bs}. Here we are applying positive V_{bs} so the threshold voltage of input transistor M_1 is reduced [3], [4].

To achieve reconfigurability we are using the combination of Switched Capacitor Bank (SCB) along with the common drain configuration with the positive feedback. Here reconfigurability is achieved. Here the resonant load is resonating over two frequencies. For using the current reuse technique C_4 is used which is working as a bypass capacitor with inductances L_{D3}, L_{D4} combined with tank load of M_1. The input transistor M_1 with transformers L_S and L_P is having K=0.7 coefficient of coupling for achieving low noise performance and better gain. Gain boosting technique is employed to enhance the gain obtained by first stag. Degeneration is used in every stage for the minimization of noise, input/output impedance matching and gain improvement. There is a connection between the output terminal of the CG first stage is connected to the source of the input of transistor M_1 through a source follower formed by MOSFET M_4 creating a positive feedback. As shown if fig. tank network is formed by resistor R_L and switched-capacitor-bank i.e. SCB is act as load of input transistor M_1 as represented in figure 2. Re-configurability in gain can be seen by changing the control signal of MOSFET's M_5, M_6. Due to employing positive feedback the input impedance is increased. In figure 1 load has been tuned. There is matching between the load of input transistor and source resistance. The circuit is resonating at the different resonance frequencies i.e. peak can be seen in different frequencies. Hence, dual feedback technique with forward-body-bias in CG first stage is used to achieve dual-band operation with significant gain tuning with low power dissipation and enhanced linearity for GSM bands namely (DCS1800) and 3G (UMTS) band. We have of connect a band pass filter at the input of proposed LNA.

Table I
Device Parameter Values of Proposed Reconfigurable LNA

Devices	Values	Device	Values
C_1	4.3 pF	C_{11}	2 pF
C_2	15 pF	M_1	300 µm/0.18 µm
C_3	16 pF	M_2	50 µm/0.18 µm
C_4	24 pF	M_3/M_4	322 µm/0.18 µm
C_5	230 fF	L_{S3}/L_{S4}	0.4 nH/0.4 nH
C_6	4.92 pF	L_P/L_S	6 nH/5 nH
C_7	4 pF	L_{D3}/L_{D4}	5.51 nH/5.51 nH
C_8	1 pF	L_L	4 nH
C_9	1 pF	R	10 K
C_{10}	0.35 pF	R_L	20 K

III. SIMULATION RESULTS

The proposed design of LNA shown in figure 1 is based on 0.18 µm CMOS process and is simulated using Keysight Advanced Design System (ADS) software tool. The proposed design is working on 0.65 V DC supply. The 0.1 DC voltage supply is used for biasing body of transistor M_1. The power dissipation of our proposed design is having 1.43 mW which is lower than the other reported reconfigure LNAs. Simulation results are depicted in figure 3, figure 4, figure 5 in form of power gain, input return loss and NF. The re-configurability in gain can be seen by varying the control signal given to the MOSFETs M_5 and M_6 of load added on the input transistor M_1. As seen in figure 3, the re-configurability in gain has been achieved from 14.46 dB to 4.43 dB at 1.86 GHz when we alter the control signal 00_2 to 11_2 of Switched Capacitor Bank, and the gain is varying from 24.68 dB to 7.49 dB at 2.10 GHz for the same pattern of control signals. The input return loss is always below the -4.27 dB for all combination of control bits.

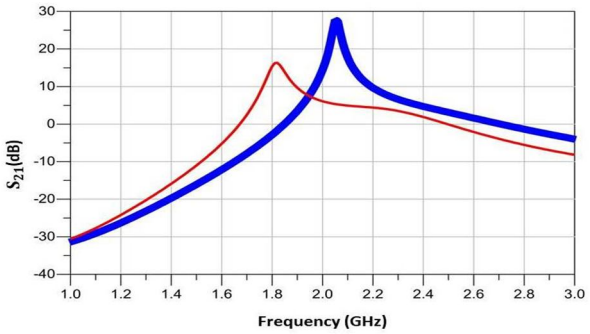

Figure 3: Power Gain : red colour graph is for when both M_5 and M_6 are OFF and blue is for when both M_5 & M_6 are ON, it varies from 14.46 dB to 4.43 dB at 1.86 GHz and from 24.68 dB to 7.49 dB at 2.10 GHz.

The NF of the proposed LNA is depicted in figure 6 and it is varying from 2.14 dB to 2.26 dB for 1.86 GHz and from 2.29 dB to 2.56 dB at 2.10 GHz for the applied control signals ranging from 11_2 to 00_2.

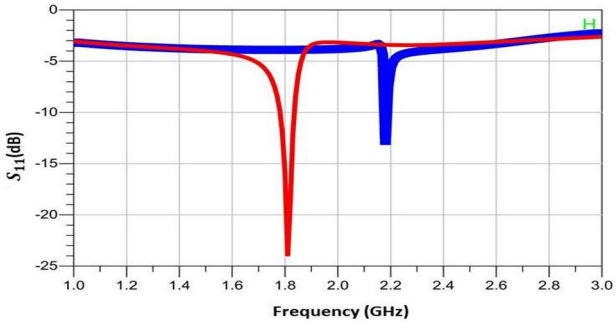

Figure 4: Input return loss (S_{11}): red colour graph is for when both M_5 and M_6 are OFF and blue is for when both M_5 & M_6 are ON $_2$ it varies from -18.61 dB to -4.63 dB at 1.86 GHz and from -9.68 dB to -4.27 dB at 2.10 GHz

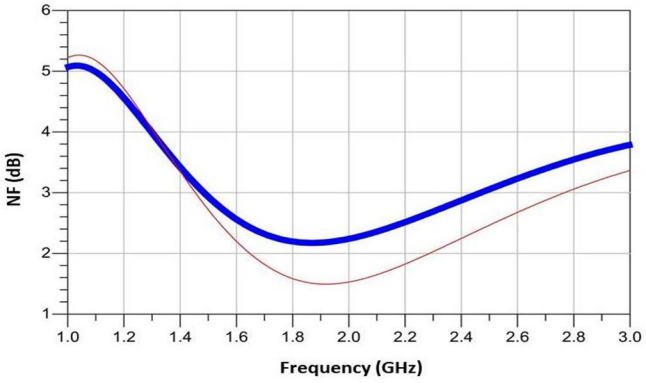

Figure 5: Simulated NF: from fig. it is seen that red colour graph is for when both M_5 and M_6 are OFF and blue is for when both M_5 & M_6 are ON, it varies from 2.14 dB to 2.26 dB for at 1.86 GHz and from 2.29 dB to 2.56 dB at 2.1 GHz.

The proposed circuit is having very low dissipation of power which is 1.43 mW and it can be further minimized by minimizing the parasitic capacitances. The IIP_3 of the proposed circuit is -8.46 dBm and having P_{1dB} of -23.18 dBm at 1.86 GHz. While it has IIP_3 of -6.27 dBm and compression point (P_{1dB}) is -19.76 dBm at 2.10 GHz. The simulation result shows the good noise performance along with the high gain and low dissipation of power. In Table II there is comparison between the performances of various reported LNAs with our proposed LNA.

IV. CONCLUSION

The proposed Reconfigurable LNA design is based on 0.18 µm CMOS process. This LNA operates over multi-band and is working at low input supply voltage. Forward–body-bias and current reuse techniques are used to minimize the power dissipation and for the maximization of gain we are employing the gain boosting technique. The results of simulation shows that our proposed LNA is working at 0.65 V DC supply and is showing the reconfigurability in the frequency range of 1.86 GHz to 2.10 GHz. It has a maximum IIP_3 of -6.27 dBm and it's able to achieve a power-gain of 14.46 dB to 4.43 dB at 1.86 GHz and from 24.68 dB to 7.49 dB at 2.10 GHz. It has minimum NF of 2.14 dB and having power dissipation of 1.43 mW. So it is clear that our proposed LNA is easily reconfigurable and have very low power dissipation among all the reported LNAs.

Table II
Comparison of Performance with other Reported LNAs

References	[3]	[5]	[16]	[17]	This Work
CMOS Technology (nm)	180	180	180	180	180
Frequency (GHz)	1.86 2.4	1.83 2.47	1.9 2.1 2.4	2.5 WB 1.8 NB 2.1 NB 2.4 NB 1.9DB 5.2 DB	1.86 2.10
Gain (dB)	9.68- 6.87 10.17 -3.96	15 17.4	21 22 23.5	14.8 WB 11.6 NB 12.8 NB 13.5 NB 18 DB 18 DB	14.46-4.43 24.68-7.49
NF (dB)	5.34 3.77	1.63 2.02	2.45 2.45 2.7	5.8 WB 8.5 NB 8 NB 8.5 NB 5.5 DB 7.8 DB	2.14-2.26 2.29-2.56
BW (GHz)	0.46	-	-	-	0.45
Supply (V)	0.63	0.63	1.8	1.8	0.65
P_{DC} (mW)	1.61	18.9	10.9	3.84 WB 1.8 NB 3.84 DB	1.43

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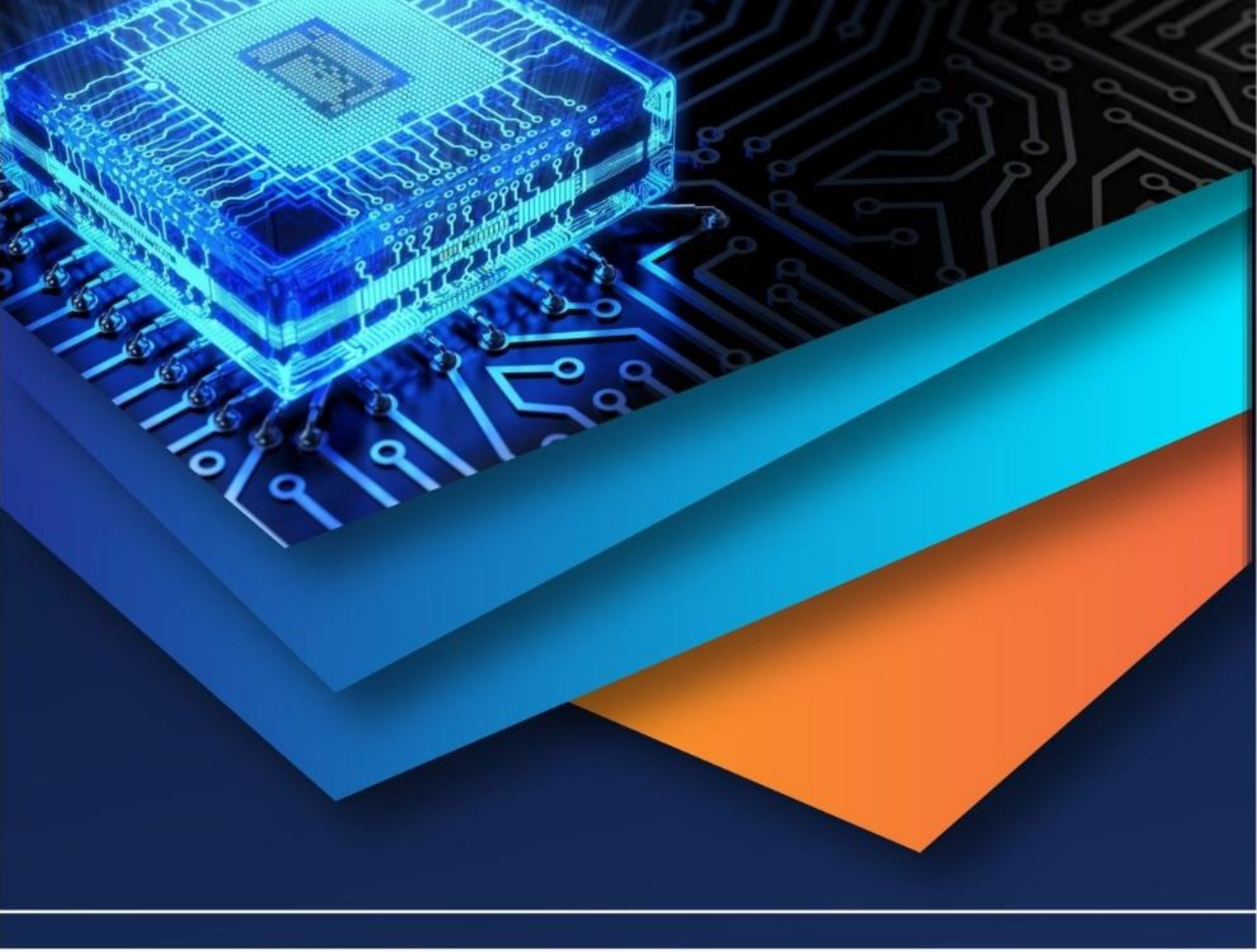

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