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An Implementation of Nine Level Cascaded H-Bridge Inverter Using Switched Capacitor

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Abstract—The enhancement of transmission frequency deserves more than the low or medium frequency applications. High frequency is mostly preferred now-a-days because of to reduce the size and cost of the power electronic equipments. Actually high frequency inverter (HF) should be present on the source side to achieve more frequency, but it is very complicate with the simple circuit. So, in this paper switched capacitor based on the multilevel inverter is preferred. Switched capacitor occupies on the front end and the h-bridge occupies on the back end. By changing the series and parallel connections of the network the levels of the voltage gets increases. As well as the voltage levels increases the harmonics is also reduced.
Keywords—High frequency ac (HFAC), cascaded multilevel inverter, switched capacitor (SC), Power distribution system (PDS).

I. INTRODUCTION

Today the power electronic converters are the most useful elements for the transformation of electrical energy and the connection between the renewable dc sources to the grids. High frequency ac power distribution system (HFAC PDS) was primitively proposed by the national aeronautics and space administration (NASA) for space power applications since the conversion of power stages are less and the number of components are reduced. Recently it has pulled more interest among the both academia and from the industry. The high frequency ac (HFAC) is the option for the traditional dc distribution system. The applications are present in electric vehicle, telecom, computer, renewable micro grid. HFAC PDS is to challenge of these activities such as high power capacity, high electromagnetic interference (EMI) and more power losses. To increase the capacity of power the output of the inverter is to be connected either in series or parallel. Since it is impractical for the HF inverter, it is difficult to synchronize both amplitude and phase with high frequency. So multilevel inverter is the best solution to increase the capacity of power without synchronization and by this high capacity of power is obtained by multilevel inverter with low switching stress. Non polluted sinusoidal waveform with less total harmonic distortion (THD) is severely caused by long distribution track in HFAC PDS. By increasing the number of voltage levels the content of harmonics of stair case output gradually gets decreases. The topologies of multilevel inverter are diode clamped, capacitor clamped, cascaded h-bridge. Firstly the diodes are used to clamp the voltage level and next the capacitors are used to clamp the voltage level and the levels get increases as well as the circuit complexity increases in these two topologies. By the series connection the cascaded structure greatly increases the reliability of the system.

II. SC BASED CASCADED INVERTER FOR NINE LEVEL

The front end of the circuit occupies the switched capacitor and the back end occupies the cascaded h-bridge. Count of voltage levels achieved by sc front end and back end are N_1 and N_2 respectively. The number of voltage levels is $2*N_1*N_2+1$ for the entire cycle operation..

A. Circuit Topology

The circuit topology of nine level inverter consists of the switches S_1, S_2, S_1',and S_2' are the switching devices of switched capacitor circuits SC1, SC2 and these are used to convert the series and parallel connections of the capacitors C_1, C_2. The switches S_{1a}, S_{1b}, S_{1c}, S_{1d}, S_{2a}, S_{2b}, S_{2c}, and S_{2d} are the switching devices of h-bridge as shown in the figure 1.

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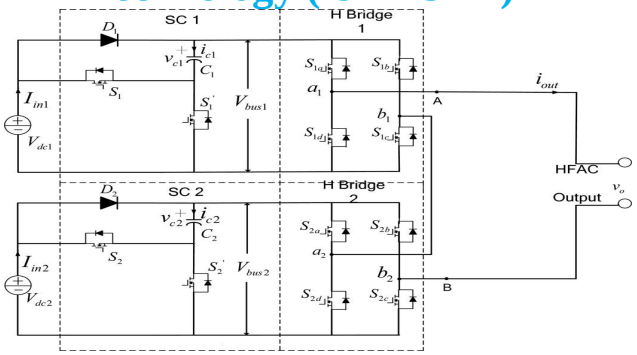

Figure 1 Circuit analysis of nine level inverter

Vdc1 and Vdc2 are the input voltages. The diodes D_1 and D_2 are used to restrict the direction of current. I_{out} and V_o are the output current and output voltages respectively.

B. Generation of Pulses

By the table 1the generation of pulses can be calculated by the different number of switches when the switches are on & off. Here there are ten working states for nine voltage levels. When the operation enters a new state from the adjacent state, only one power switch changes between on and off.

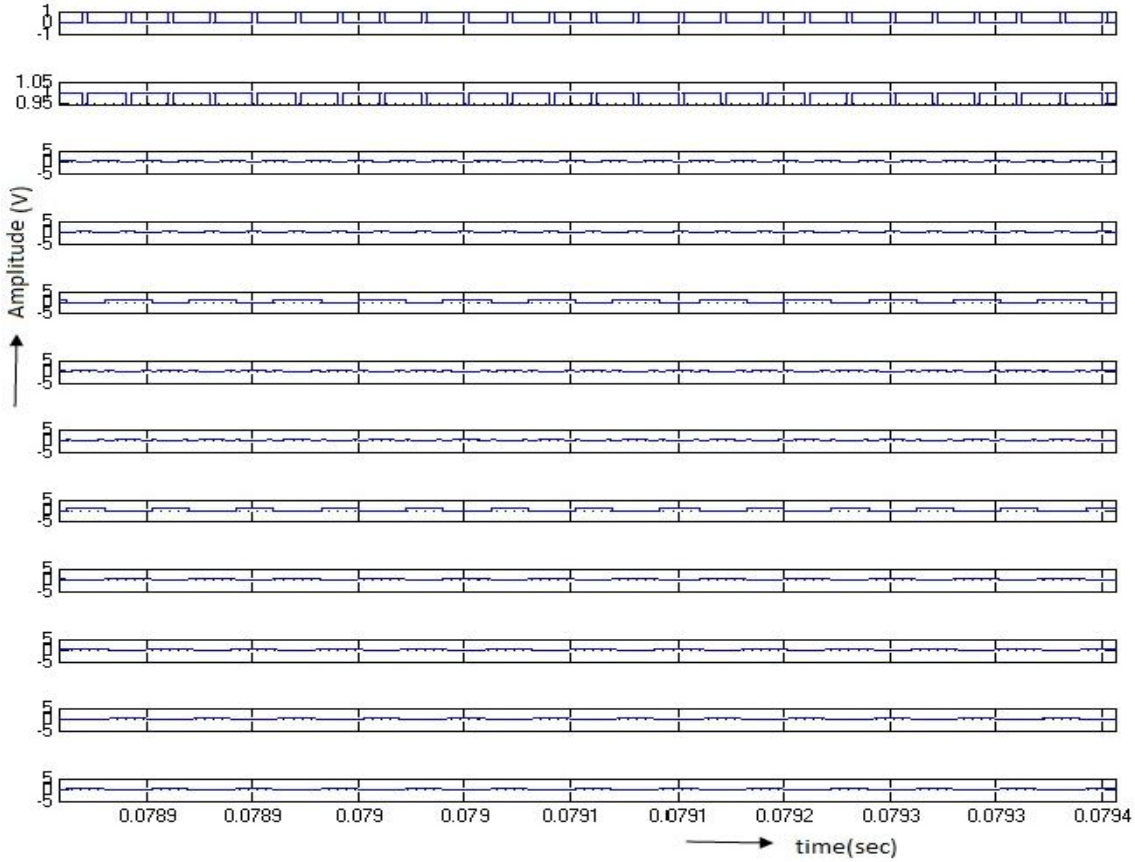

Figure 2 pulses for nine level inverter

III. MODES OF OPERATION

In this mode there are 8 stages of operation at different instants.

Volume 3 Issue VII, July 2015
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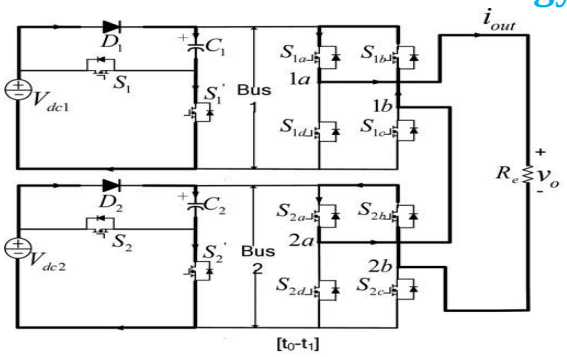

Figure 3(a)

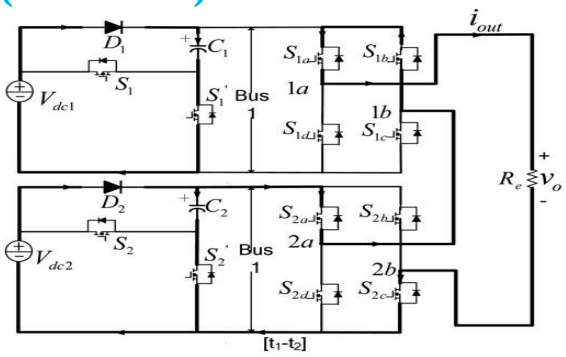

Figure 3(b)

In stage 1 at the instant when t satisfies $t_o \le t < t_1$ the switches S_{1a}, S_{1b}, S_{2a}, S_{2b} are in on position. H-bridges 1&2 are in freewheeling state and the output voltage equals to zero. The switches S_1', S_2' are on and the capacitors are charged to Vin and the voltages across the bus 1&2 are same as Vin as in figure 3(a).

In stage 2 at the instant when t satisfies $t_1 \le t < t_2$ the switches S_{1a}, S_{1b}, S_{2a}, S_{2c} are in on position. H-bridge 1 is in freewheeling state, 2 are in positive conducting state and output voltage equals to Vin. The switches S_1', S_2' are on and the capacitors C1, C2 charged to Vin and voltages across buses are same as Vin as in figure 3(b).

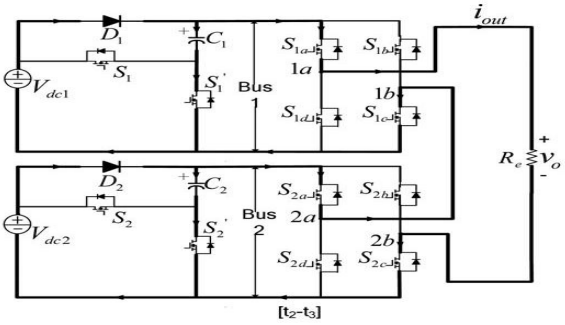

Figure 3(c)

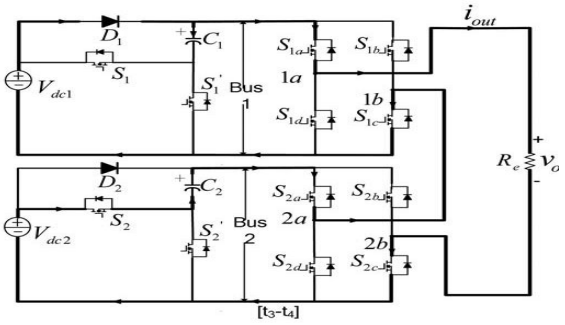

Figure 3(d)

In stage 3 at the instant when t satisfies $t_2 \le t < t_3$ the switches S_{1a}, S_{1c}, S_{2a}, S_{2c} are in on position. H-bridges are in positive conducting state and output voltage equals to 2Vin. The switches S_1', S_2' are on the capacitors keep charged to Vin and the voltages across the buses are Vin as shown in figure 3(c).

In stage 4 at the instant when t satisfies $t_3 \le t < t_4$ the switches S_{1a}, S_{1c}, S_{2a}, S_{2c} are in on position. H-bridges are in positive conducting state and the output voltage equals to 3Vin. The switches S_1', S_2 are on the capacitors C_1 charged to Vin and C_2 is discharged and the voltages across the bus 1 is Vin, bus 2 is 2Vin as shown in figure 3(d).

In stage 5 at the instant when t satisfies t4≤t<t5 the switches S1a, S1c, S2a, S2c are in on position. H-bridges are in positive conducting state and the output voltage equals to 4Vin. The switches S1, S2 are on the capacitors are discharged and the voltages across the buses are 2Vin as shown in figure 3(e).

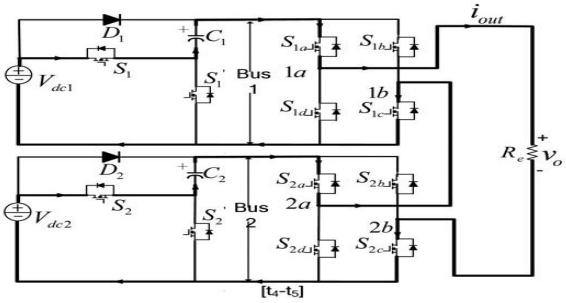

Figure 3(e)

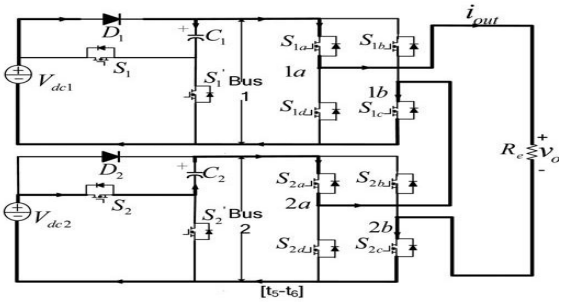

Figure 3(f)

At the instants $t_5 \le t < t_6$, $t_6 \le t < t_7$, and $t_7 \le t < t_8$ are same as the operations in $t_3 \le t < t_4$, $t_2 \le t < t_3$, $t_1 \le t < t_2$ respectively.

Volume 3 Issue VII, July 2015
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IV. SIMULATION MODEL AND RESULTS

The simulation is based on the MATLAB software for the proposed inverter and the model is shown below. The waveforms for nine level sc based cascaded inverter at low power is taken as Vin=12v, C_1=100µf, C_2=220µf, Ro=12Ω and at high power is taken as Vin=100v, C1=300µf, C2=560µf, Ro=12Ω.

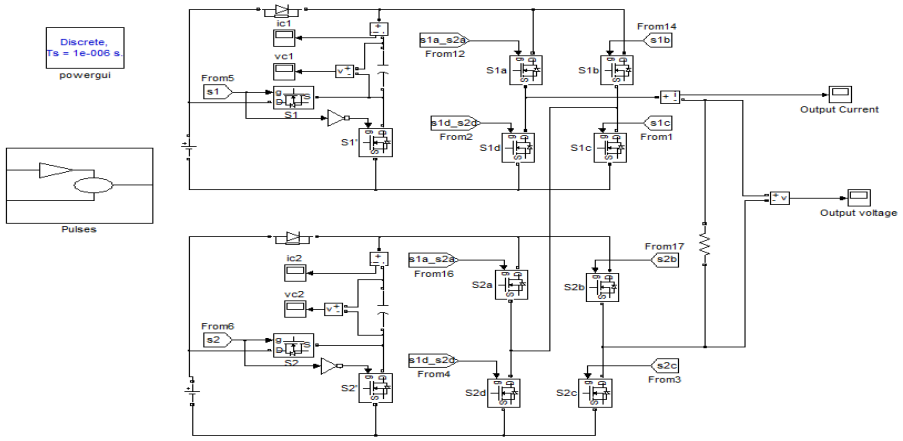

Figure 6 Simulation circuit for nine level SC based cascaded inverter

At low power at 50w

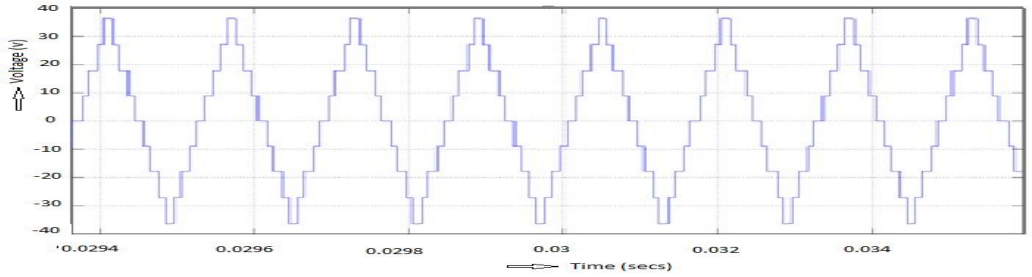

Figure7 Output voltages for sc based cascaded inverter

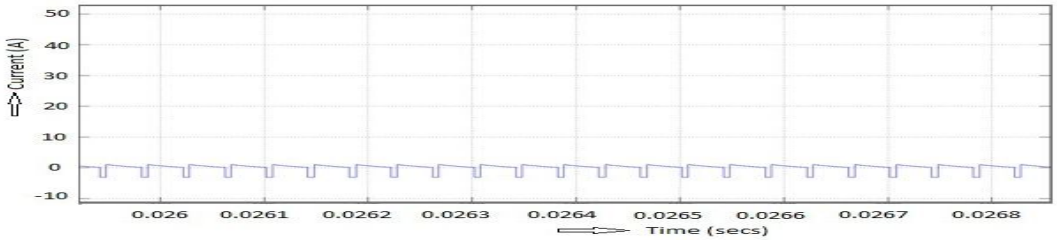

Figure 8 Current across the capacitor C_1

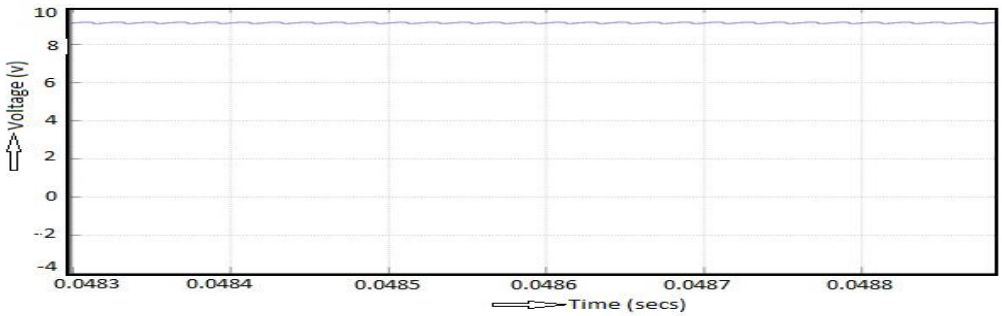

Figure 9 Voltage across capacitor C_1

Volume 3 Issue VII, July 2015
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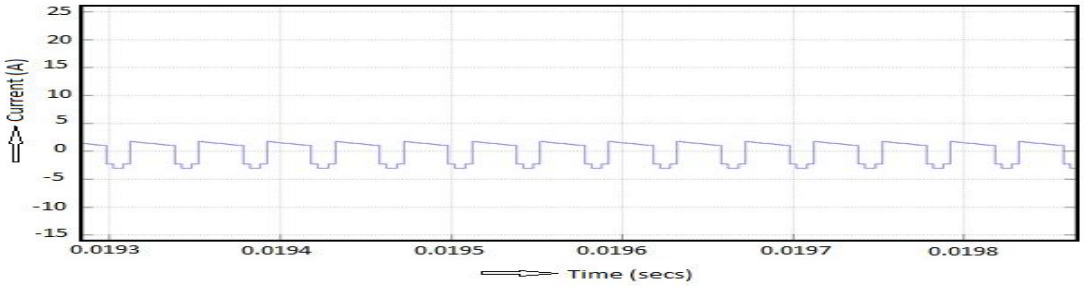

Figure 10 Current across capacitor C_2

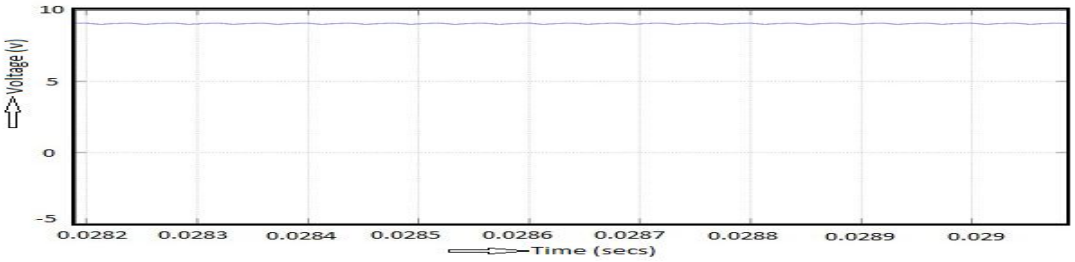

Figure 11 Voltage across capacitor C2

At high power at 100w

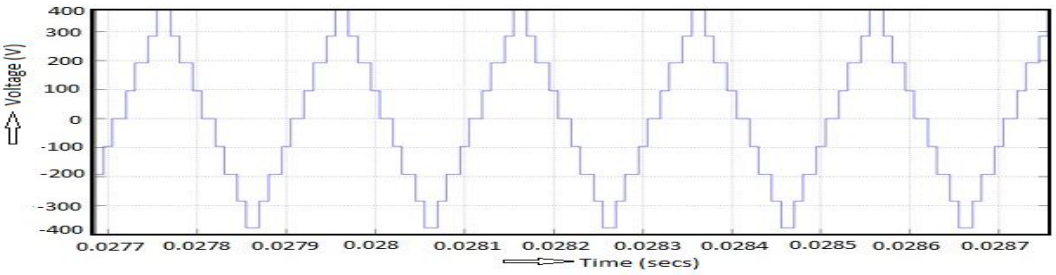

Figure 12 Output voltage for sc based cascaded inverter

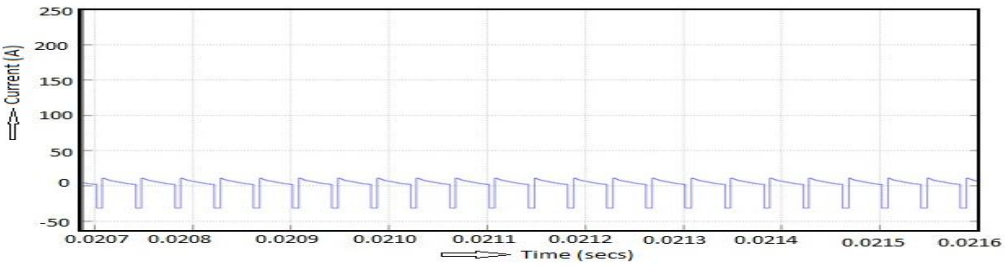

Figure 13 Current across the capacitor C_1

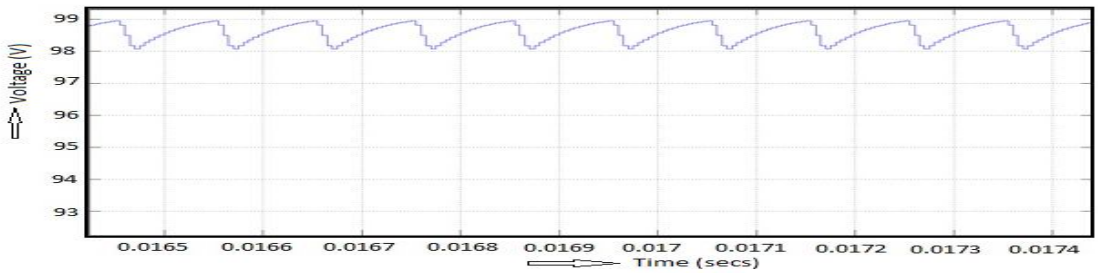

Figure 14 Voltage across capacitor C_1

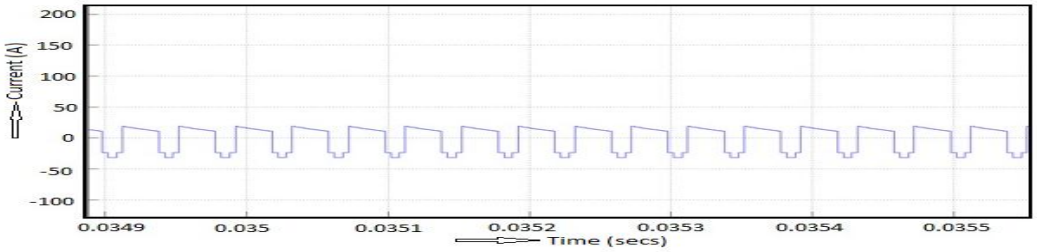

Figure 15 Current across the capacitor C_2

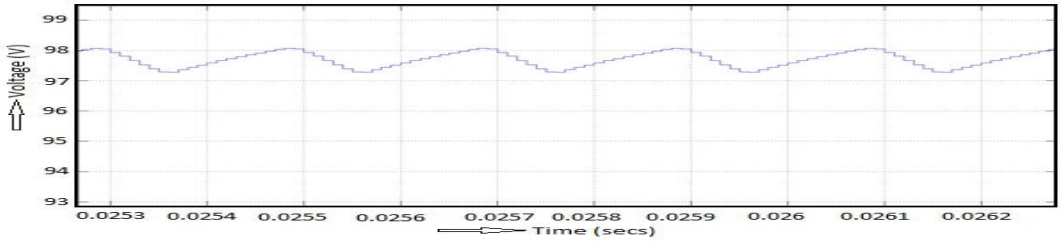

Figure 16 Voltage across the capacitor C_2

The total harmonic distortion for the conditions at low power is 18.46 and at the high power is 17.54

V. CONCLUSION

In this paper sc based cascaded inverter for nine levels is proposed in MATLAB/simulink. Here the proposed inverter can greatly decrease the number of switching cells. The voltage levels can be easily increases by the sc front end than the normal cascaded H-bridge. The proposed inverter can also be applied to electrical network of electric vehicle (EV) because multiple dc sources are available easily from solar panel, ultra capacitors, fuel cells and batteries.

VI. ACKNOWLEDGMENT

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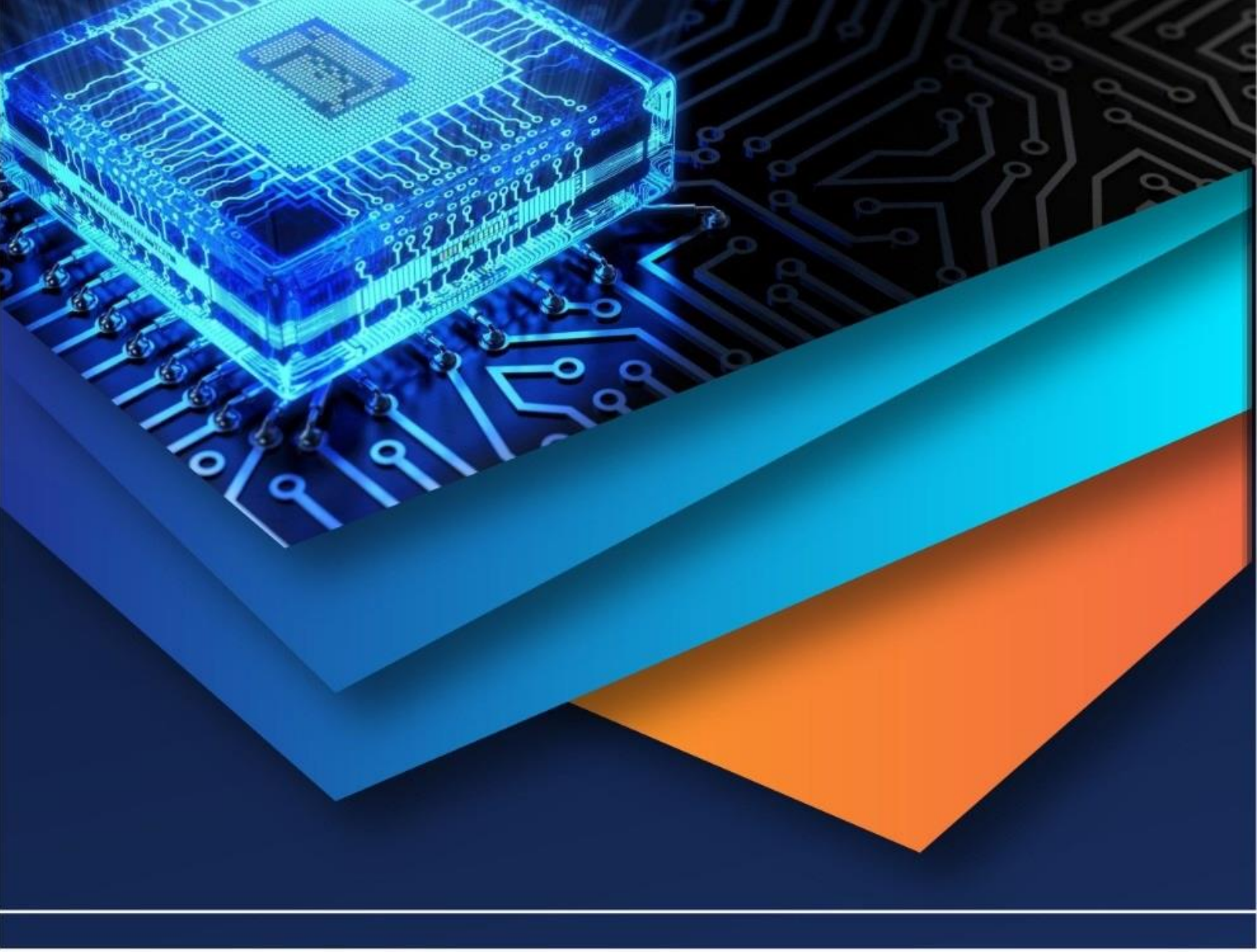

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