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A 8 Bit ALU Design using Cadence

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Abstract: ***In the era of growing technology and scaling of devices up to nanometer regime, the demand for optimization of area has come to the forefront .The design, schematic, and layout of an 8-bit Arithmetic Logic Unit (ALU) using cadence tool.With the advancement in technology area had become a major concern for the growing VLSI industry. Static CMOS logic does not fully meet the needs of future computing. Therefore improved digital logic techniques and styles which are energy efficient, fast and consume lesser area must be utilized. In this a area optimized 8-Bit Arithmetic Logic Unit having minimum circuit complexity is presented in an elegant way. The proposed ALU is designed using Cadence Virtuoso tool.The simulation results show that the proposed design requires less area and having a better performance by using minimum number of transistor.***
Keywords: ALU, Cadence virtuoso.

I. INTRODUCTION

Now a days there is a rapid increase in the utilization of portable applications which demands small-size, low power, high speed and high throughput circuitry. One of the most important parts of a digital processor is the arithmetic logic unit. ALU is designed to do the logic and arithmetic operations which are the processes that need to be done for almost any data that is being processed by central processing unit. And that's why the ALU is called heart of microprocessor, microcontroller and digital signal processor.As we known this arithmetic logic unit which is used to perform many logical operations and also arithmetic operation. Logical operation like AND, OR, XOR, NOT etc and also arithmetic operations like addition multiplication subtraction etc. In this arithmetic logic unit which take two operands and also which will perform the operation between that two operands.In this arithmetic logic unit which is having control signal which is used to select the output which is from the operation which are performed thus this control unit which is designed using the multiplexer which is helps in selecting required operation.For designing many electronic components need arithmetic function in which this addition operations helps in the determining speed and also which helps in reducing delay.This arithmetic logic unit which perform both arithmetic operation which will play major role in design of digital signal processor architecture and also which are used in the microprocessor and also which are used further in data processing. The arithmetic operations like addition subtraction division and multiplication are done by designing arithmetic logic unit and which are helps in designing microcontrollers. The adder circuit which are designed can be used in design many logical units which are helps in reducing the delay and also helps in increasing the speed of operation which are major components in the digital systems.Not only adders but also other components of the processor van be used to designing to table indication and also for calculation. And also we can design the other operatins like subtraction multiplication and also division. This addition function is the very common operation in electronics circuit designs. Just like microprocessor, digital signal processing & data processing application-specific integrated circuits.Here cadence virtuoso tool is used to perform simulation and results. Reduced in time and also reduction in consuming power in VLSI circuits. This reduce in time delay and area is directly depends on the number of transistors.

II. DESIGN OF ARITHMETIC LOGIC UNIT OPERATION:

A. NOT Operation

This NOT gate which is having single input in this if the given input is high that is 1 then it will return output as zero that is low or if input given to the not gate is low that is 0 then it will return the output as high that is 1.THE single bit not gate circuit is shown in Fig 1which is having input A and output Y. this not operator is the one of the basic operators used in alu in which the 8 bit NOT gate is shown in Fig 2 in which it is having 8 bit inputs A0 to A7 and out put Y0 to Y7 each not gate are connected to VDD and VSS.We know that the NOT gate which is nothing but negation that is which helps in express the condition in negetive.If condition is true, then the logical NOT operator which makes it false, and also vice versa. As with the other logical operator this not can gate can be used to create other expressions by combining it with the other logics. The NOT operator is used in most which support logical and comparison operators. It is used in construction of logical statements and in supporting bitwise negation. It is also an important component while setting up logic digital circuits and truth table of not operation shown in table 1.

Table 1: NOT gate truth table

INPUTS	OUTPUTS
A	Y
0	1
1	0

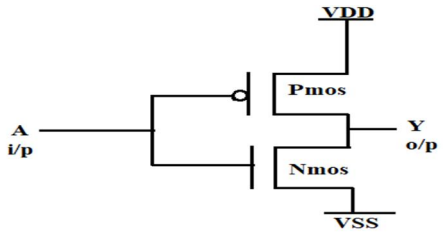


Fig 1: 1-Bit NOT circuit

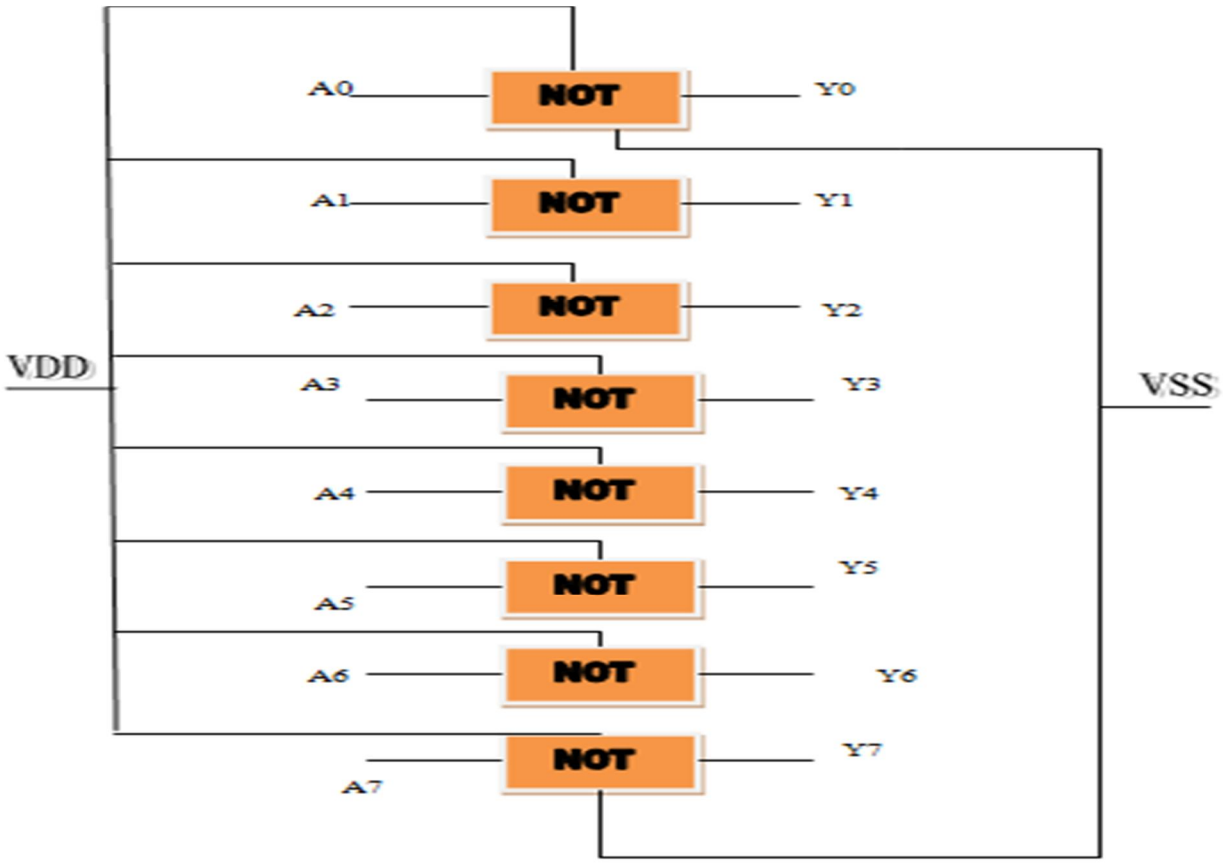


Fig 2:8-Bit NOT circuit diagram

B. XOR Circuit

Design of 3T XOR gate:

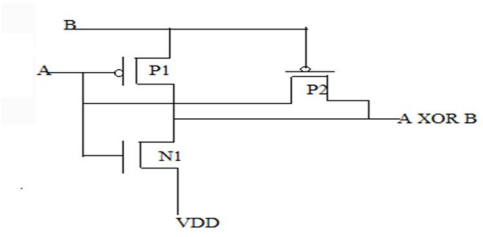


Fig 3: 3T XOR gate circuit

Table 2:Truth table of XOR gate

INPUT A	INPUT B	OUTPUT Y
0	0	0
0	1	1
1	0	1
1	1	0

3 transistor XOR gate is shown in Fig 3 and also XOR truth table is shown in table 2.3T XOR gate which is a combination of CMOS inverter & one pass transistor .This XOR which is having CMOS inverter and one pass transistor when input B=1the output become of XOR gate input A compliment.And another condition B=0 CMOS inverter output impedence go high. When the pass transistor is switched on and output is same as A input when B=0 and A=1 Both the transistor P2 & N1 trying to switched on because of the W/L ratio P2 threshold voltage is minimum comparative N1 that the reason P2 is conducted first & the output is same as the A input The minimize threshold voltage which will increases W/L ratio of transistor is relates by channel length & width.

$V_T = V_{TO} + \gamma(V_{SB} + \varphi_0) - \alpha_1 t_{ox}/L(V_{SB} + \varphi_0) - \alpha_V t_{ox}/L\ V_{ds} + \alpha_w t_{ox}/w\ (V_{SB} + \varphi_0)$.....(1)

V = zero bias threshold voltage

V_{TO} = threshold voltage of zero bias

γ = Threshold coefficient of bulk

φ_f= is fermi potential

t_{ox}= Oxide layer thickness

α_1 ,α_v and α_w = process dependent parameter

According to the equation 1 by increasing width can be reduce the threshold voltage. A problem is when A=1, B=0 in this condition 1 N transistor region the gate which is having high logic input 2 P transistor is also in active region its gate input voltage is logic low .This problem can be reduced by reducing the W/L ratio.The circuit diagram of 8 bit XOR is shown in the Fig 4 which is having 8 bit inputs A0 to A7, B0 to B7 and outputs Y0 to Y7 and supply VSS and grounded to VDD in which it perform the 8 bit XOR operation.

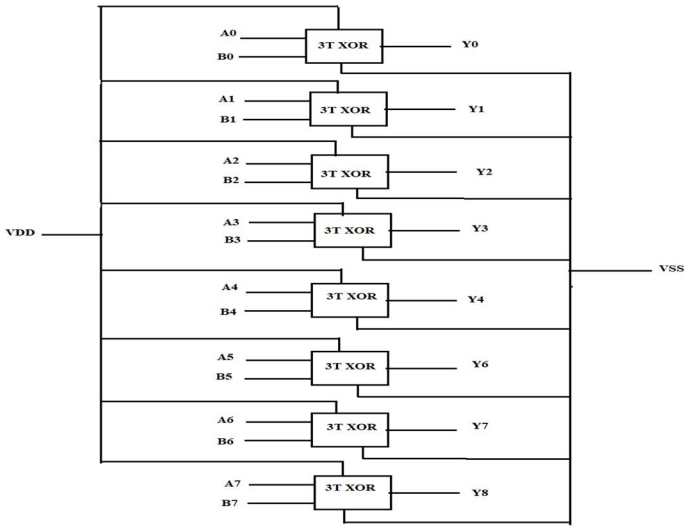


Fig 4: 8-Bit XOR gate Circuit

III. ADDER SUBTRACTOR CIRCUIT

In this adder subtractor circuit the full adder is designed by using 1 MUX and also 2 XOR gate in which xor is constructed by using pass transistor logic and mux is designed by using 2 transistor only. XOR is explained in 2 and MUX is explained below.

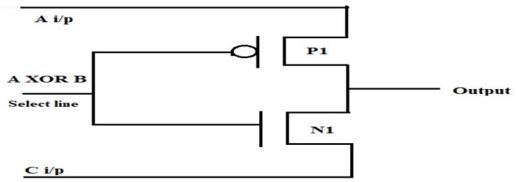
A. Design Of 2×1 Mux

Let us explain 2 input lines having signals as I_0 and I_1 for selecting one of the 2 inputs signals.We require addresses which can be a one bit word the address line are designated as a S_1.

Table 3: Truth Table for 2×1 Multiplexer

S1	Output
0	I_0
1	I_1

Fig 5: 2×1 multiplexer



This truth table can be expressed by the following Boolean expression.

Output=~S_1 I_0 + S_1 I.....(3)

Multiplexer circuit also works as select line A ⊕ B when A ⊕ B =0 the PMOS transistor is activated and its pass A input voltage at output terminal.when A ⊕ B = 1 NMOS was is activated is transfer the C input voltage at the output. NMOS W/L ratio is 1/1 and PMOS W/L ratio 2/1 [1]. MUX output is satisfied full adder carry output. 2×1 Multiplexer shown in Fig 5.

B. Design & Implementation Of Full Adder Circuit

This present approach as shown in symbolic circuit diagram of Fig 6 In this transmission gate and two XOR cells used along with mux.For design the full adder circuit in which carry is generated by mux and sum is generated by two xor gates.

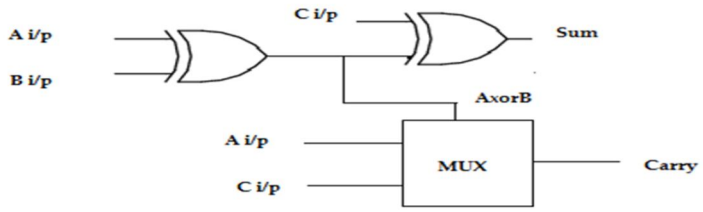


Fig 6: Full adder circuit diagram

In this single bit full adder circuit is having one multiplex gate and two XOR gates. A and B which are connected to the first XOR gate. C input to the second XOR gate .A⊕ B is select line for MUX, if A⊕ B=0 PMOS transistor is selected. A⊕ B=1 NMOS transistor is selected. Source terminal of PMOS is connected to A input voltage, NMOS source terminal is connected to C input voltage[1]. This design is based on a modified version of a CMOS inverter and a PMOS pass transistor. The input B become a high .The CMOS inverter behaves like a simple inverter. The output become of XOR gate is the complement of input A.The single bit Adder sub tractor circuit is shown in Fig 7 in which 1 bit adder subtractor circuit is constructed by using 1 bit xor and 1 bit full adder. Similarly by cascading 8 single bit add/sub 8 bit Adder Subtracter circuit is build shown in Fig 8 which is having inputs A0 to A7 and B0 to B7.If we operate of addition operation M is at low that is at zero when both A and B should be added on that time when this M=0 it operate as B xor 0 which is equal to B the full adder get value of b and input carry is low that is zero. For subtraction M=1 THEN B xor 1 which is equal to complement of B and carry input is high that is 1 and which is A minus B.C0 is the carry in which means when C0 is high it act as a adder circuit and when C0 is at low input it acts as a subtractor. Eight full adder circuit are cascaded to build 8 bit adder subtractor circuit. Cout is carry output line, S0 to S7 are output lines.

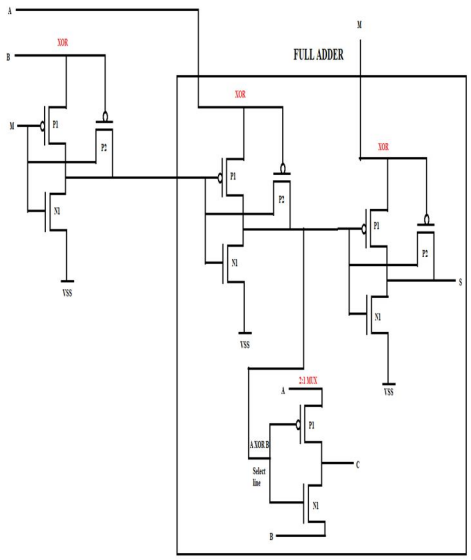


Fig 7: 1-Bit Adder/Subtractor circuit

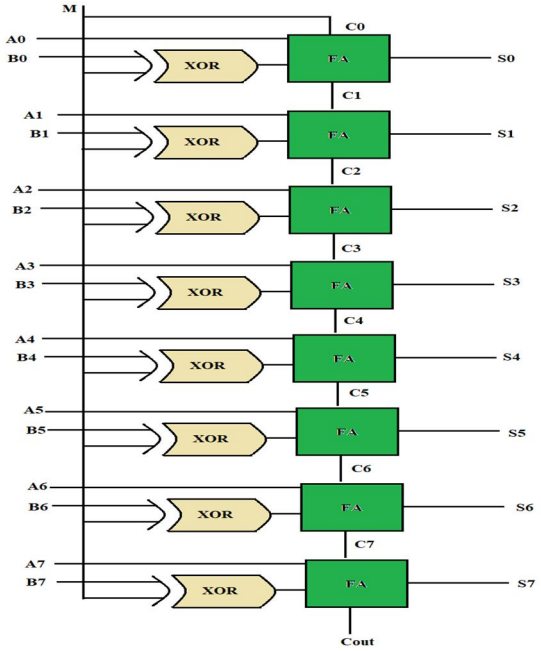


Fig 8: 8-Bit Adder/Subtractor circuit

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C. Increment Operation

In this increment operation adds one to the least significant bit in which for example the 8 bit register as value of 00000110 it will go to 00000111 as the incremented. The increment operation is done by cascading the half adder circuits. The single bit half adder which is designed by using 3T XOR and AND gate in which number of transistor is reduced in 3T XOR gate which leads to reduce in total number of transistor in half adder circuit hence in each single bit increment circuit reduces the number of transistor which is shown in Fig 9.Similarly 8-bit increment circuit is shown in Fig 10. In single half adder circuit input which is connected to the high input and also the number which as to be incremented that is A input which is shown in Fig 9 output s and also carry out is taken out which can be taken as a input to the other half adder circuit. If we consider 8 bit increment circuit which is shown in Fig 10 in which which is having input A0 to A7 and carry C0 to C7 and out put sum S0 to S7. The carry is zero at all condision except when all input bit are at high that is 1 then the carry is at 1 which is clearly shown in the table 4.

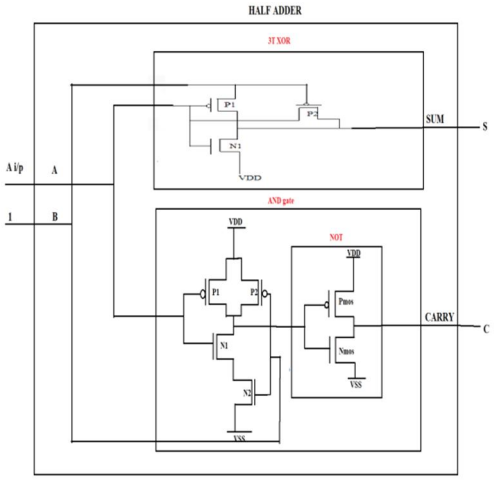


Fig 9:1-Bit Increment circuit

	INPUT	OUTPUT	
Cin	**A**	**SUM**	**Carry Out**
1	**00000001**	**00000010**	**0**
1	**00001011**	**00001100**	**0**
1	**10111011**	**10111100**	**0**
1	**11111111**	**00000000**	**1**
1	**01111111**	**10000000**	**0**
1	**01111110**	**01111111**	**0**

Table 4:Increment logical operation

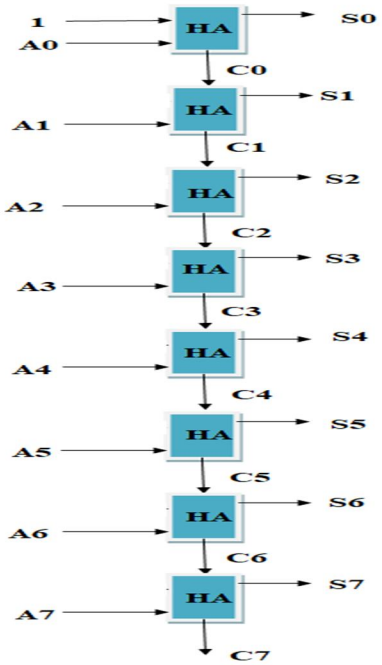


Fig 10: 8-Bit Increment circuit

D. Decrement Operation

The single bit decrement required one full adder in which the full adder construction is explained in 3.2. and also single bit decrement circuit is shown in Fig 11.To design a 8 bit decrement 8 full adder circuit are cascaded together to form a 8 bit decrement. A 8 bit Decrement circuit is shown Fig 12. A 8-Bit binary decrement circuit is created by cascading 8 fulladder circuit in which each full adder having input high and also inputs A0 to A7,carruin Cin,carryout Cout and outputs S0 to S7 which is shown in Fig 12.

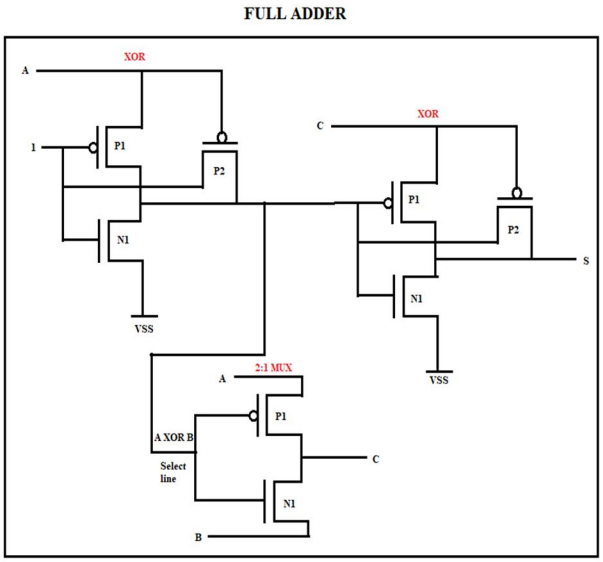


Fig 11: 1-Bit Decrement circuit

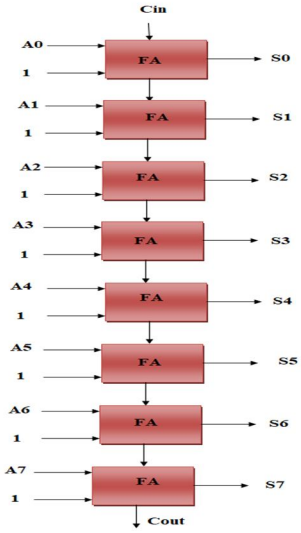


Fig 12:8-Bit Binary decrement circuit

E. Shift Left/Right Operation

For shift operation we need 2X1 MUX that is for single shift it requires 1 MUX the single bit mux is explained in 3.1 hence to construct 8 bit shift operation eight 2X1 MUX is cascaded together to construct a 8 bit shift left/right. In Fig 13 which shows the circuit diagram of 8 bit shift left/right.

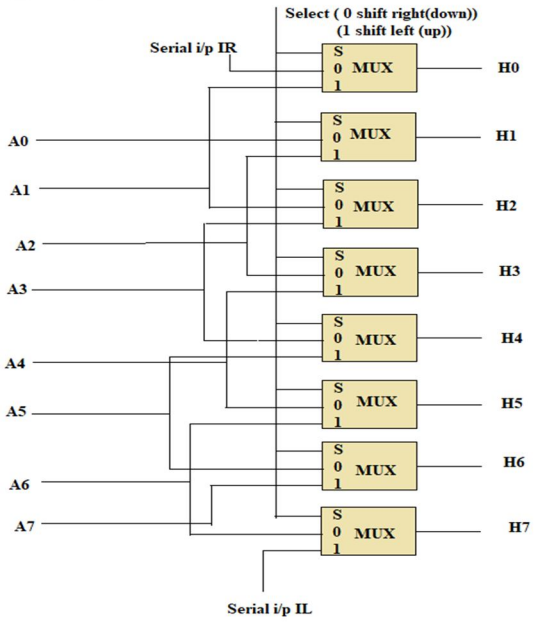


Fig 13: 8-Bit Shift Left/Right circuit

Table 5: Function table

Select	Outputs							
S	H0	H1	H2	H3	H4	H5	H6	H7
0	IR	A0	A1	A2	A3	A4	A5	A6
1	A1	A2	A3	A4	A5	A6	A7	IL

The 8 bit shift left/right circuit is designed by using mux circuits which is shown in the Fig 13 and as shown in the above figure that each mux which are having data input lines that is the data input line in 8 bit shift left/right circuit are A0 to A7 and also which are having serial input lines IL and IR and also which is having a selector which is used to select the mode of operation that is for left the selector is selected as high that is 1 and for the shift right operation the selector is selected as low that is 0.This 8 Bit shift operation is shown in table 5.

F. And Operation

The AND gate which is having the two input and output which is shown in Fig 14 in this AND gate the output is high only when the both inputs are at high or if any of the input is low then the output is low.

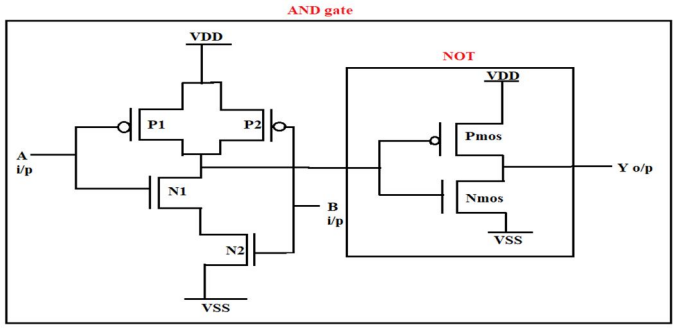


Fig 14: 1-Bit AND gate circuit

Table 6:Truth table of AND gate

A Input	B Input	Y Output
0	0	0
0	1	0
1	0	0
1	1	1

The AND output is low when any of inputs are at logic 0. The expression of AND gate is A.B = F where the expression given for a AND gate the dot denotes multiplication. The logical operation is shown in truth table 6 .Fig 15 which shows the 8-Bit AND gate circuit diagram eight 1 bit AND gate cascaded together to create 8 bit AND which is having inputs A0 to A7,B0 to B7,and which are connected to supply VDD and ground VSS out puts are Y0 to Y7.

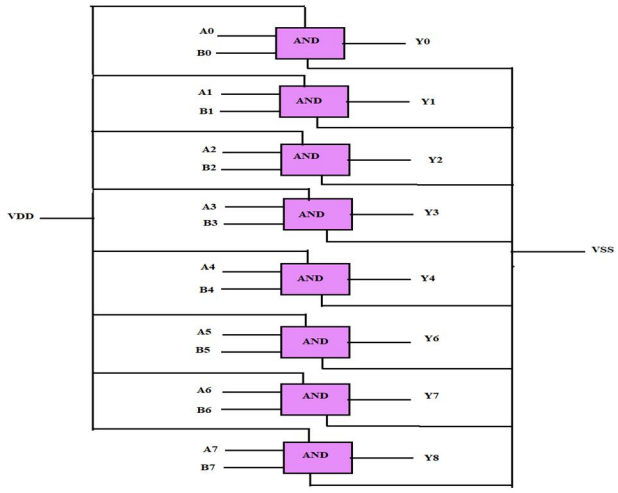


Fig 3.15: 8-Bit AND gate circuit

G. Or Operation

In this OR operation a high output that is 1 when any of the input is high when both the inputs are at zero then it results in low out put that is 0.OR gate truth table is shown in table 7.

Table 7:OR truth table

Input A	Input B	Output Y
0	0	0
0	1	1
1	0	1
1	1	1

A single bit or gate using four transistor is shown in Fig 3.16 Here in this project 4 transistor OR gate by using pass transistor logic which is explained in 3.2 and this 4T ORgate which is constructed to reduce the total number of transistors and also which performs as same as complimentary cmos the 4 transistor 8 bit OR gate ciecuit diagram is shown in Fig 3.17 in which it is having inputs A0 to A7,B0 to B7,supply VDD and ground VSS along with outputs Y0 to Y7.

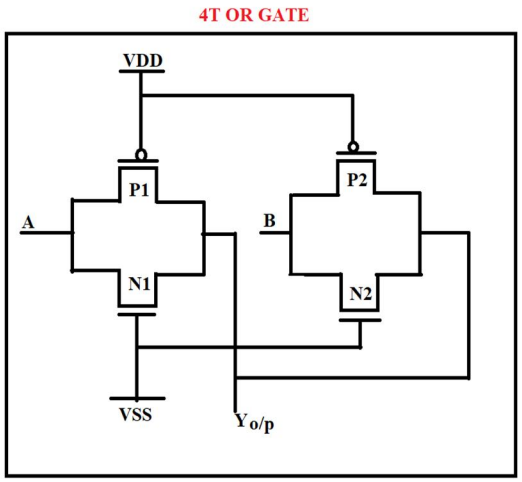


Fig 16:1-Bit OR gate

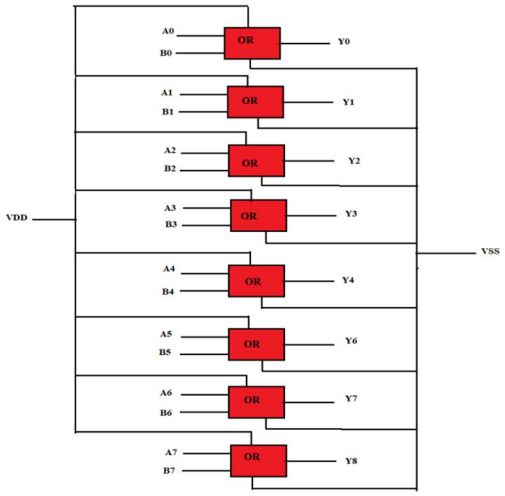


Fig 17 : 8-Bit OR gate circuit

H. 8X1 MUX Design for ALU Operations

In this a 8x1 MUX is constructed by cascading 2x1 MUX in which it is explained in 3.1.Let us explain 8x1 MUX which is having 8 input lines having signals as I0 to I7 for selecting one selecting line in 8 inputs signals. We require addresses which can be a three bit word the address line are designated as a S_0,S_1,S_2 which is shown in Fig 18

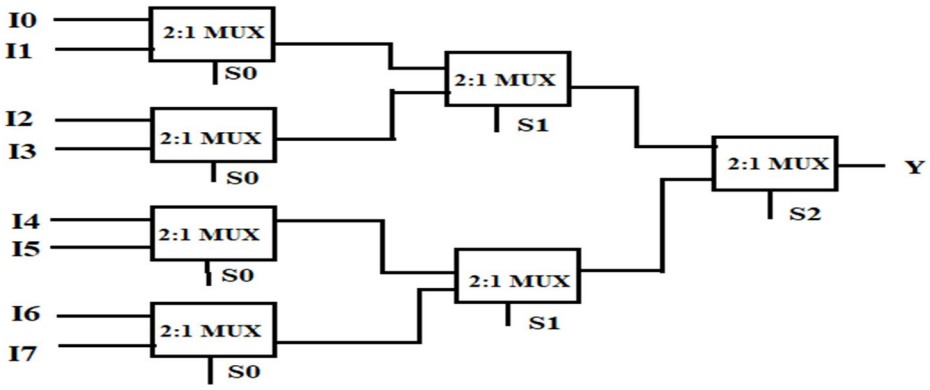


Fig 18: 8x1 MUX circuit

Table 8: 8X1 MUX operation

No.	S2	S1	S0	Y	Operations
1	0	0	0	I0	Add/Sub
2	0	0	1	I1	Increment
3	0	1	0	I2	Decrement
4	0	1	1	I3	Shift
5	1	0	0	I4	NOT
6	1	0	1	I5	AND
7	1	1	0	I6	OR
8	1	1	1	I7	XOR

Table 8 which shows the arithmetic logic unit mode of operation in which the arithmetic and logical operations are selected by using select lines S1,S2 and S3.When selecting lines are at S2=0.S1=0 and S3=0 the the output line I0 selected and Add/Sub operation will executed, when it is at 001 the output line I1 selected and increment operation will execute, when 010 the output line I2 selected and Decrement operation will execute, when 011 the output line I3 selected and Shift operation will execute, when 100 the output line I4 selected and NOT operation will executed, when 101 the output line I5 selected and AND operation will executed, when 110 the output line I6 selected and OR operation will executed, when 111 the output line I7 selected and XOR operation will executed by using this 8x1 MUX a ALU was designed in this project. Schematic Fig 19, test bench Fig 20 and waveform Fig 21 of 8x1 MUX.Total number of transistor used in 8X1 MUX is 14.

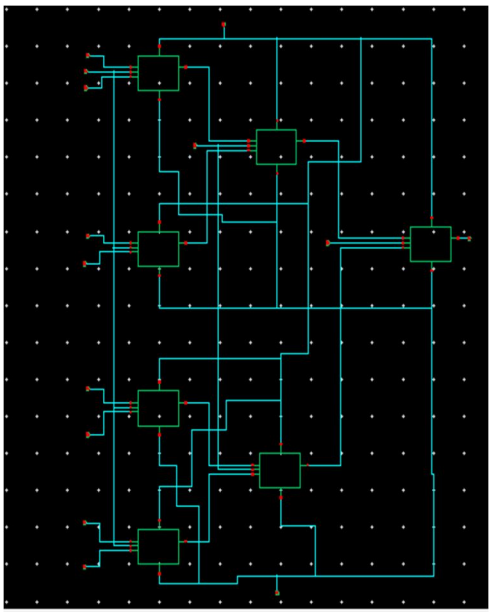


Fig 19: 8-bit MUX schematic

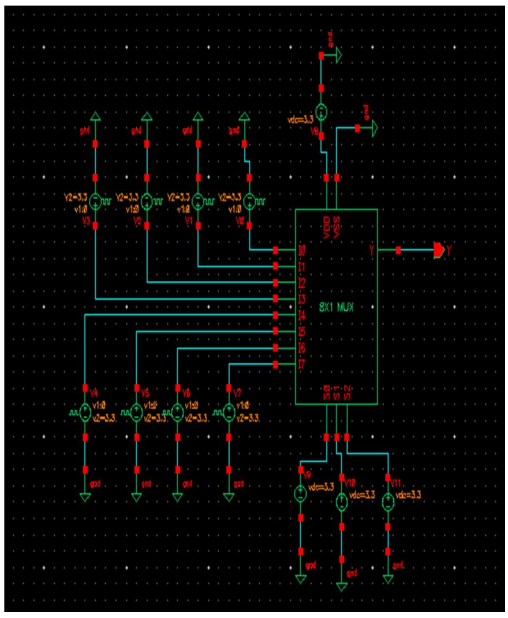
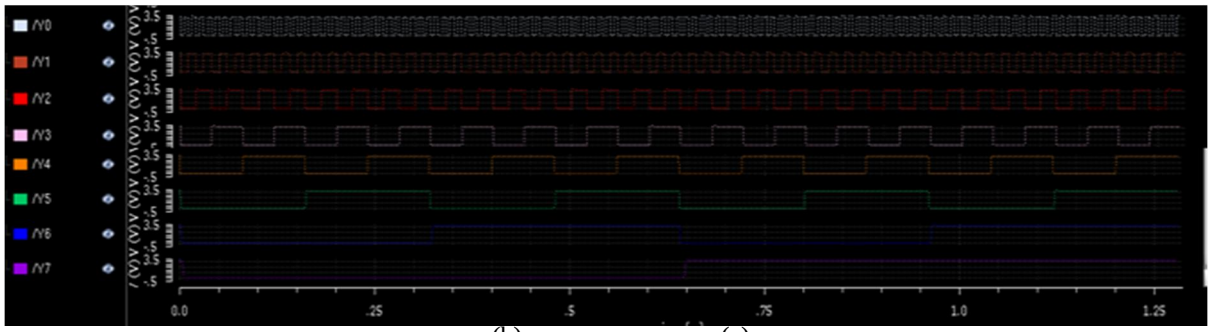


Fig 20:8-Bit MUX testbench



(b) (c)

Fig 21: 8-Bit MUX waveform

IV. DETAILED DESIGN OF 8 BIT ARITHMETIC LOGIC UNIT

Here we provide detailed design of 8 bit arithmetic logic unit.

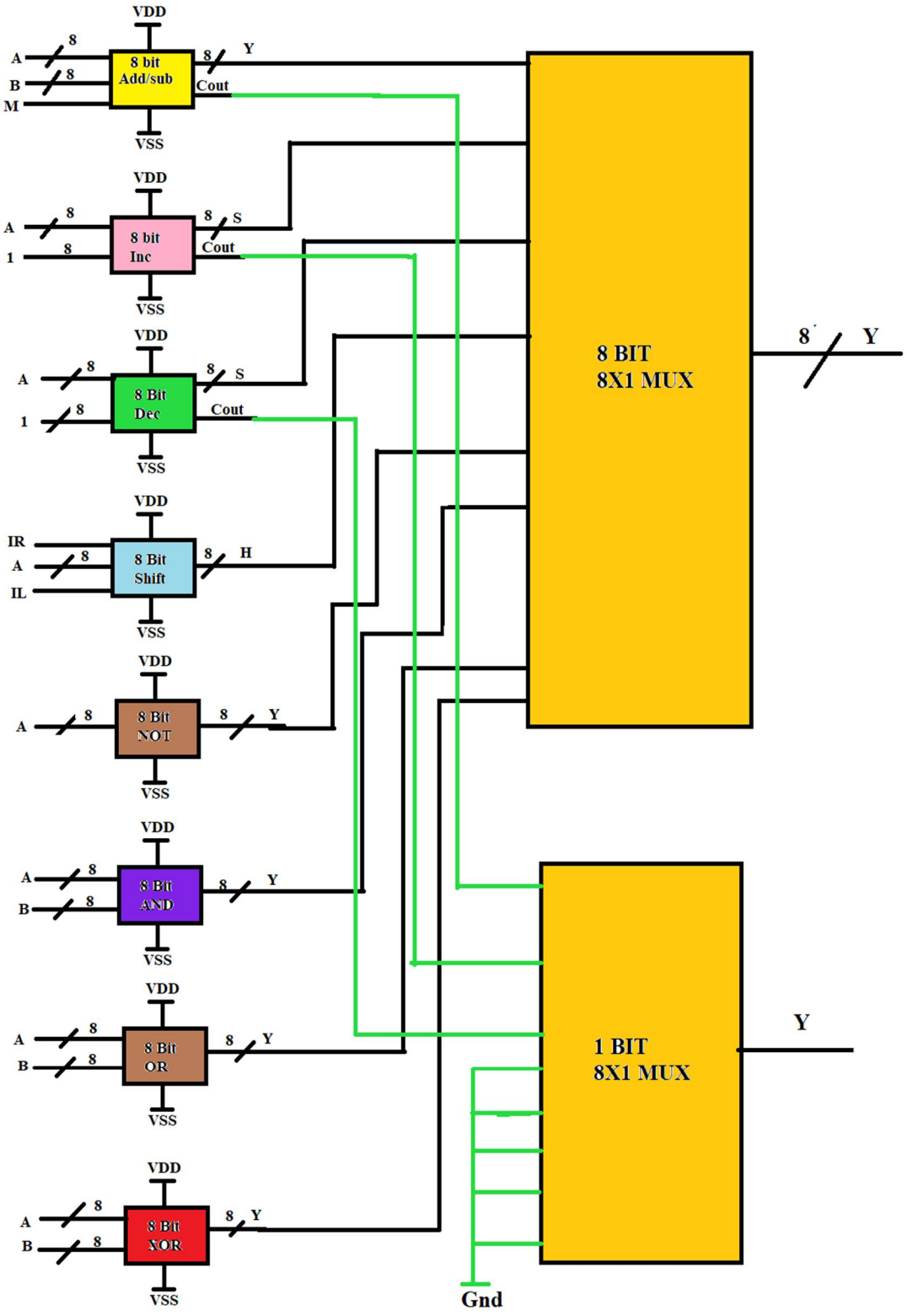


Fig 22:8-Bit Arithmetic logic unit circuit

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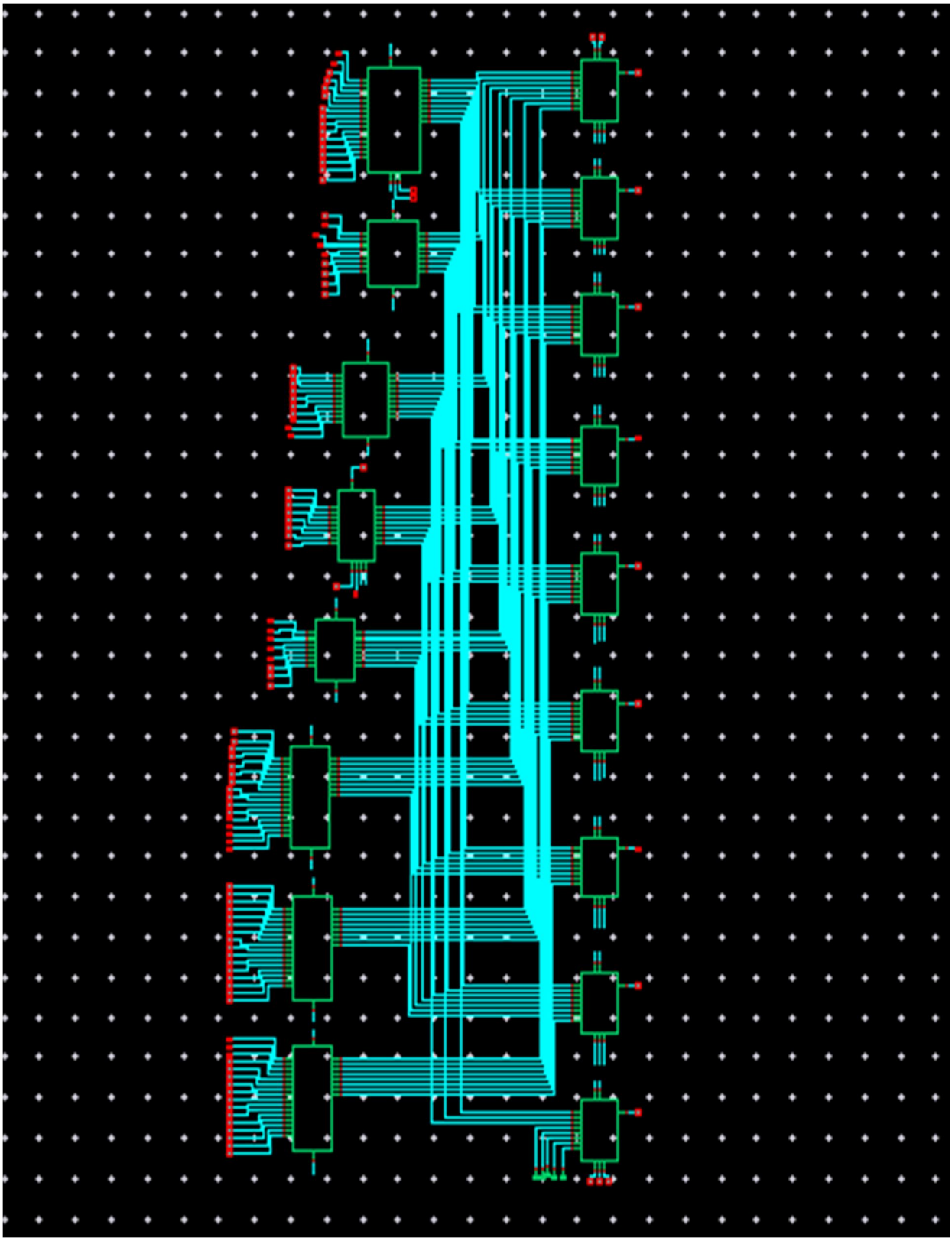

Fig 23: Final 8-Bit Arithmetic logic unit design schematic

The complete design of this arithmetic logic unit is shown in Fig 22 in which each that is both arithmetic and logical operation the arithmetic operation selected in this project is addion subtraction increment decrement shift and also logical operation lik AND OR XOR NOT were selected in logical operation.when we select the selecting lines at 000 the addition/subtraction will take place when it is at logic 0 it will perform as a adder and when it is at logic 1 it perform as subtractor the operation are perform respectively.like that each and every arithmetic and logic operations are done by choosing the selecting lines S2 S1 S0 which is clearly explained in chapter 4.The operation performed by arithmetic logic unit is shown in table 6 in which it shows the selecting lines which should select to perform appropriate operatios and the full schematic is shown in Fig 23.In this 8 bit arithmetic logic unit having three selecting lines, and nine out put Y0 to Y7. And this entire 8 bit ALU design have 104 inputs.among them for add/sub address lines are that is i/p lines are A0_AS to A7_AS, B0_AS to B7_AS,M_AS,Cin_AS which is clearly explained in 3. Increment address lines are that is i/p lines are A0_INC to A7_INC, B0_INC to B7_INC,High_INC which is clearly explained in 4.Decrement address lines are that is i/p lines are A0_DEC to A7_DEC, B0_DEC to B7_DEC,High_DEC, Cin_DEC which is clearly explained in 5. Shift address lines are that is i/p lines are A0_SLR to A7_SLR, B0_SLR to B7_SLR, Select_ SLR ,IL_SLR and IR_SLR and which is clearly explained in 6. XOR address lines are that is i/p lines are A0_XOR to A7_XOR, B0_XOR to B7_XOR which is clearly explained in 2. NOT address lines are that is i/p lines are A0_INV to A7_INV which is clearly explained in 1. AND address lines are that is i/p lines are A0_AND to A7_AND, B0_AND to B7_AND which is clearly explained in 7.OR address lines are that is i/p lines are A0_OR to A7_OR, B0_OR to B7_OR which is clearly explained in 8.The 8 bit arithmetic logic unit is designed using cadence virtuoso platform in this project Total transistor count used in entire ALU design in this project is 774

V. RESULTS AND DISSCUSSION

Here overall result and discussion of the proposed system.In this work, the designing and the simulated result done at each stages is explained which are done by using cadence virtuoso tool by using 180nm technology.

A. 8 Bit Adder/Subtractor when MUX selected as S2=0 S1=0 AND S0=0

When then MUX select line set at 000 then it perform the arithmetic operation that is Add/Sub operation and which select the I0 as input lines which is Add/Sub. Add/sub is clearly explained in section 3 the schematic is shown in Fig 24 and testbench is shown in Fig 25 and output wave form in Fig 26 and also total transistor in Adder subtractor circuit is 216.

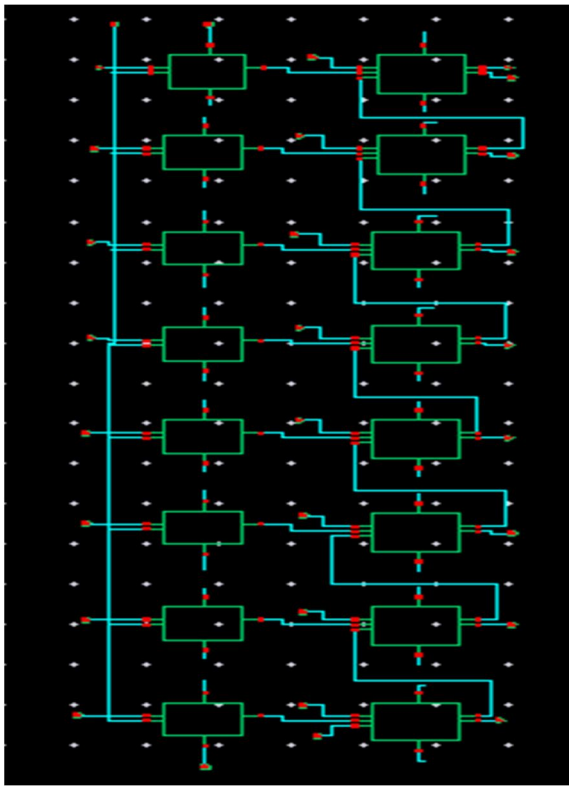

Fig 24:8-Bit Add/Sub schematic

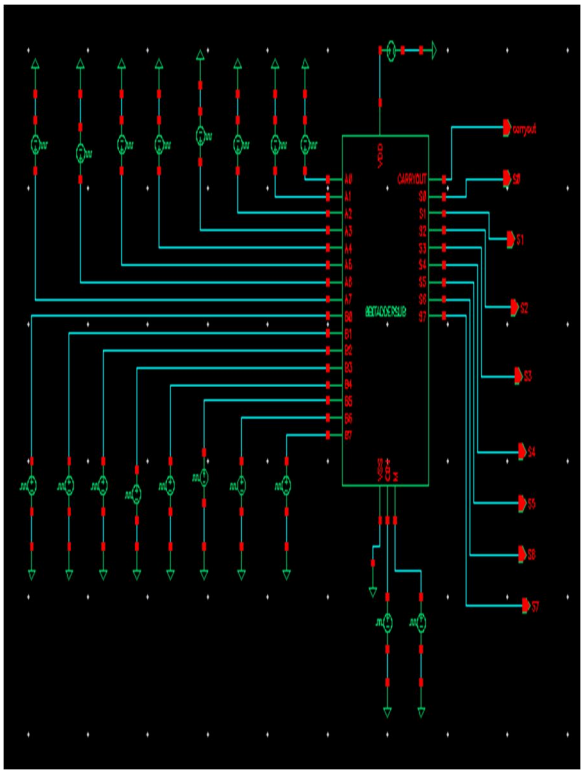

Fig 25:8-Bit Add/Sub testbench

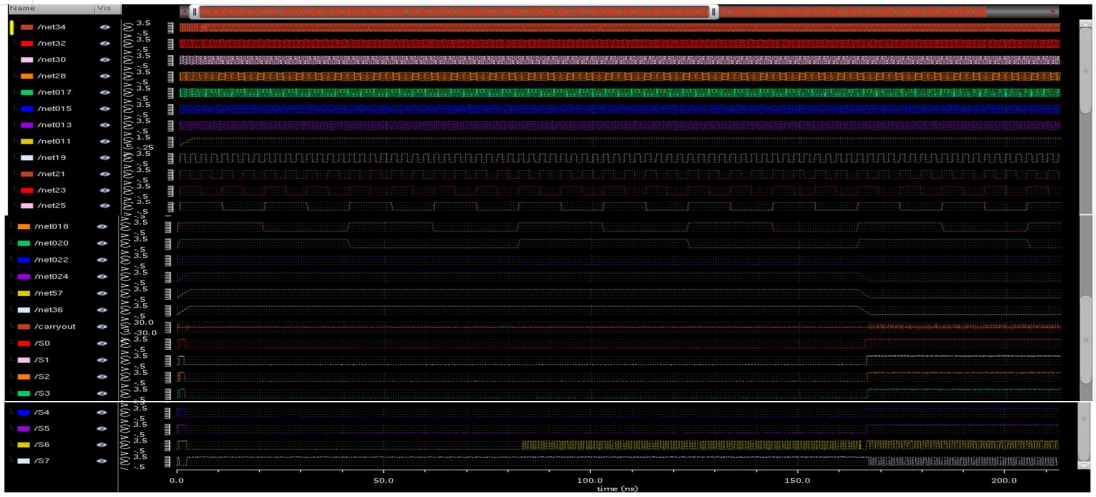

Fig 26:8-Bit Add/Sub output wave form

B. 8-Bit Increment when MUX selected as S2=0 S1=0 AND S0=1

When then select line set at 001 then it perform the arithmetic operation that is Increment operation and which select the I1 as input lines. Increment which is clearly explained in section 4 the schematic is shown in Fig 27 and testbench is shown in Fig 28 and output wave form in Fig 29 transistor used in Increment circuit is 104.

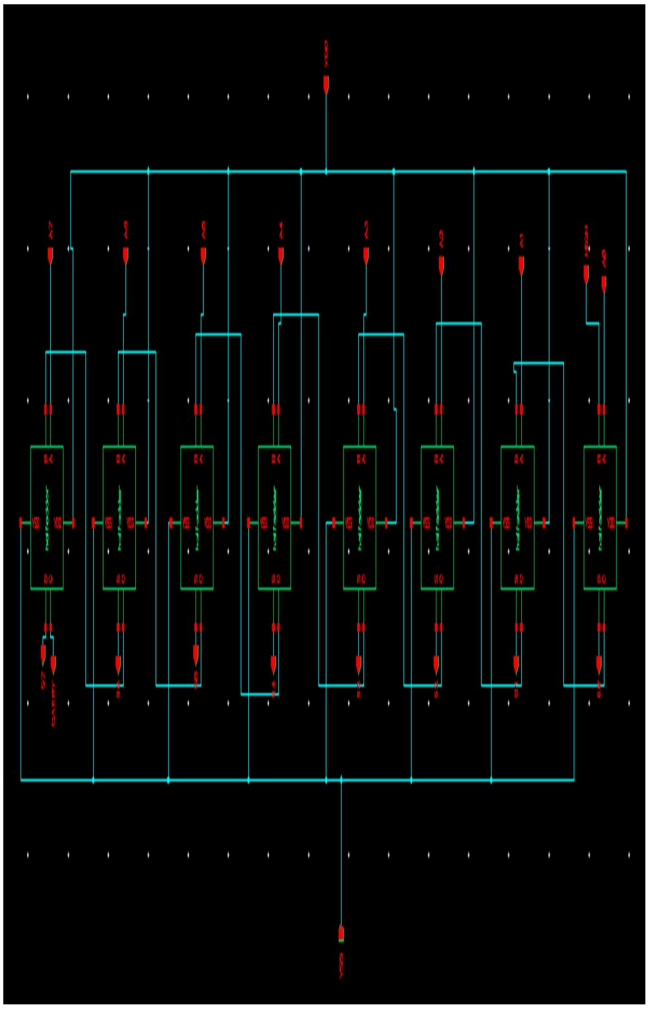

Fig 27: 8 Bit increment schematic

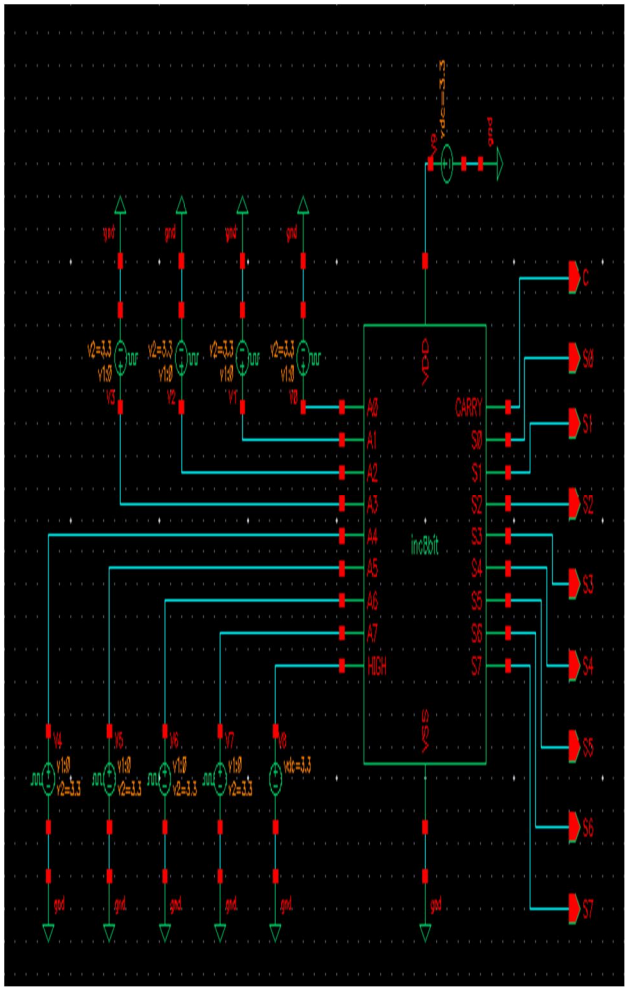

Fig 28: 8 Bit increment testbench

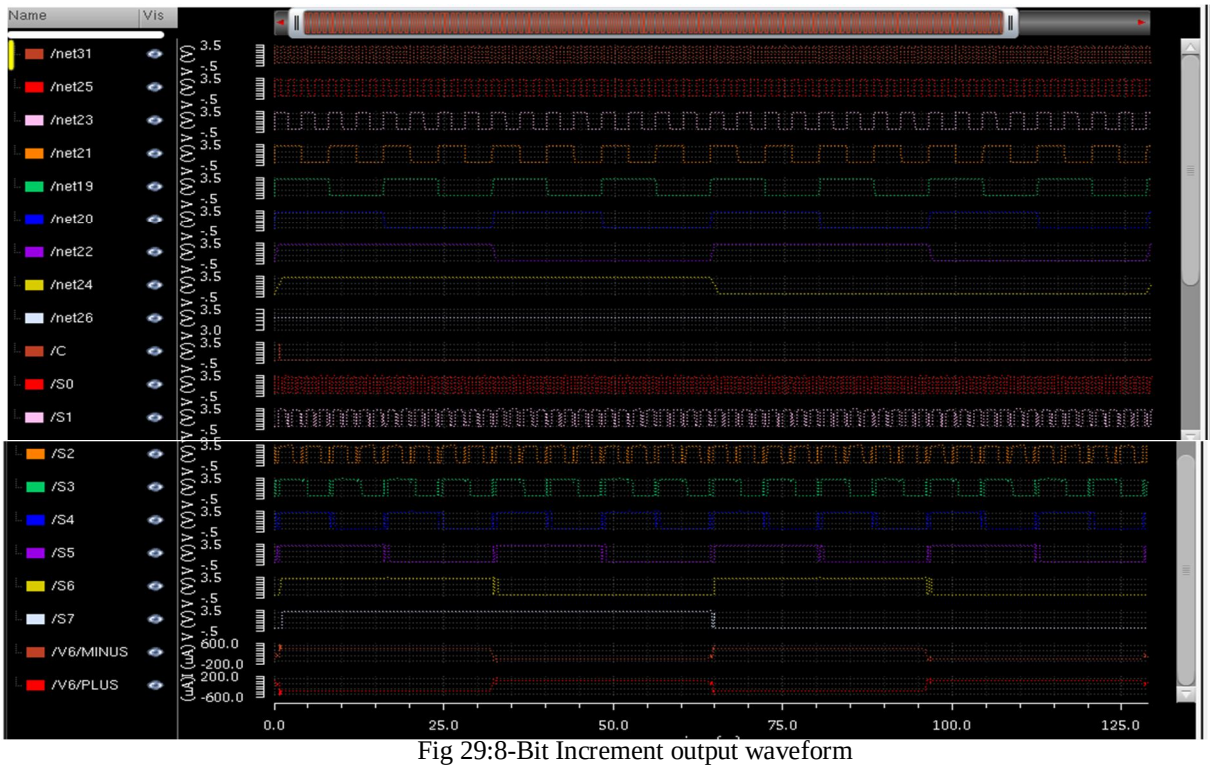

Fig 29:8-Bit Increment output waveform

C. 8-Bit Decrement When MUX selected as S2=0 S1=1 AND S0=0

When then select line set at 010 then it perform the arithmetic operation that is Decrement operation and which select the I2 as input lines. Decrement which is clearly explained in section 5 the schematic is shown in Fig 30 and testbench is shown in Fig 31 and Fig 32 output wave form.Transistor count in Decrement circuit is 160.

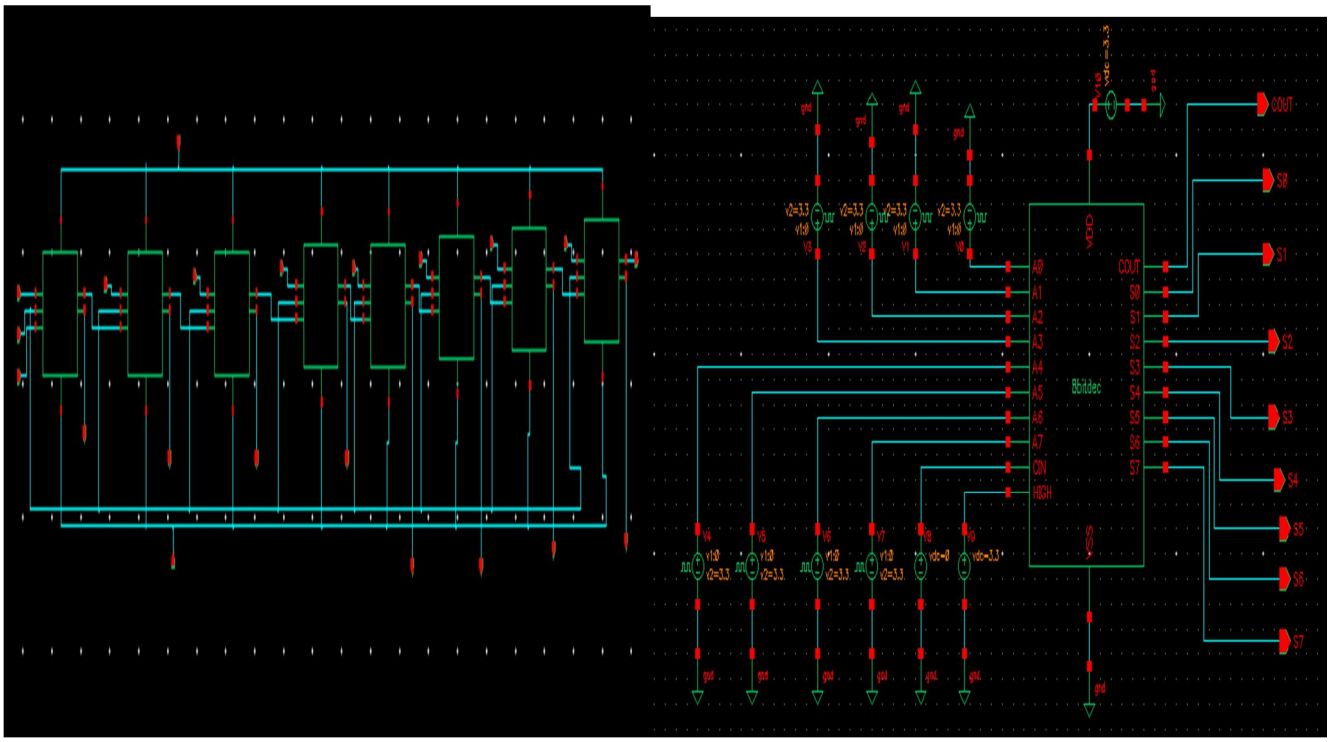

Fig 30: 8 Bit Decrement schematic

Fig 31 :8-Bit Decrement testbench

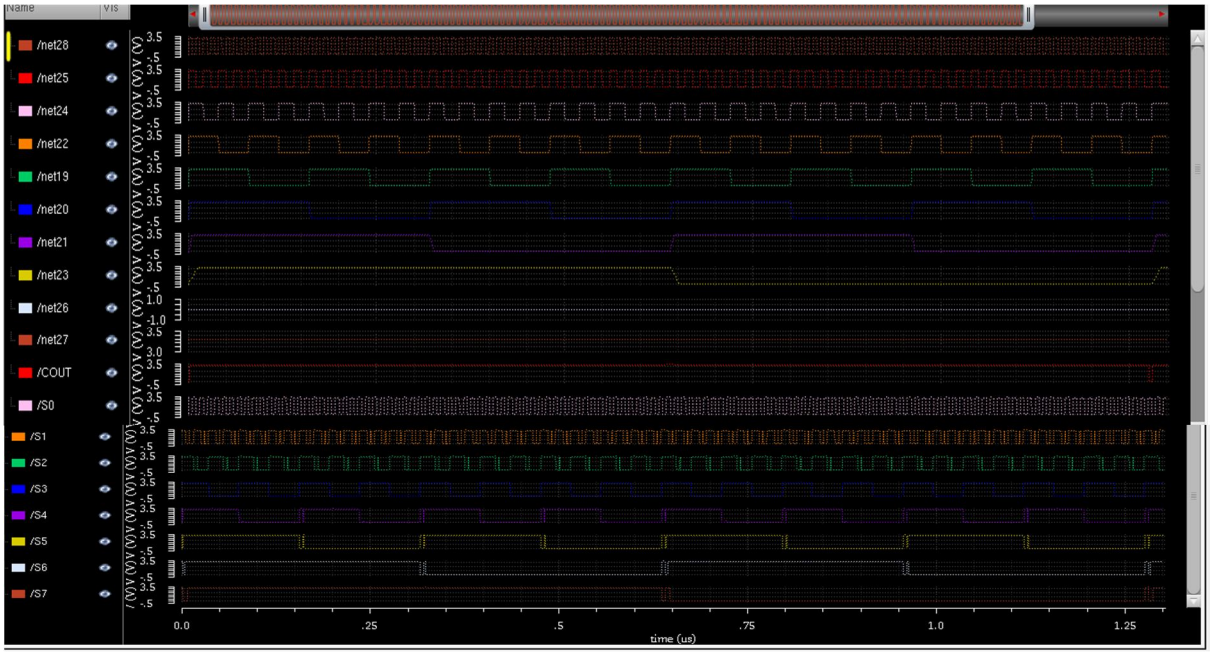

Fig 32:8-Bit Decrement output wave form

D. 8-Bit Shift Left/Right When MUX selected as S2=0 S1=1 AND S0=1

When then select line set at 011 then it perform the arithmetic operation that is shift operation and which select the I3 as input lines. Shift which is clearly explained in section 6 the schematic is shown in Fig 33 and testbench is shown in Fig 34 and output wave form in Fig 35 number of transistor in Shift circuit is 16.

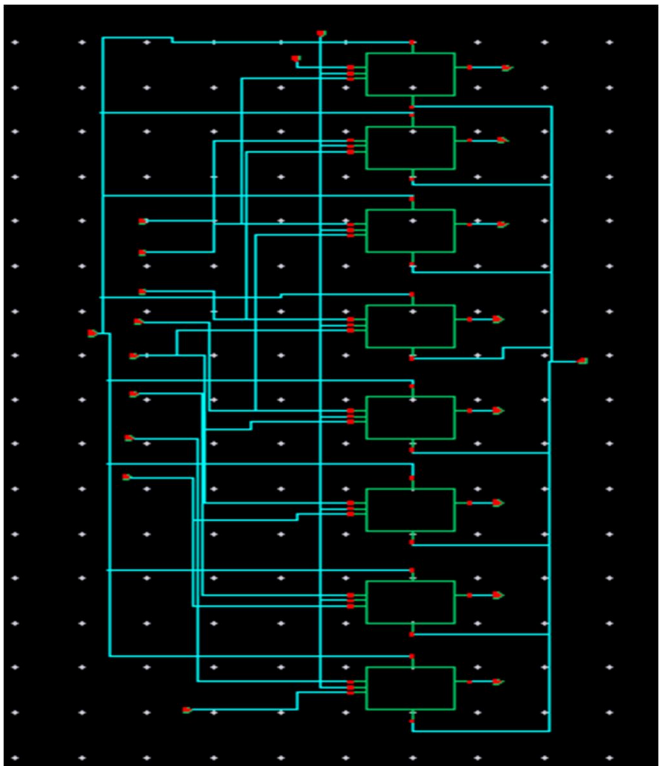

Fig 33:8-Bit Shift left/right schematic

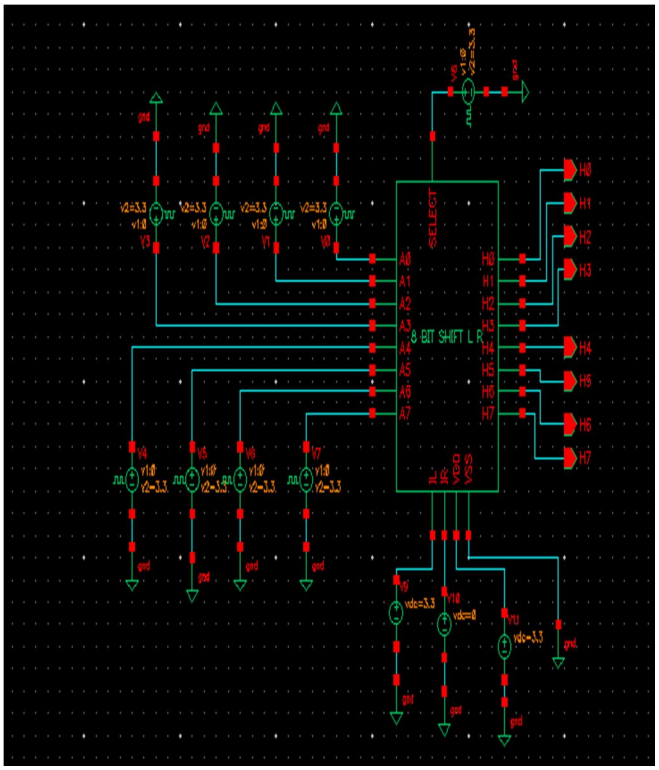

Fig 34:8-Bit Shift left/right testbench

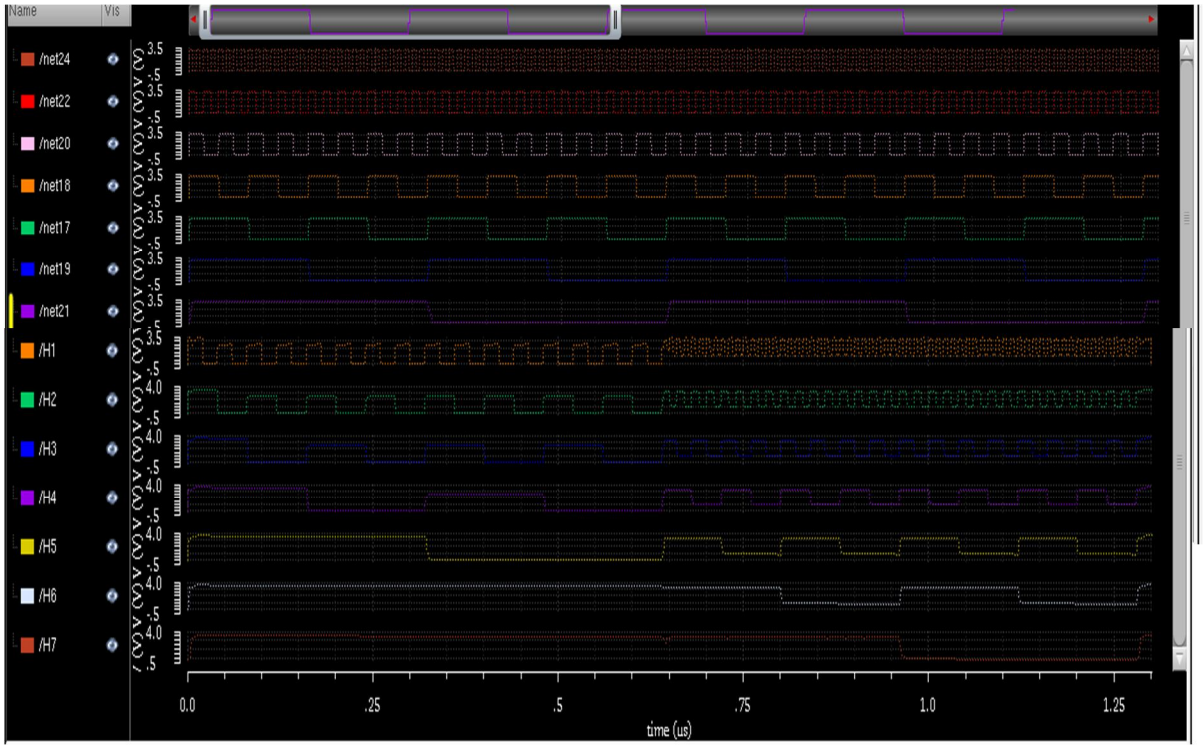

Fig 35:8-Bit Shift left/right output waveform

E. 8-Bit NOT gate When MUX selected as S2=1 S1=0 AND S0=0

When then select line set at 100 then it perform the logical operation that is NOT operation and which select the I4 as input lines. NOT operation which is clearly explained in section 1 the schematic is shown in Fig 36 and testbench is shown in Fig 37 and output wave form Fig 38 and also transistor count in NOT circuit is 16.

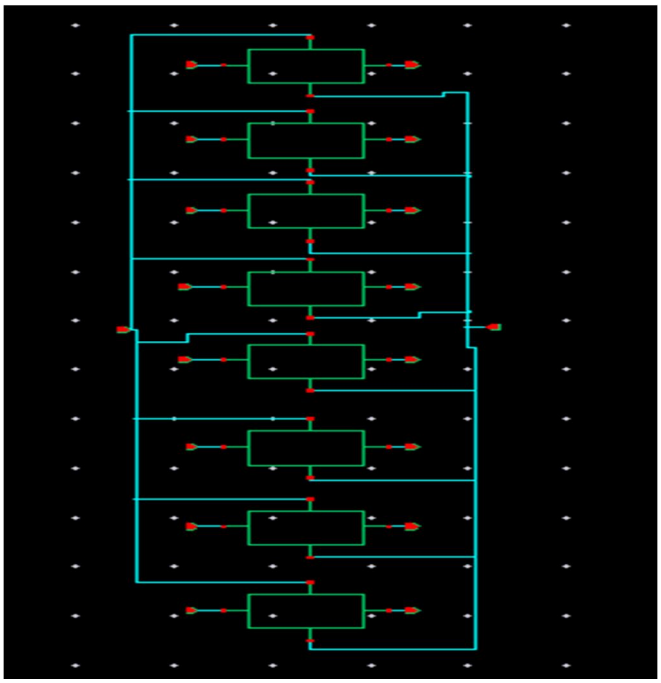

Fig 36:8-Bit NOT schematic

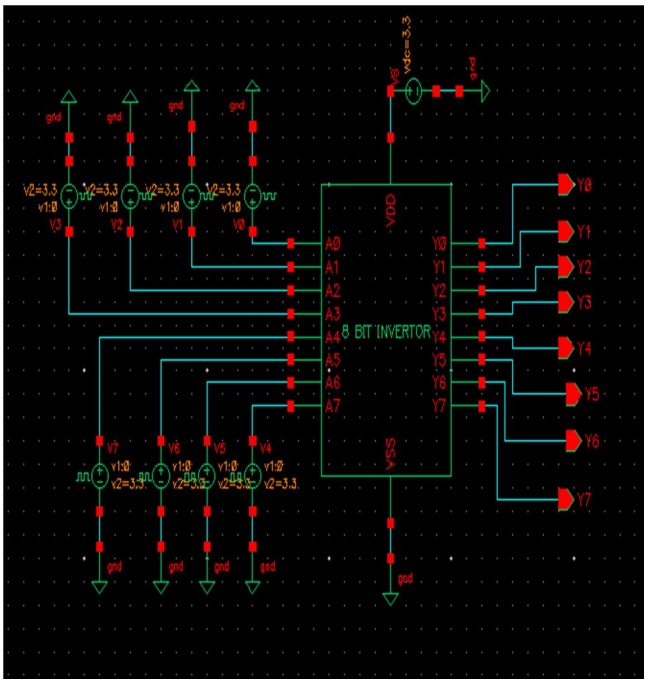

Fig 37:8-Bit NOT testbench

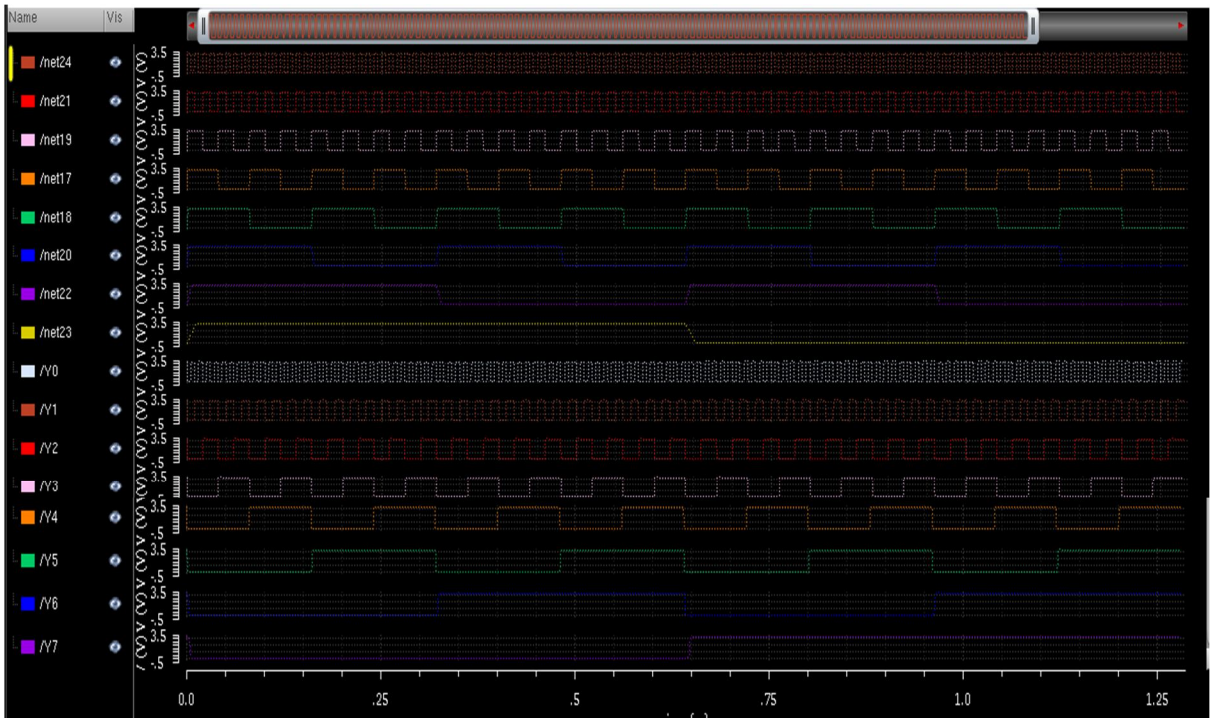

Fig 38:8-Bit NOT output waveform

F. 8-Bit AND gate When MUX selected as When S2=1 S1=0 AND S0=1

When then select line set at 101 then it perform the logical operation that is AND operation and which select the I5 as input lines. AND operation which is clearly explained in section 7 the schematic is shown in Fig 39 and testbench is shown in Fig 40 and Fig 41 output wave form.Transistor count in AND circuit is 48.

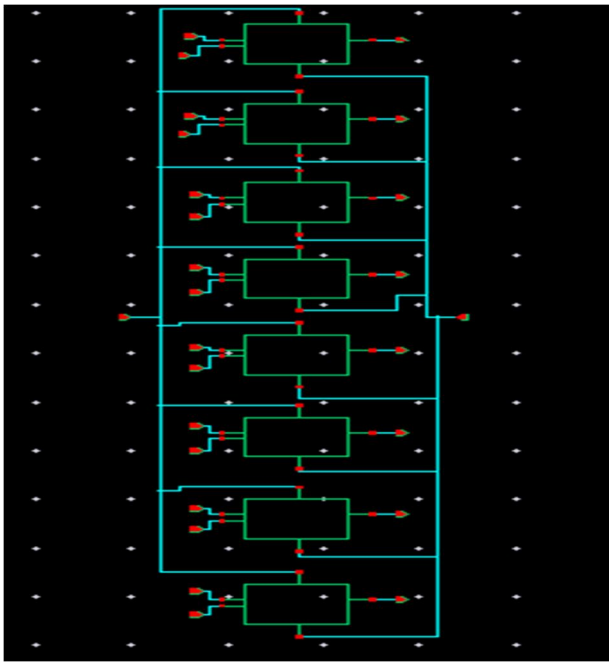

Fig 39: 8-Bit AND schematic

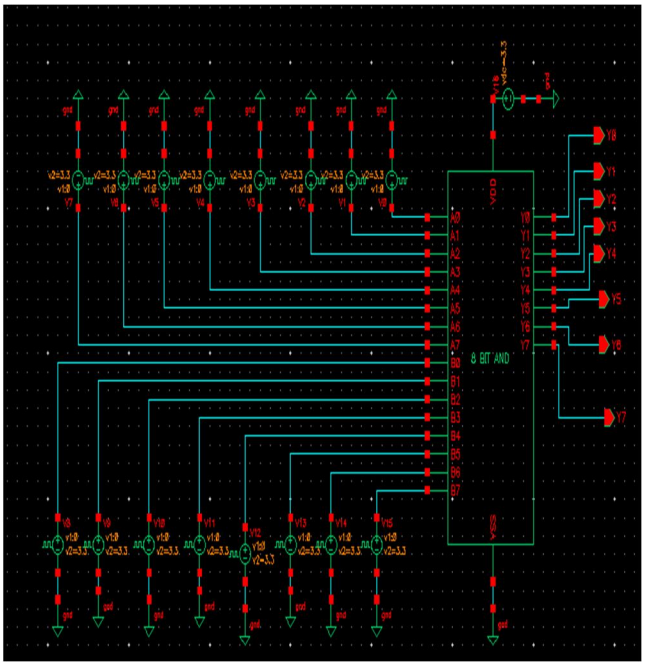

Fig 40: 8-Bit AND testbench

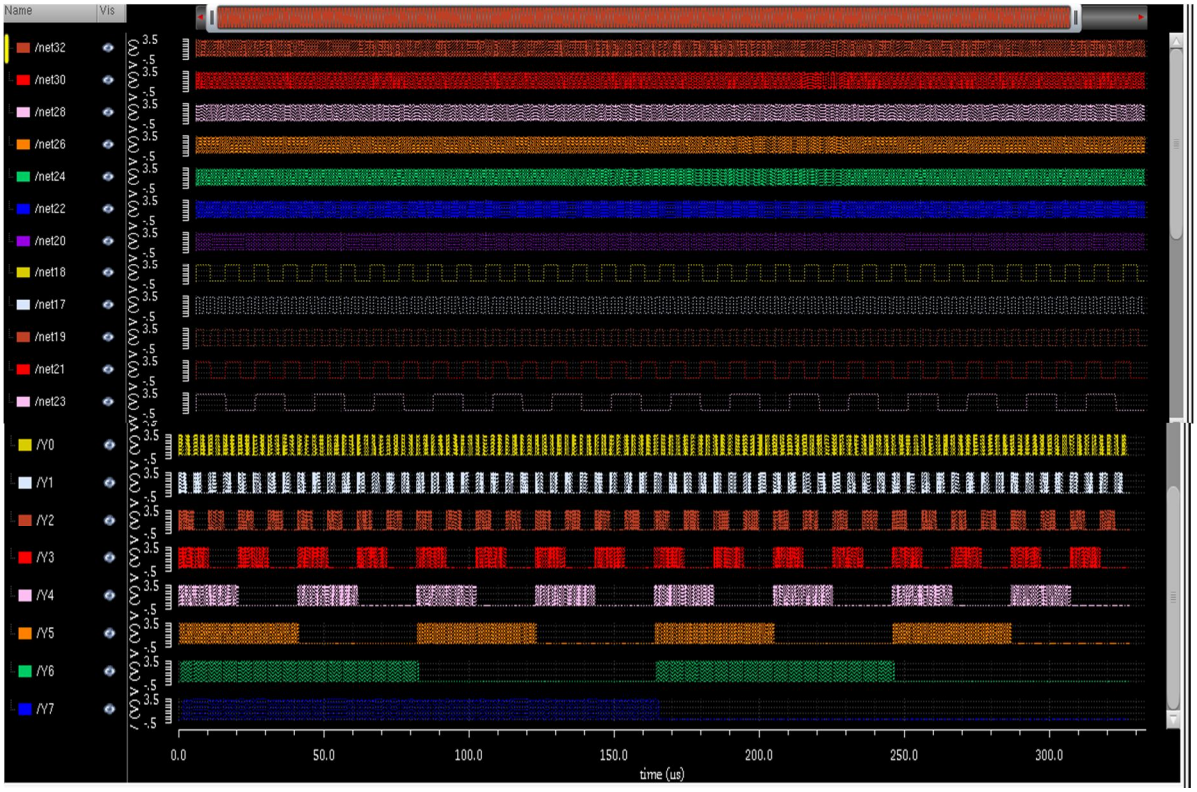

Fig 41: 8-Bit AND output waveform

G. 8-Bit OR gate when MUX selected as S2=1 S1=1 AND S0=0

When then select line set at 110 then it perform the logical operation that is OR operation and which select the I6 as input lines. OR operation which is clearly explained in section 8 the schematic is shown in Fig 42 and testbench is shown in Fig 43 and Fig 44 output wave form and also having transistor count in OR circuit is 32.

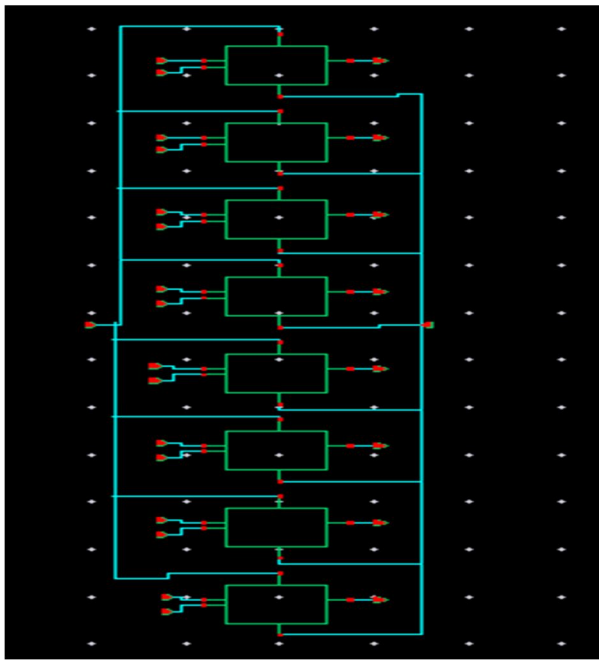

Fig 42: 8-Bit OR schematic

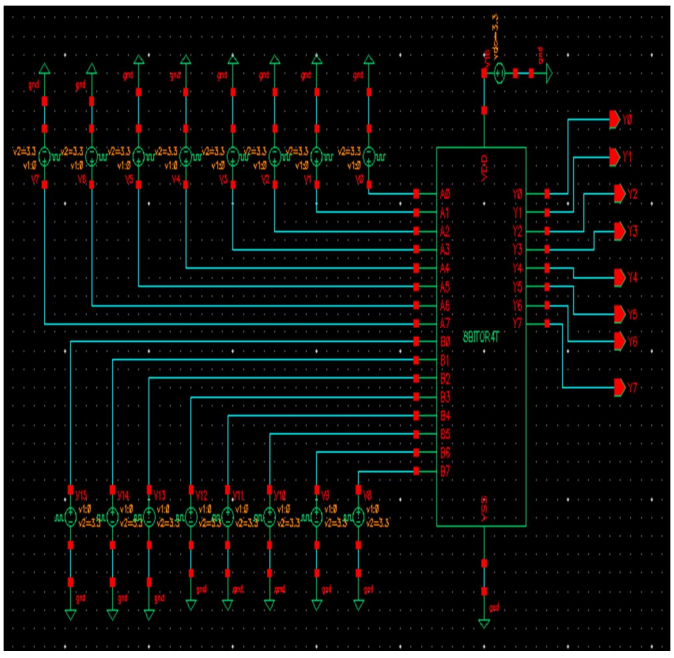

Fig 43: 8-Bit OR testbench

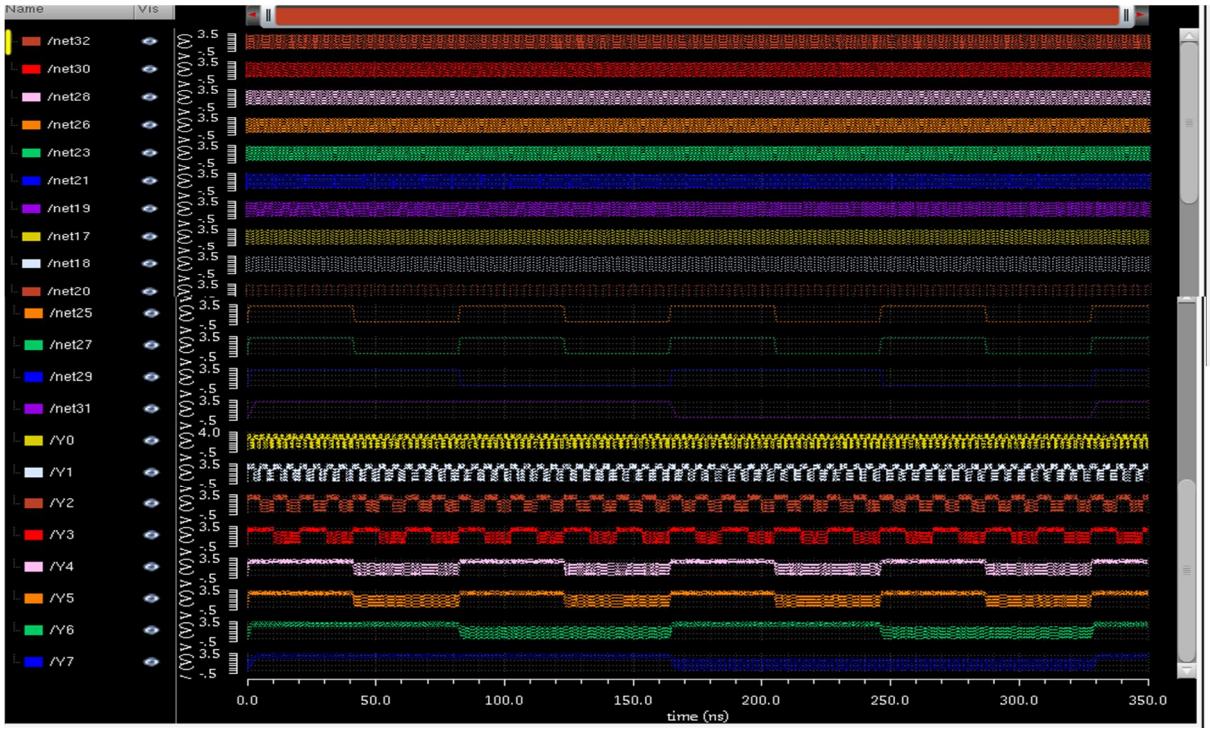

Fig 44: 8-Bit OR output waveform

H. 8-Bit XOR gate when MUX selected as S2=1 S1=1 AND S0=1

When then select line set at 111 then it perform the logical operation that is XOR operation and which select the I7 as input lines. XOR operation which is clearly explained in section 2 the schematic is shown in Fig 45 and testbench is shown in Fig 46 and Fig 47 output wave form and also transistor count in XOR circuit is 56.

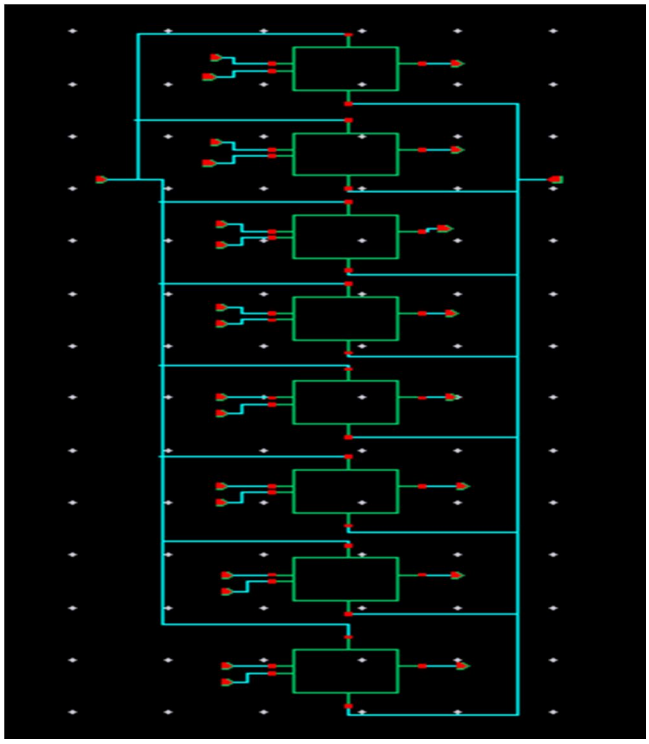

Fig 45: 8-Bit XOR schematic

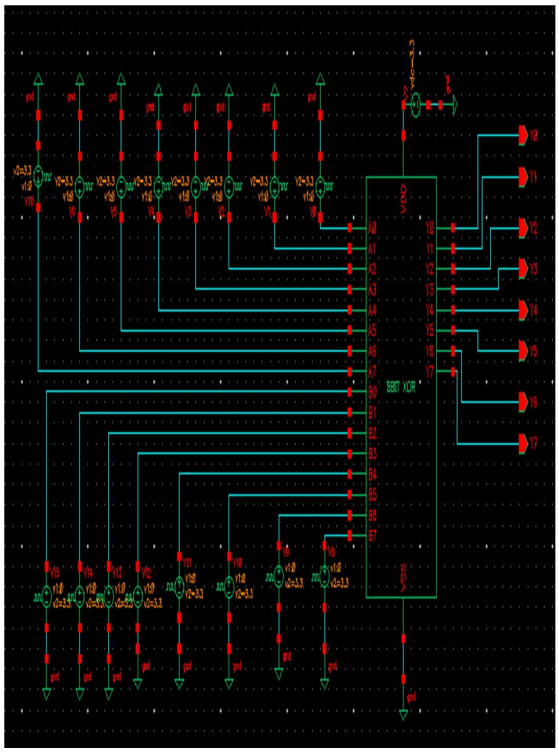

Fig 46: 8-Bit XOR testbench

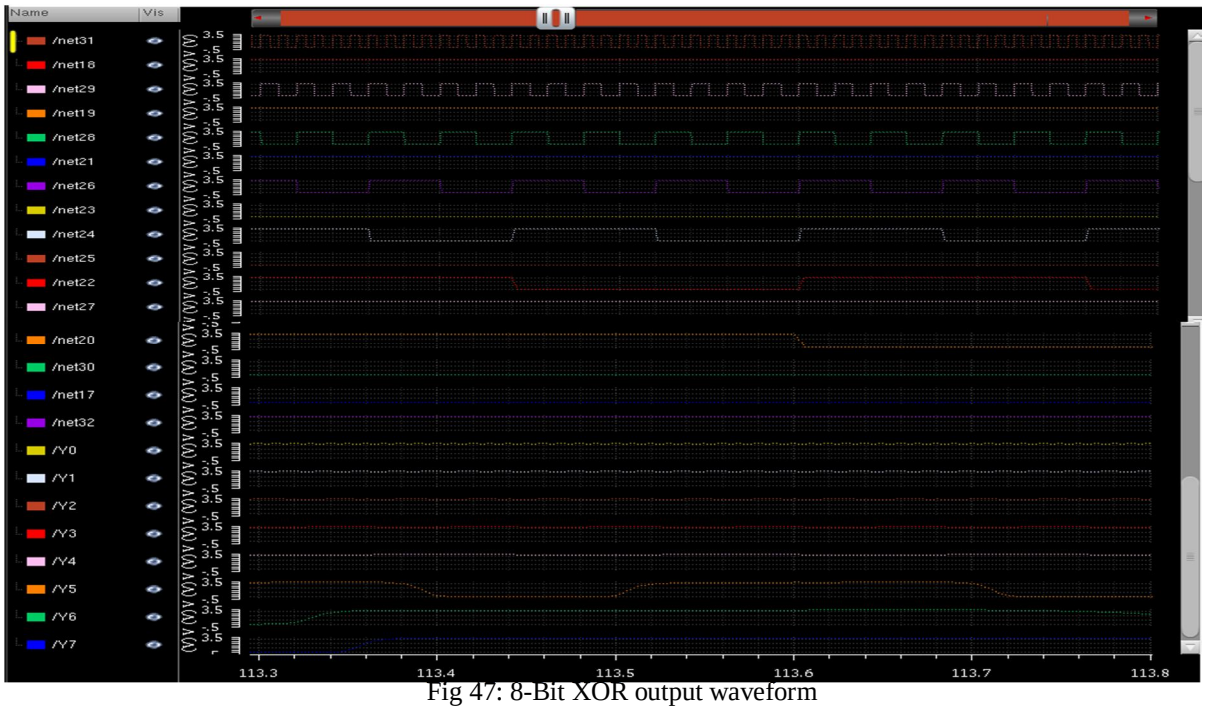

Fig 47: 8-Bit XOR output waveform

I. Number Of Transistor In Project

In this total number of transistor used in the entire project and also comparison of transistor count with conventional cmos is given in the below table in which total numbr of transistor used in this project was 774T.

Table 9

Operations	Conventional CMOS	Proposed
8 Bit Add/Sub	304T	216T
8Bit Increment	128T	104T
8 Bit Decrement	224T	160T
8 Bit Shift	48T	16T
8 Bit NOT	16T	16T
8 Bit AND	48T	48T
8 Bit OR	48T	32T
8 Bit XOR	80T	56T
8 Bit MUX	378T	126T

VI. CONCLUSION

The 8-Bit arithmetic logic unit is designed with minimal number of transistor by using cadence virtuoso tool. In this work, the different design is done by using different techniques combining the advantages and also focusing on limitations which can be used to optimizes the overall area by using different design aspects.

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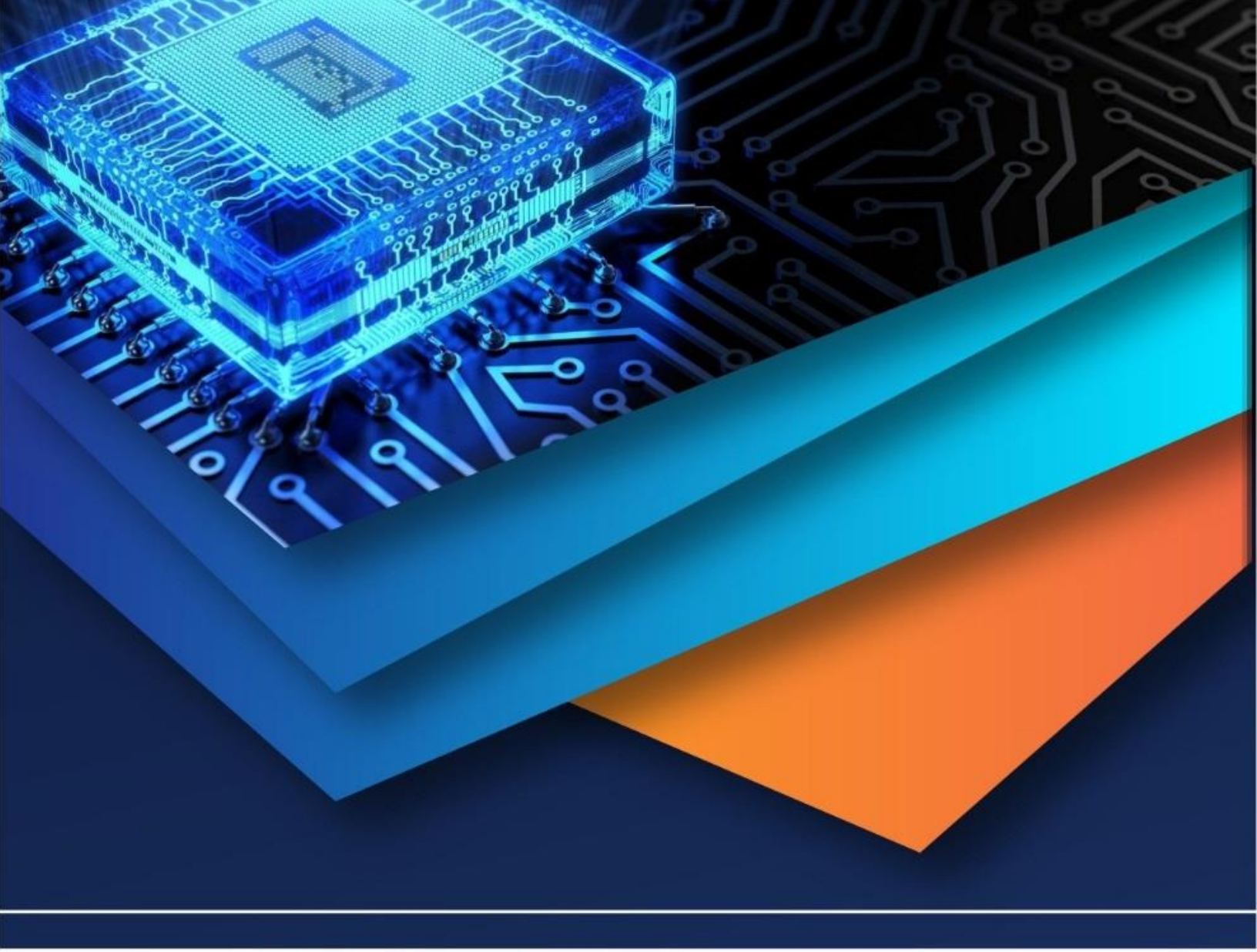

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