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A PTL Based Full Adder Design using Cadence

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Abstract: ***In recent days, demand for VLSI or ULSI has been improved drastically due to its robustness and efficiency. Due to peoples' demand of having miniature device with more battery life the VLSI Engineers are trying to innovate the existing designs by slightly modifying the pre-existing one. One of such examples is to use pass transistor logic, which has tremendous advantage over all other logics. Thus by exploiting the architecture of such logics may give rise to a device which satisfies all the demands of the market. In this work, the design of a low power and area efficient hybrid full adder is proposed which uses the pass transistor logic. The circuit has been designed and tested using minimum number of CMOS elements. The implementation of the design has been made in 180nm technology in CADENCE tool and it is simulated various times for numerous test cases. Also the design has been compared with the previously existing works. Thus the simulated results show the effectiveness in terms of area, speed and power dissipation.***
Keywords: Cadence virtuoso, DPL, PTL, SRCPL.

I. INTRODUCTION

Addition is a basic arithmetic operation, which is widely used in many applications specifically in DSP architecture and microprocessor. In recent years mobile communication is the fast growing technology which widely uses addition for its computation [1]. The operation like multiplication, subtraction, division, address generation and many other operations uses addition in direct or indirect form [2]. In electronics, the digital circuit which performs addition is commonly known as adder. They are used not only in computers but also in process. The basic function of adder is not restricted to add the logic units but also to calculate increment, decrement, addresses, table indices and in many similar operations. Various numerical representations are constructed by using adders. Commonly most of the adders do binary operations. Different ways of implementations can be made for a full adder with customized level of transistor circuits or combinations of gates.

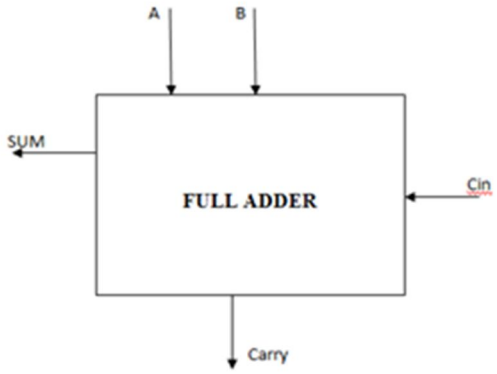


Figure 1.1: General Block diagram of Full adder

Function of any full adder is to add binary numbers and produces carry IN and OUT. Three 1- bits will be added by 1-bit full adder, often written as A, B and C as shown in figure 1.1; A and B are the operands, and C is a bit carried from the previously saved less significant stage. This 1-bit is usually cascaded to add multiple bits like 8, 16, 32, etc and produces 2-bit output, CARRY and SUM. Any integrated system is said to be optimal when it dissipates less power and occupies less silicon chip area. Today's integrated systems demands for low power designs. The efficiency of the arithmetic unit is determined by the efficiency of the adder circuit [3]. The demand for mobiles with ultimate battery power and high throughput capability is increasing robustly. This increases the importance of designing the low power adder cells.

II. DESIGN ANALYSIS

A. Complementary Pass Transistor Logic

Complementary pass-transistor logic (CPL) belongs to a logic family which includes certain designs for specific advantages. Thus for multiplexers and latches it is necessary to use CPL. Output is used to drive an inverter and non-inverted signal is generated by using series of transistors which enables to select required inverted outputs. The pass-transistor gates require both inverted as well as non-inverted inputs to drive the gates. It includes complementary inputs/outputs and NMOS pass-transistor logic network, CMOS output inverters. The inverters which are used here can be restored by PMOS latches. The threshold voltage which is less than the supply voltage is due to the high level of pass- transistor output nodes. Thus PMOS latches pulls up the output loss. The significance of using PMOS latches come in to picture when maintaining high speed swinging becomes a challenge. Due to which there will be a huge spike in the power supply while it swings, this is a major drawback. Thus the voltage swing will be equal to V_{dd} which is the major drawback of this logic. Complementary output pass-transistor logic is used by CPL which performs evaluation of logic and checks the driving of the outputs by CMOS inverters. This design can include leakage current produced by the inverter in the absence of soft pull-up latch.

B. Double Pass Transistor Logic

Some of the inverter stages will be eliminated by using DPL. This is made possible by using both N and P channel in the transistors. The limited capacity which drives load is due to low input capacitance and high speed. Both NMOS and PMOS pass transistors consist of DPL gate with swinging tree. By adding PMOS in parallel with NMOS it is possible to achieve operation with full swing. This results in increasing of input capacitance. By using DPL the full swing output voltage is restored this is done by using the NMOS and PMOS combination instead of PMOS-latches and inverters. Even though it fulfills all the requirements of full adder it has a major drawback of consuming high area but it has high-area and power. Figure 2 shows full adder designed using DPL logic style.

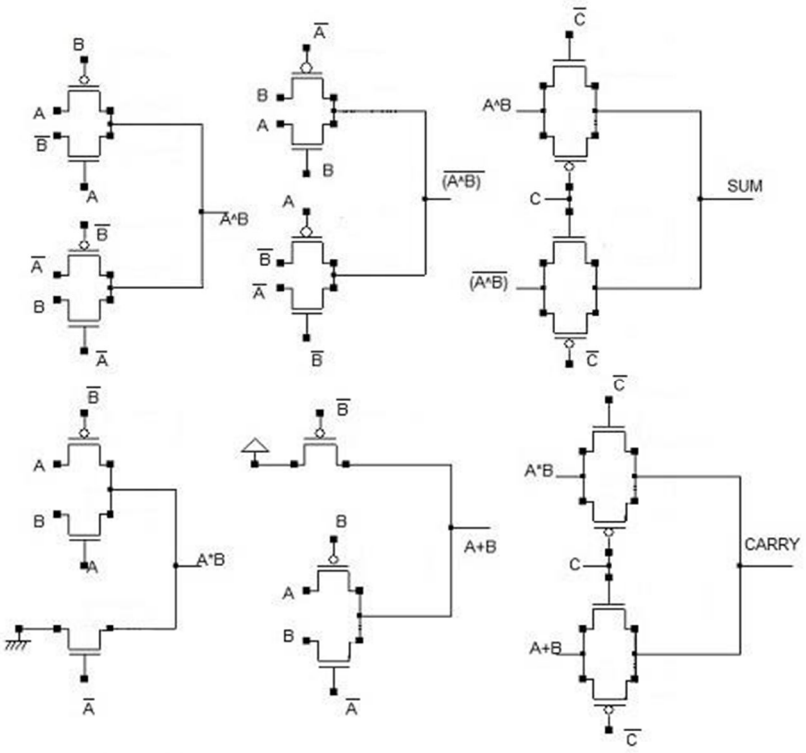


Figure 2: Full Adder Designed Using DPL Logic Style

In figure 2 the number of nodes are 18, number of NMOS are 14 and number of PMOS are 14. Therefore 28 MOSFETS are used for the full adder design using DPL.

C. Swing Restored Pass Transistor Logic

The CPL is used to derive Swing Restored Pass transistor logic (SRCPL) style. The swinging network uses the same NMOS pass-transistor. For recovering the output signal the swing restoration output inverters and latch structure are cross coupled. An advantage of SRCPL is its simple design, but a disadvantage is the spikes on power-supply that occur during swinging. Figure 3 shows full adder designed using SRCPL style.

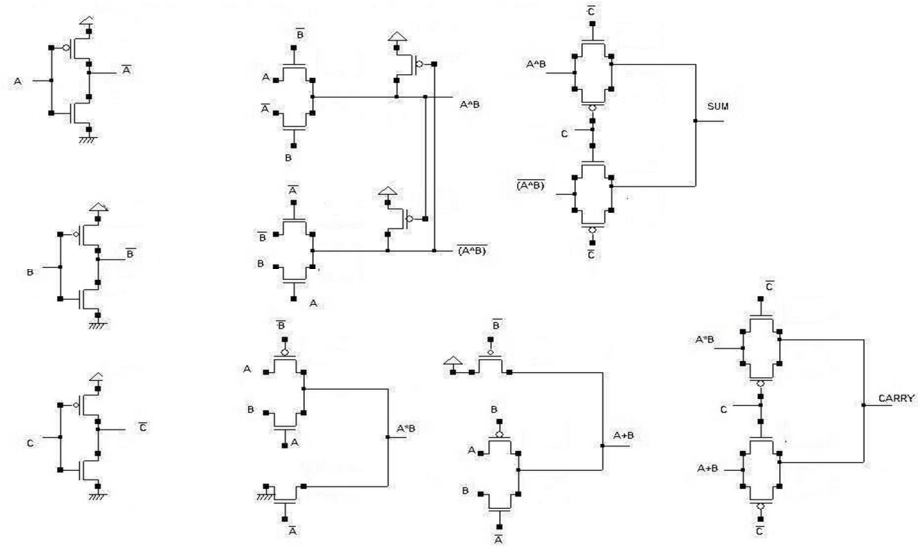


Figure 3: Full Adder Designed Using SRCPL Logic Style

In figure 3 the number of nodes are 14, number of NMOS are 14 and number of PMOS are 12. Therefore 26 MOSFETS are used for the full adder design using Swing restored pass transistor logic.

D. Proposed Circuit

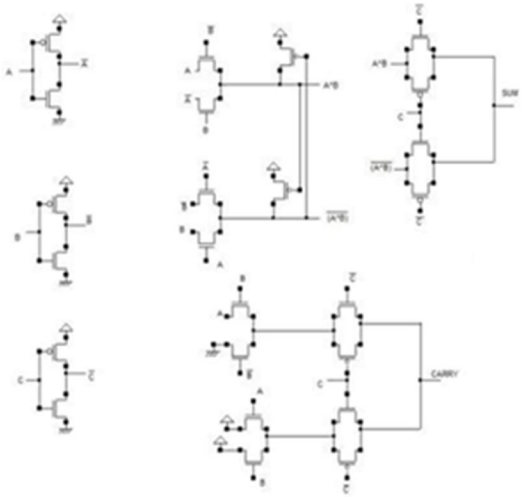


Figure 4: Proposed CMOS Full Adder Using Pass logic Transistors

With the proposed circuit number of p-mos and n-mos transistors will be 12 and 6 respectively. This in turn reduces the power consumption and area. Figure 4 shows the proposed circuit and logic respectively.

Table 1: Truth Table of FA (Proposed Logic)

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1(det)
1	1	1	1	1(det)

Table 1 shows the proposed full adder's truth table where in 'det' represents the deteriorated value.

III. DESIGN IMPLEMENTATION

The proposed design is been designed and tested using CADENCE Virtuoso designing tool.

A. Procedure For Implementation

The circuit for sum and carry is designed and tested separately. The simulated results were studied. Upon testing individually both the circuits are converted in to a working block or test cases. Later these working blocks were combined to form a single working block of a full adder. This block is simulated and the results were studied.

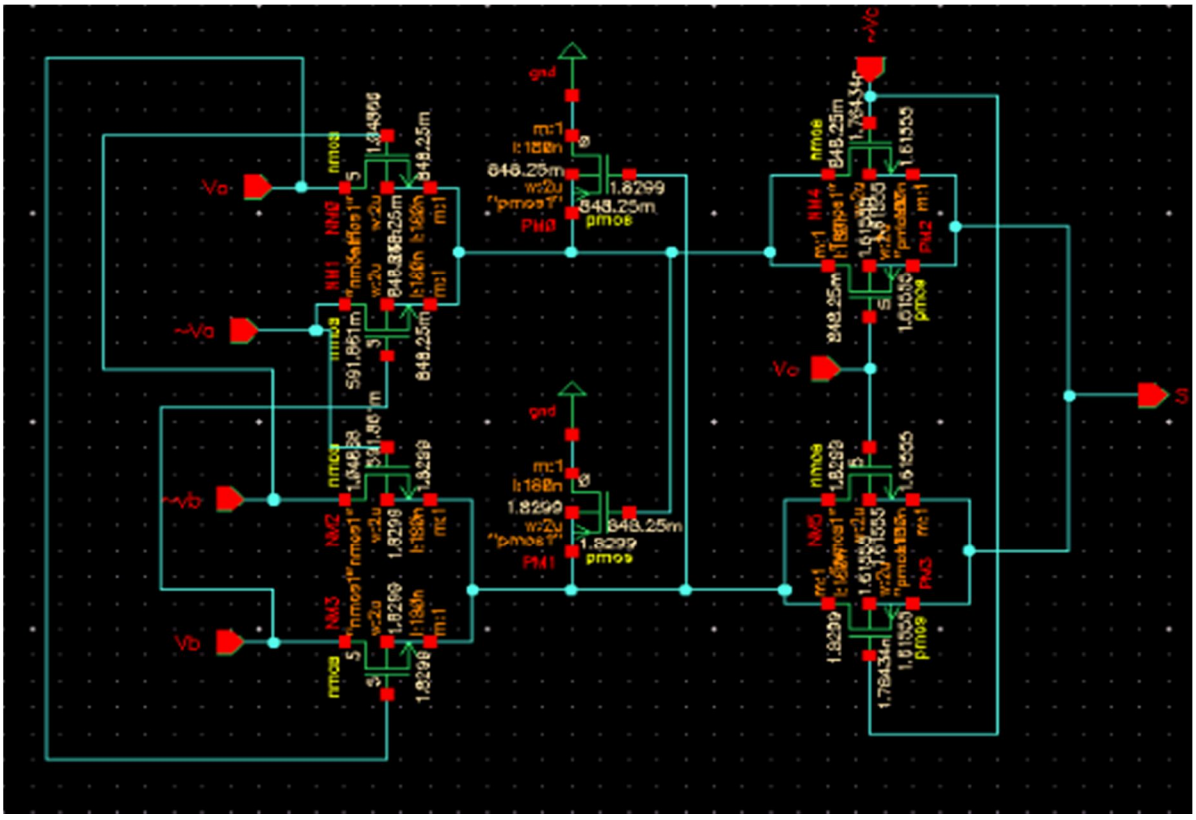


Figure 5: Implementation of Sum Circuit

Figure 5 shows the sum circuit which is been implemented in a tool. Where V_a, V_b and V_c are inputs fed to the circuit and S is a sum. PM1 and PM2 are pull up transistors which restores the deteriorated value.

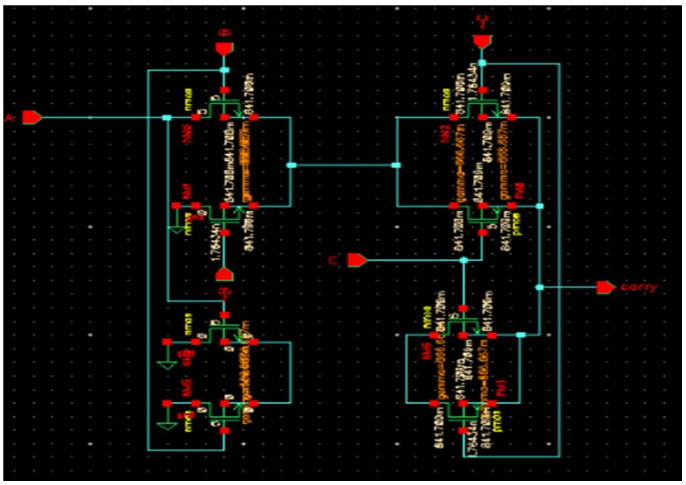


Figure 6: Circuit Implementation for Carry

The above figure 6 shows the implementation of carry circuit. Where A, B and C are inputs and carry is the output. The two blocks (SUM and CARRY) were combined to get a single block. And the result was studied.

IV. TESTING

C_{ds}, C_{gs}, C_{gd} and device temperature is obtained by testing the device or circuit. Figure 7 and 8 shows the device characteristics of Sum and CARRY respectively.

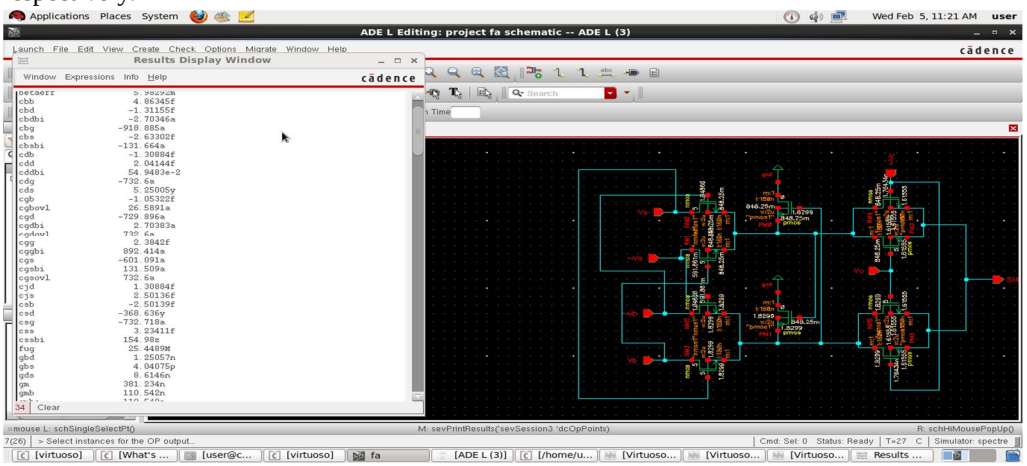


Figure 7: Device Characteristics of SUM

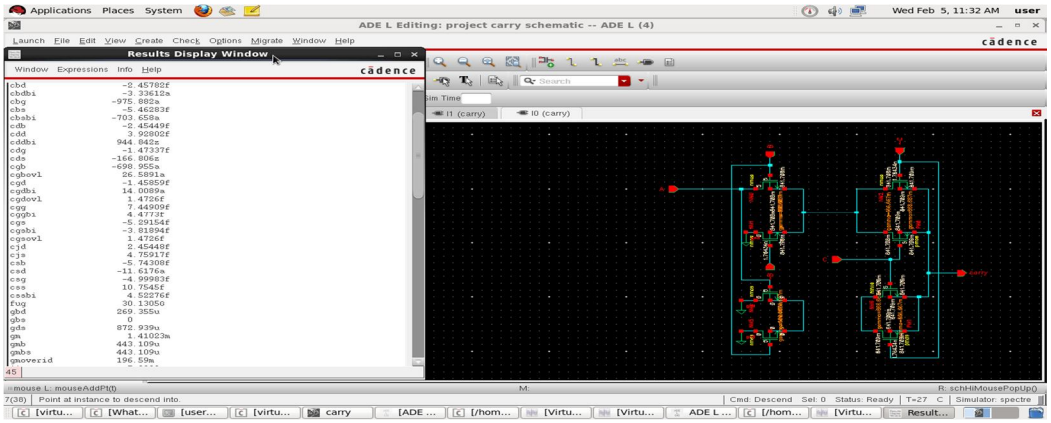


Figure 8: Device characteristics of CARRY

V. NOISE AND DELAY TESTING

Noise and delay are caused due to the presence of interconnections in the device this reduces the speed of the device. It can be reduced by using buffers in the design. Figures 9 and 10 show the noise and delay of the SUM and CARRY circuit.

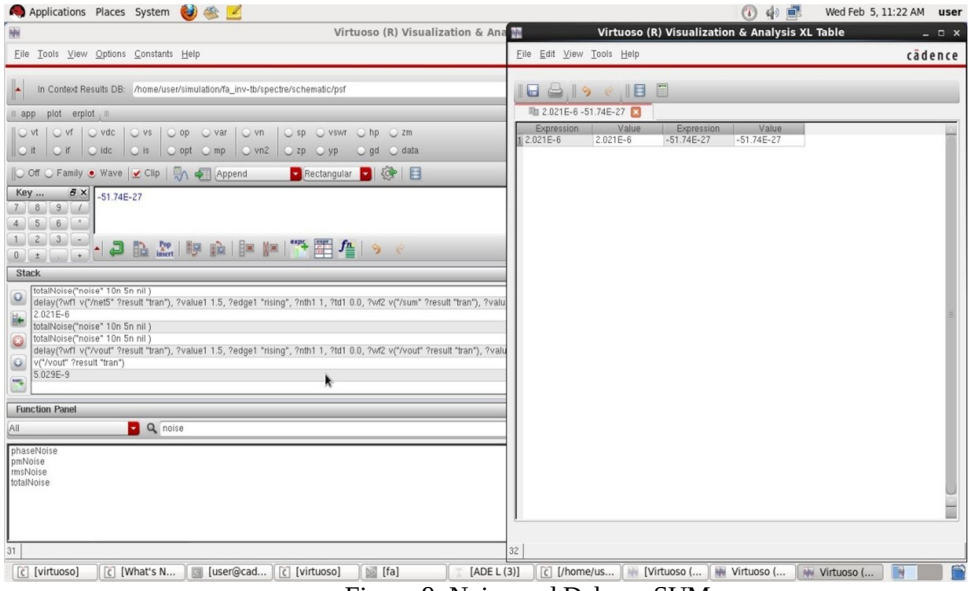


Figure 9: Noise and Delay – SUM

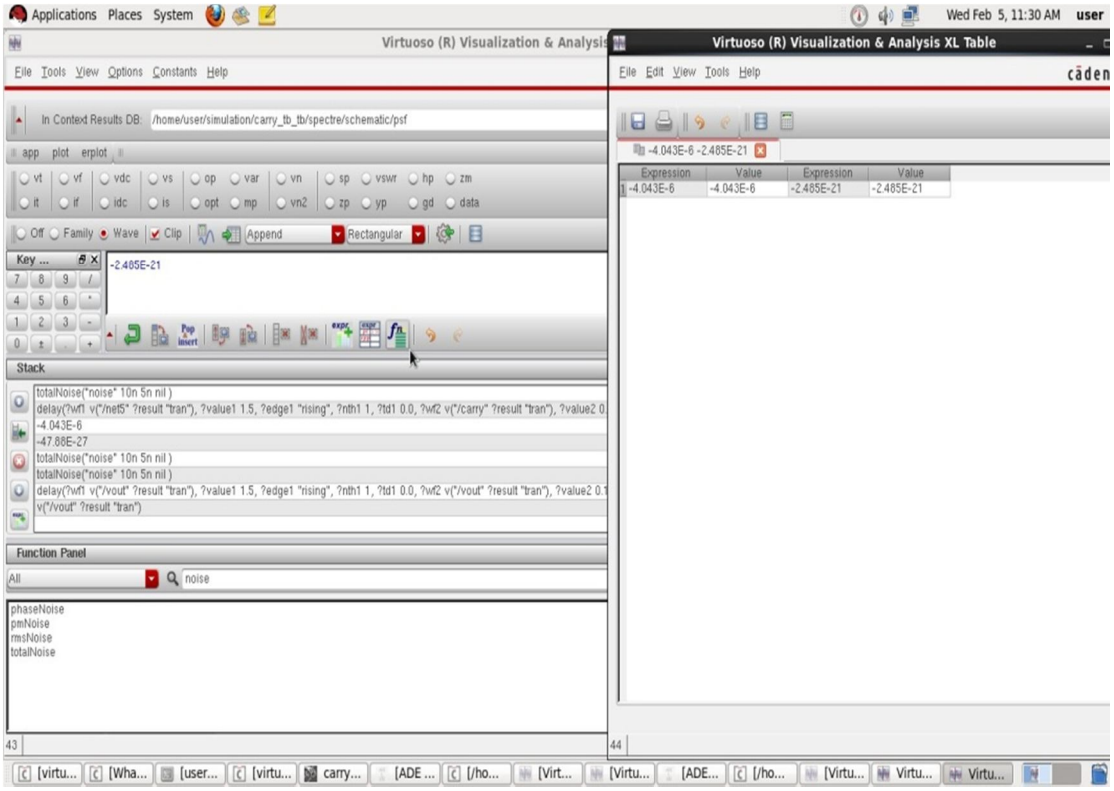


Figure 10: Noise and Delay - CARRY

Therefore the SUM and CARRY show delay of 2.021us and 4.043us respectively. Also the noise $-51.74*10^{-27}$ and $-2.485*10^{-21}$ respectively for SUM and CARRY.

VI. RESULTS AND DISCUSSIONS:

The result of the proposed work and description is based on snapshots taken by executing the implemented work. It describes the results that are tested.

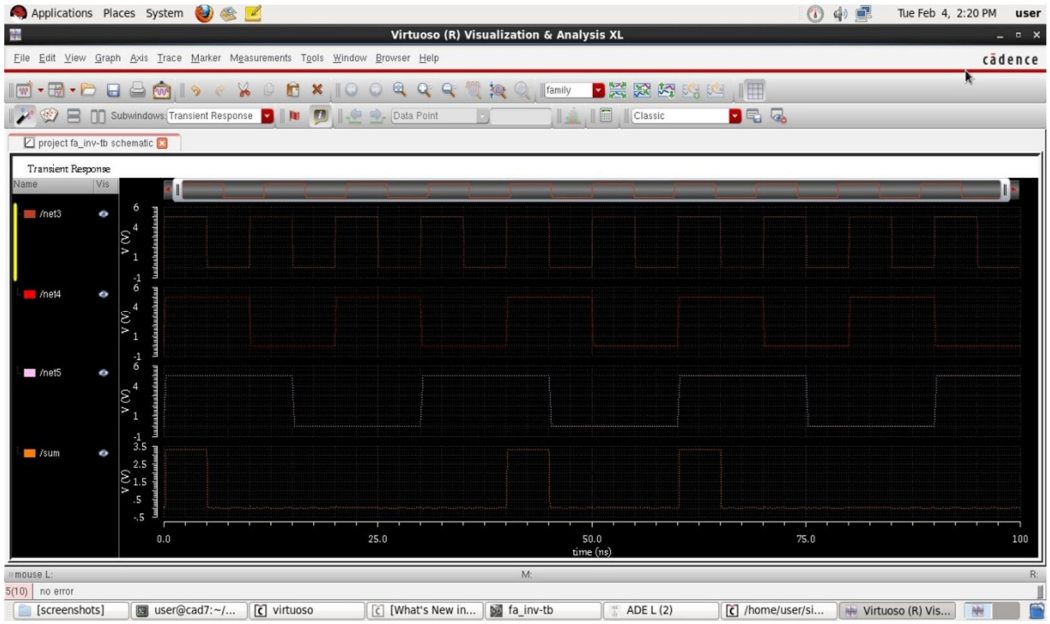


Figure 11: Output of SUM

Figure 11 shows the simulated result of 1 bit Sum. Clearly it shows the efficiency of design. The simulation does not contain any glitches or delay.

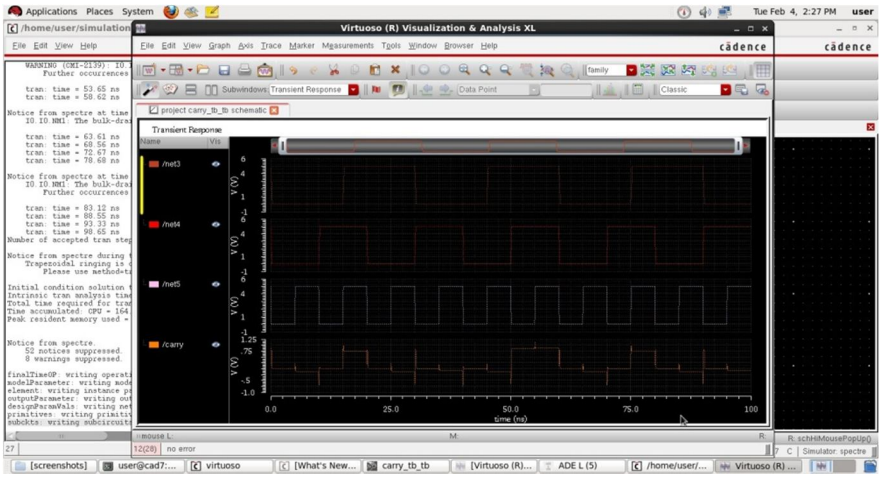


Figure 12: Output of CARRY

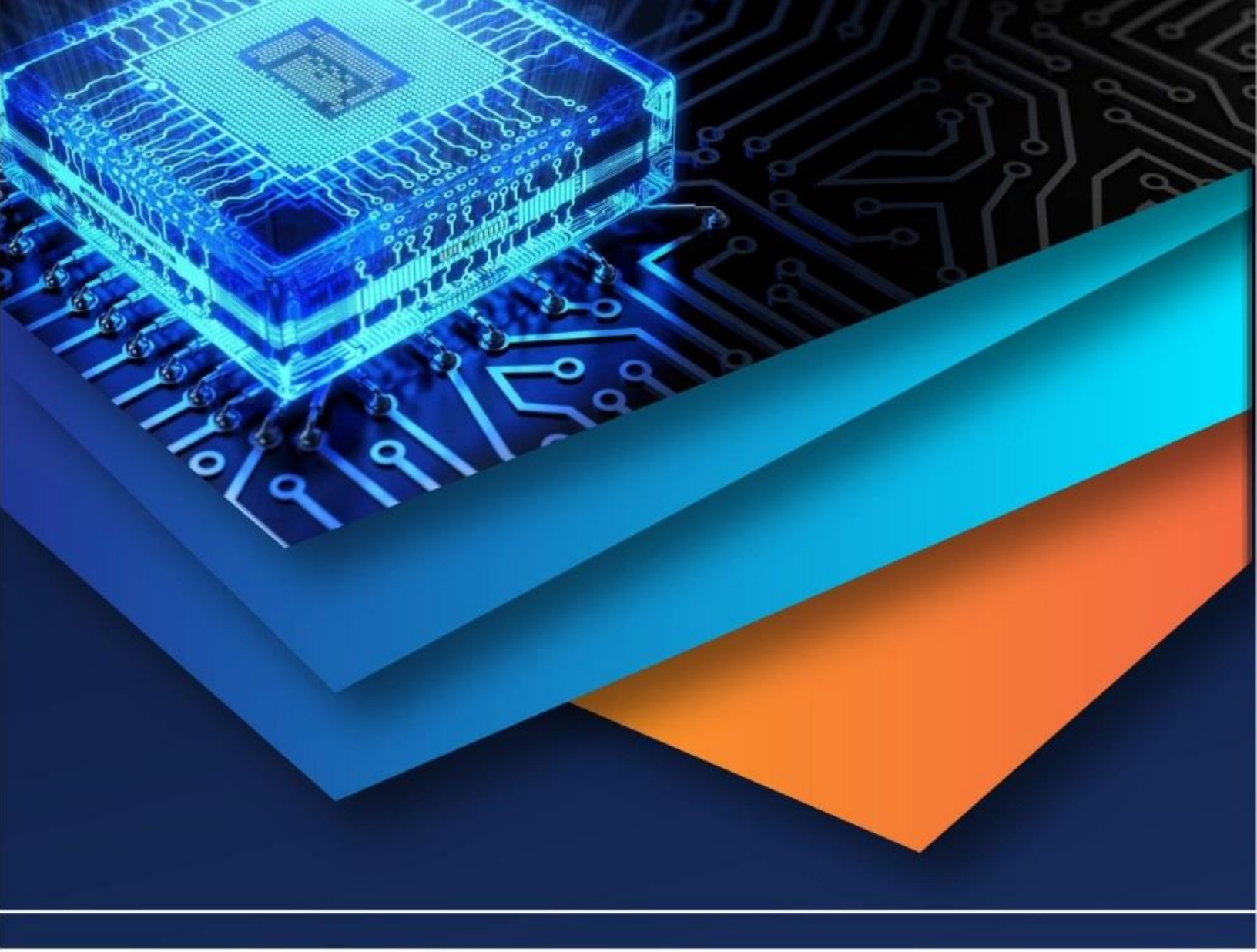
Figure 12 shows the output of 1 bit CARRY. It contains some glitches and delay due to the interconnections in the device.

VII. CONCLUSION

This paper presents the full adder design which uses PTL method. The design presented in this work aims in minimizing the area and power consumption of full adder. The design works in two stages and later combined to a single stage which gives the final full adder design. The proposed logic can be cascaded to derive the multiple stage full adder. In this proposed work CADENCE Virtuoso tool plays a very important role to achieve all the objectives. The logic used in this design helps the designer to achieve a module which needs less power and area.

REFERENCES

[1] Ahmed M. Shames, Tarek K. darwish and Magdy A. Bayoumi, "Performance Analysis of Low-Power 1-Bit CMOS Full Adder Cells", IEEE Trans. Very Large Scale Integr.(VLSI) Syst., vol.10, no.1, Feb.2002.
[2] Mariano, Aguirre and Monico Linares, "An Alternative Logic Approach to Implement High-Speed Low-Power Full Adder Cells." 2005 18th Symposium on Integrated Circuits and Systems Design. IEEE, 2005.
[3] Sundeepkumar Agarwal, pavankumar V K and Yokesh R, "Energy-Efficient, High Performance Circuits for Arithmetic Units", IEEE DOI 10.1109/VLSI.2008.49.
[4] Nan Zhuang and Haomin W U, "A New Design of the CMOS Full Adder", IEEE Journal of Solid-State Circuits, vol.27, no.5, May 1992.
[5] Reto Zimmermann and Wolfgang Fichtner, "Low-Power Logic Styles: CMOS Verses Pass-Transistor Logic", IEEE Journal of Solids-State Circuits, vol.32, no.7, Jul 1997.
[6] A. Shams, and M. Bayoumi, "Performance Evaluation of 1-bit CMOS Adder Cells", IEEE, 1999.
[7] Makoto Suzuki, Norio Ohkubo, Tohinobu Shinbo, Toshiaki Yamanaka, Akihiro Shimizu, Katsuro Sasaki and Yoshinobu Nakagome, "A 1.5-ns 32-b CMOS ALU in Double Pass- Transistor Logic".
[8] Eugene D Fabricius *Introduction to VLSI Design.* McGraw-Hill International Editions.



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