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Design and Test of T/R Chain for Beam Former Module

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Abstract: ***A compact Radar transmitter/Receiver using fully integrated chip ADAR1000 a 4 channel X, Ku frequency Bandwidth phased array beamformer and ADTR1107 front end IC, working in a frequency range from 8GHz to 16GHz has been developed. The wide modulation bandwidth enables better range resolution with the low power consumption of approximately 2.3W. The phased array beamforming ICs which are established allow cost-effective, upcoming generation system solutions for Satellite communication and radar applications. The presented radar system is satisfying the needs of several novel measuring tasks. A compensated measurement of 2.5 dB noise figure is achieved for the given frequency range by the inbuilt low noise Amplifier. Additionally 8×16 array beam former has been designed on the sandwich PCB and tested resulted has been noted. From the tested simulation results its noticeable that sustained return loss is less than -20 dB at certain range of frequencies, with isolation of more than -75dB between transmitter and receiver. The performance of the designed system is evaluated and considered as best compact designed radar with less lost compared to other radars in the present era.***
Keywords: beam forming, front end IC, transmitter/ receiver, Phased array, Radar

I. INTRODUCTION

The evolution shows the traces from these first transmitter/receiver modules between the expansion of the 1990s and 2000s GaAs MMIC based modules that power the systems of today to the evolving Gallium nitride and silicon based modules of upcoming (AESA) active electronically steerable antenna phased array radars. A Ku-band AESA antenna with a lesser cost former phased array beam, which is an integrated T / R 3D module. It assembles various multirole modules into an entire multilayer frame. The 3D T / R approach significantly increases device performance and reduces expense and size for implementation. Here, they used IC chips that are very compact compared to other technologies to use the discreet components to build the T/R board. This also increases accuracy, performance, noise, gain, and more advanced metric requirements. It is easy to see that more integrated ICs greatly reduce the antenna design challenges and, with more compactness, new semiconductor technology designs are required to make feasible solutions.[1] - [3]

In previous years, this front-end antenna solution each of the parts would have separated, possibly found on technology based on gallium arsenide. They are contained of a phase shifter to change the each antennas phase feature (which antenna is eventually steered), also a good attenuator capable of tapering the beam, and to transmit a signal a power amplifier has been used, and to receive a signal low-noise amplifier is used, and a from switches between transmit and receive. Each of these ICs are housed in a 5 mm / 5 mm package in previous implementations, or more proceeded solutions may provide an integrated one-channel monolithic Gallium Arsenic IC for this feature. Semiconductor technology has aided the recent proliferation of phased array antennas. The nodes which are advanced in Silicon Germanium BiCMOS,(silicon-on-insulator), and volumed CMOS combined digital circuitry to monitor the array steering, and also the RF signal path to accomplish the process, and the amplitude adjustment in one IC. Nowadays it is possible that multiple channel beamforming ICs can be achieved which adjust gain and phase in a channel of 4 configuration with upto 32 designed channels for designs of mm wave to reach multichannel beamforming ICs that fine-tune gain and phase in a four channel configuration with up to 32 designed channels for mm wave architecture. [4] - [6]

The feature, which can only be tooled through analog circuits and analog technique, can now be implemented by digital circuits and digital technique, examples like digital receiver, digital beam forming in phased array radar. This express improvement in digital technology has made the way to phased array radar digitisation. [7], [8] In this paper, the 8×16 transmitter / receiver chain was equipped with a lightweight, cost-effective IC, namely ADAR1000 X and Ku frequency band phased beam forming chip and ADTR1107 front end IC chip from analog devices. Compared with other T / R modules with 360 degree angle resolution and best isolation, the key benefit of the built module has best noise figure. The module is mounted on sandwich PCB and is managed and processed at a frequency of 8 to 16GHz by smart fusion M2S150TS-FCG11521 FPGA The 8×16 array built, all of which operate at the same frequency at a time. The IC's are interfaced with SPI busses, with the integration of Single Pole Double Push. The integrated T / R module includes a Phased-array antenna, combat radar, climate radar, communication channels, and an (EW) electronic-warfare and satellite communications systems as well.

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II. THEORY AND OPERATIONS

Below are details of each of the components used for designing. Each component has its own design with the desired frequency with its own features and all the components have their own Maximum Temperature Value for which it must be tested in that set of temperature if it exceeds it can damage the circuit.

A. Architecture Design

A representation of the transmitter/receiver module architecture for phased-array beam forming has been illustrated in figure1. In this case of Design, 8×16 array have been mounted on PCB, but as shown in figure 1 only 2×4 array setup is shown as it a wide array. Each array consist of one phased array beam former with four front end IC interfaced as a transmitter and receiver. Phased array beam former gives gain with 360º angular resolution and front end IC consisted with power amplifier and low noise amplifier. When it is in transmitter mode only power amplifier is on work and LNA is on off condition and vice versa. This gets switched on and off with SPDT switch, and all this operations are controlled by smart fusion FPGA. The details of each components are given below with their functional block diagram.

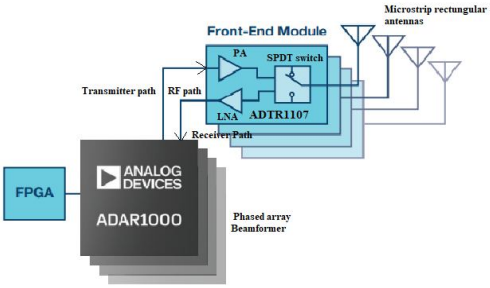

Figure 1: Interfacing of T/R chain on PCB layout

B. Phased-array Beamformer (ADAR1000) a 4-Channel, X, Ku frequency Bands.

The ADAR1000 is a four channel, a beamforming core chip for phased arrays with X and Ku frequency band. This component operates in half-duplexed between transmitter and receiver mode. In receiver mode, outgoing signals are transmitted through 4 receiving channels and combined into a common RF IO pin. In transmitter mode, through the four transmit channels, the RF_IO input signal is splitted and passed. In both modes, the ADAR1000 provides a full range phase adaptation of 360° in the radio frequency path and a ≥31 dB gain adjustment range, with a 6-bits resolution (lower than ≤0.5 dB and 2.8°, individually). A simple 4-wire serial port interface (SPI) controls all of the on-chip registers. Additionally, on the same serial lines, two address pins allow serial peripheral interface control of up to 4 devices. Resolute transmitter and receiver load pins also provide a solitary pin controls fast switching between the transmitter and receiver modes and synchronisation of all corebase chips in the same array. The ADAR1000 is available in a compact, it is specified from −40°Celsius to +85°Celsius, 88-terminal, and 7 mm × 7 mm, LGA package. Figure 2 shows the block diagram of the phased array beam former functions. The Range of Operating calefaction is −40 degree Celsius to +85 degree Celsius and room Temperature range is −65°Celsius to +150°Clesius. The performance of the ADAR1000 transmitter to receiver and receiver to transmitter functionality based on a control signal of transmit and receive input to the chip. Mode transition can be accomplished through either via the digital transmit and receive input pin of the chip or a SPI register write.

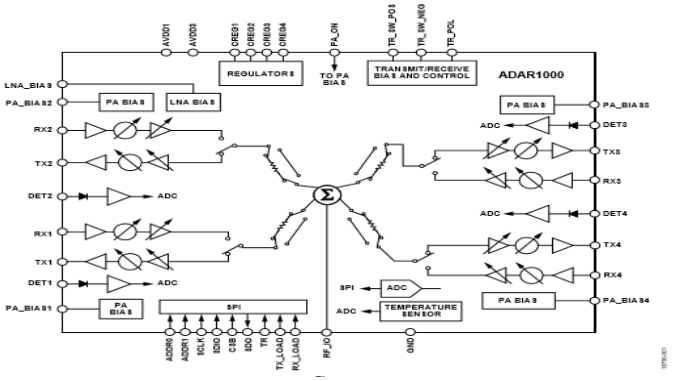

Figure 2: block diagram of ADAR1000 functions

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C. ADTR1107 Front-End IC

The ADTR1107 is a compact, front-end module with an integrated power amplifier (PA) works at the frequency range of 6 GHz to 18 GHz, a reflective single-pole double-throw (SPDT) switch and a low noise amplifier (LNA). For phased array antenna and radar applications these integrated features make the device ideal. The front-end IC offers small signalgain of 18 dB ,and noisefigure of 2.5 dB in receive state , small signal gain of 22 dB in transmit state and 25 dBm of saturated output power (PSAT). For power detection the device uses a directional coupler. The input/outputs (I/Os) are internally matched with 50 Ω. The ADTR1107 is a kit of 5 mm which is supplied through, 24-terminal and land grid array (LGA). The below figure 3 and 4 shows the functional block diagram the front end IC and each connection of the pins which has to made for ADAR1000.

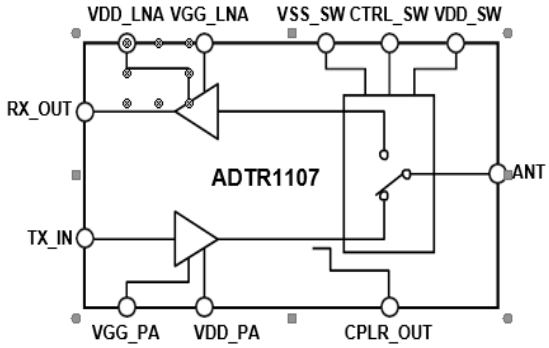

Figure 3: Functional block diagram of ADTR1107

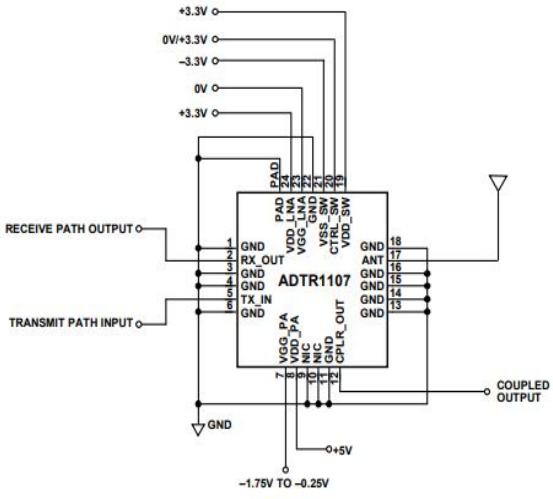

Figure 4: Typical Application Circuit

D. M2S150TS-FCG11521 FPGA

M2S150TS-FCG11521 FPGA is a system-on - chip (SoC) SmartFusion2 FPGAs that combines the fourth-generation flashbased FPGA fabric and highly performable communication interaction on a solitary chip. The SmartFusion2 family is the low power, very much reliable, and most stable programming logic solution in the industry. SmartFusion2 provides the gate solidity of up to 3.6X, the performance of preceding flash-based FPGA similar groups up to 2X, and encompass several memory blocks and multiplies DSP processing blocks. The 166 MHz ARM Cortex-M3 processor is intensified with an embedded trace macro cell , Memory Protection Unit , 8 Kbyte command cache, and supplementary peripherals considering a Control Area Network , Gigabit Ethernet, and highly speeded universal serial bus (USB). Highly speeded serial interaction include PCI EXPRESS (PCIe), 10 Gbps attachment unit interface plus native serialization / deserialization communication, while double data rate 2 memory controllers have high speed memory interfaces. Figure 5 below shows FPGA's smart fusion2 system-on - chip (SoC) development board diagram. Micro semi's flash-based FPGA fabric outcome in highly low power design implementation with static power on the M2S150 gadget as low as 10 mW.

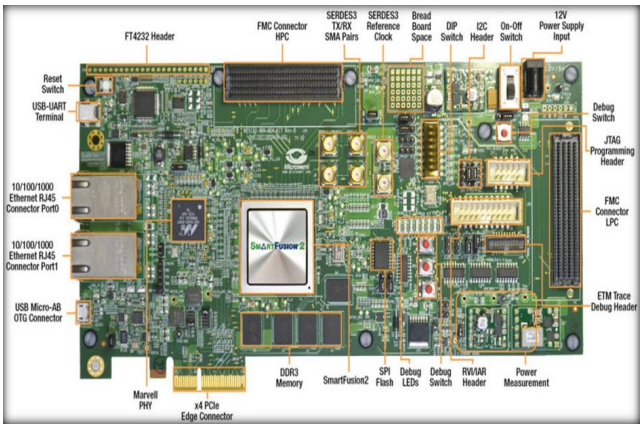

Figure 5: Development board diagram of Smart Fusion2 system-on-chip (SoC) FPGAs

III. DESIGNING OF T/R CHAIN AND RESULTS

The designed T/R module is illuminated on sandwich PCB with components of ADAR1000, ADTR1107 and smart fusion FPGA M2S150TS-FCG11521, and the designing of 8×16 array on PCB board has been shown. It's given that how the front end IC gets interfaced with a beamformer and the results of designed module has been shown. The system can be used for two purposes for observe the T/R module and for calibration of the T/R modules. Transmit and receive transfer functions of individual T / R module are achieved by inserting control signals with a network of control delivery and couplers at antenna ports of the T / R module. All channels share a similar control circuit for the RF signal, thus reducing the number of control schemes compared to other structures.

A. Interfacing of ADTR1107 and Phased-array Beamformer (ADAR1000)

As shown in Fig 6, ADTR1107 can be configured with the ADAR1000 X band and the Ku quad beamformer IC. Note that Figure 6 shows only a single device of the ADAR1000 and excluded additional components for clarification. The ADAR1000 supplies numerous bias voltages and control signals, making the ADTR1107 a flawless interface so no need for any additional control signalsADAR1000 PA BIAS3 pin provides the gate voltage for the ADTR1107 Power amplifier (VGG PA). For power amplifier gate heavily biased, one of four independent negative gate voltages is required. Instead every voltage is set by a Digital-to-Analog (DAC) 8-bit transformer with output voltage range from 0 V to −4.8 V. Typical gate voltage necessary to bias the power amplifier of ADTR1107 is −1.1V. The ADAR1000 TR input pin (rising edge allows the power amplifier) or a serial peripheral interface (SPI) write could assert this voltage. The ADAR1000 TR pin is used to swap the polarity of the ADAR1000 TR SW NEG pin and TR SW POS pin. The TR SW POS pin can drive up to four switches through the gates and can be used to regulate the ADTR1107 SPDT switch. While the voltage of the ADTR1107 LNA gate is self-based (the VGG LNA pin is attached to 0 V or grounded), the voltage can be controlled from the ADAR1000 also. Throughout this case, there is an 8-bit DAC regulated single LNA BIAS voltage (0 V to −4.8 V) that can be used to bias four ADTR1107 devices attached to each ADAR1000.

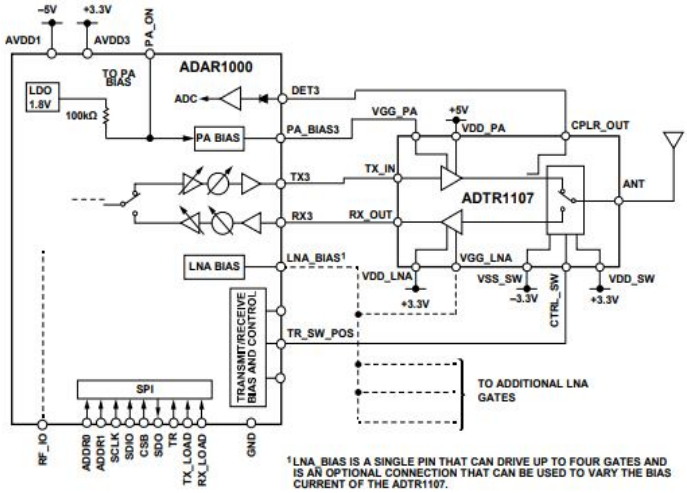

Figure 6*:* one channel Interfacing of ADTR1107 to ADAR1000

B. PCB Designing of Transmitter/receiver Module

ADAR1000-EVALZ is designed to determine the performance of the ADAR1000 4-channel, X-band, and Ku-band beamformer on radar systems as shown in Figure 7. Both input / output channels for radio frequency (RF) and detector inputs are carried out to Subminiature Version a (SMA) connectors. On-board logic level translators convert on-chip 1.8 V logic signals to 3.3 V for interfacing with external 3.3 V controllers. Two identical, 20-pin, dual row, rectangular headers provide digital interface signals to allow up to four ADAR1000-EVALZ boards to be linked together. A 24-pin connector provides interface power and bias outputs to four external transmitters and receivers modules each with ADAR1000-EVALZ. Figure 6 shows the ADAR1000-EVALZ, with 13 high frequency connectors for the four transmit outputs, four receiving inputs, four detector inputs and a common RF input and output. Four on-board banana jacks provide power supply connections and an SDP adapter board connector that interfaces with the USB on a Windows-based PC. Dual row, square pin headers allow connections to four transmit and receive modules, as well as the daisy chaining of up to four ADAR1000-EVALZ boards together. To configure the system the ADAR1000-EVALZ requires an SDP-S or SDP-B adapter board. The evaluation program ADAR1000-EVALZ and the examples provided in this user guide both make use of this SDP link.

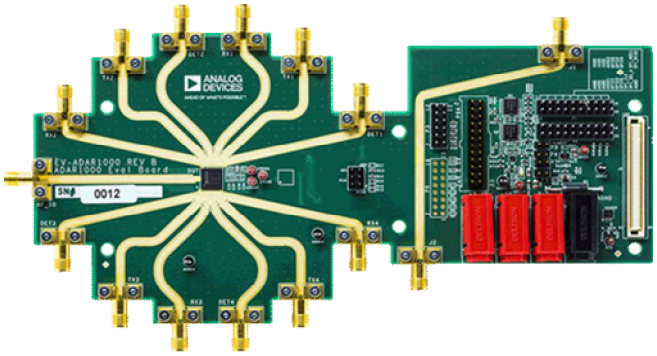

Figure 7: Evaluation BOARD of ADAR1000

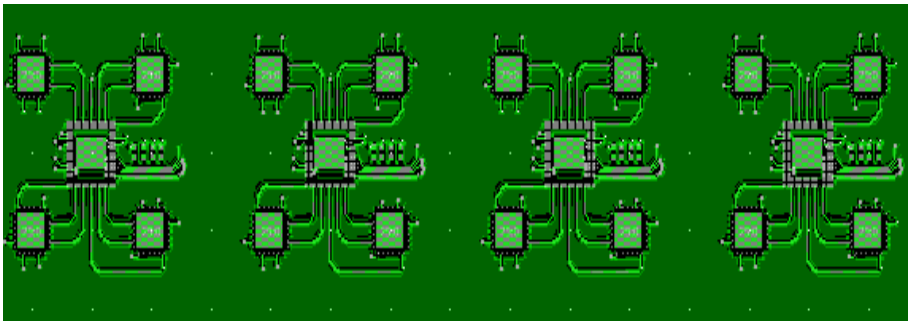

Figure 8: Top layer interfacing of ADAR1000 and ADTR1107 on PCB designer

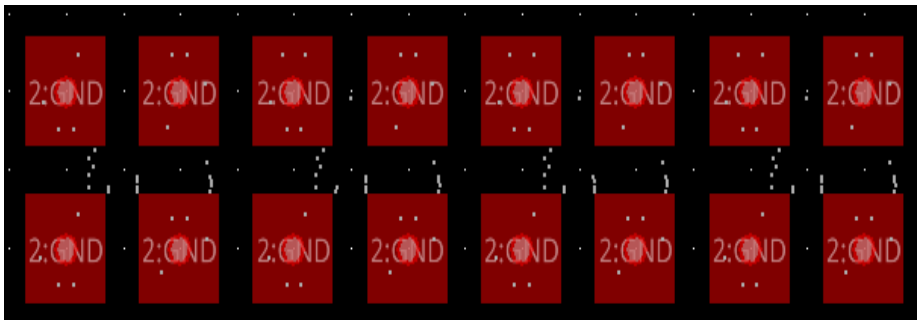

Figure 9: Bottom layer interfacing of ADAR1000 and ADTR1107 on PCB designer

The above figure 8 and 9 shows the top and bottom layer designed on PCB. As observed the figure has 4×1 array, but the design is of 8× 16 array that is 512 arrays have been placed and the tested value will be noted. Each array consist of 4 ADTR1107 front end IC interfaced with ADAR1000 beamformer.

C. Results and Simulation

T / R systems are vital components of the radar system, they require a considerable portion of the overall cost. Reducing the cost and size of a T / R module is therefore a major problem for the next generation installation of the phased-array. Considering all these in the scenario the chain has been designed with low cost with less noise figure and with good return loss and gain.

The designed T/R module consumes the total Power of 2.3W. The tested results has been given in the table 1 for two different voltage of 3.3V and 5V. The two voltage power are added and converted to watts.

Table 1: Power consumption tested

	3.3V	5V
RX	223mA	4mA
TX	345mA	4mA
Total power (W)	1.589	0.7559

Table 2 shows the tested value of the evaluations board of ADAR1000 and ADTR1107 when it works only in the transmitter state. According to the design the circuit work either in transmitter mode or receiver mode. When transmitter mode is on the receiver side switch to off condition, when it's in receiver mode the transmitter side switches off. The below table values has been tested and noted under the frequency range of 6GHz to 14 GHz.

Table 2: When T/R chain works in Transmitter state

FEATURES	TESTED VALUES
Frequency range	6GHz-14GHz
Saturated output power	0.31622 W
Small signal gain	21.5 dB
Gain flatness	±0.8 dB
I/O return loss	13 dB
Isolation Tx-Rx	-40 dB
Isolation Ant-Rx	-60dB
RF setting time	17ns
Switch speed rise to fall time	2ns
Turn on turn off time	10ns

Table 3 also shows the features and their tested values of the evaluation board of integrated chips. These values are tested for the 1 array and these values has been tested under the frequency range of 6 GHz to 14GHz as similar to the transmitter side.

Table 3: when T/R chain works in Receiver state

FEATURES	TESTED VALUES
Frequency range	6GHz-14GHz
Saturated output power	16dBm
Small signal gain	15.5 dB
Gain flatness	±0.6 dB
I/O return loss	13 dB
Isolation Ant-Tx	-32dB
Isolation Rx-Tx	-48dB
RF setting time	17ns
Switch speed rise to fall time	2ns
Turn on turn off time	10ns

Normally, radars need T / R solid state devices with high power output, low noise and adequate gain in both transmitter and receiver. As the cost of the T / R module is 40 to 60 percent of the costing of the antenna, it's important to use a design with a less number of IC chips that fulfil all requirements. Figure 10 shows the plot between noise figure and the certain frequency. Its shows from graph that from antenna to receiver output the noise figure has been noted as 2.5dB at +25º Celsius and nearly 2db at temperature of -40º Celsius. It's also shows in figure 11 that the return loss of the tested module has been less than -20 dB at the frequency range of 8GHz to 9.5GHz.

The isolation of the radars between transmitter and receiver is essentially significant, as the transmitting radar signals can be penetrated directly into the receiver in the event of a bad isolation.

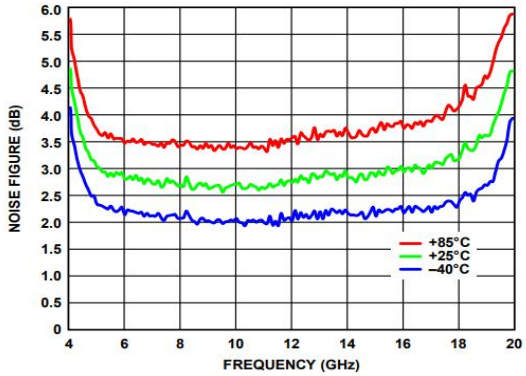

Figure 10: Noise Figure vs. Frequency

In the radar transceivers, a half-duplexer is also introduced to isolate the transmitter and the receiver when the same antenna is shared to transmitting and receiving signals. Here the Isolation between transmitters to receiver path is nearly-65dB at the temperature of -40º Celsius and -60dB at +25º Celsius which is compared to the normal room temperature in the give figure 12.

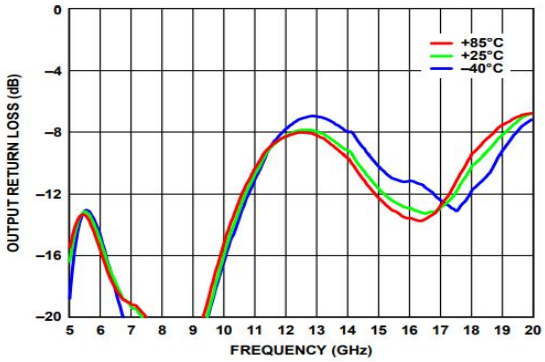

Figure 11: Output Return Loss vs. Frequency

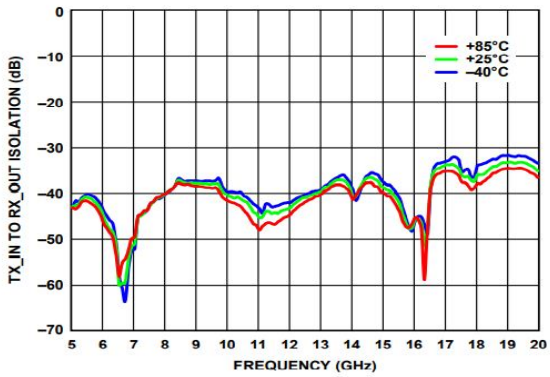

Figure 12: Isolation vs. Frequency, transmitter to receiver

The Isolation between Antennas to receiver path is nearly -85dB at +25º Celsius which is compared to the normal room temperature has shown in figure 13. The recommended IC chips Absolute Maximum Ratings needs to be considered as give in their tested values to achieve optimum performance while not damaging the device

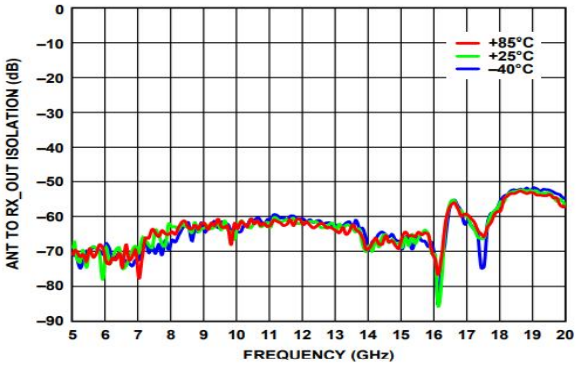

Figure 13. Isolation vs. Frequency ,antenna to receiver

IV. CONCLUSIONS

In several applications, existing technology permits the production of active phase-array radars. The cost and performance levels achieved for the module demonstrate the possibility of creating phased beam array developing the T / R chain. A fully integrated chip ADAR1000 a four channel X and Ku frequency Band phased array beamformer and ADTR1107 front end IC working in a frequency range from 8GHz to 16GHz, compact radar transmitter/Receiver has been developed. Additionally 8×16 array has been designed on the sandwich PCB and tested resulted has been noted. A compensated measurement of 2.5 dB noise figure is achieved for the given frequency range by the inbuilt low noise Amplifier. From the tested simulation results it's evident that received return loss is less than -20 dB at certain range of frequency, with isolation of more than -75dB between transmitter and receiver. The performance of the designed system is evaluated and considered as best compact designed radar with less lost compared to other radars in the present era with the applications of Phased-array antenna, Military radar, Weather radar, Communication links,(EW) Electronic warfare and many more.

V. ACKNOWLEDGMENT

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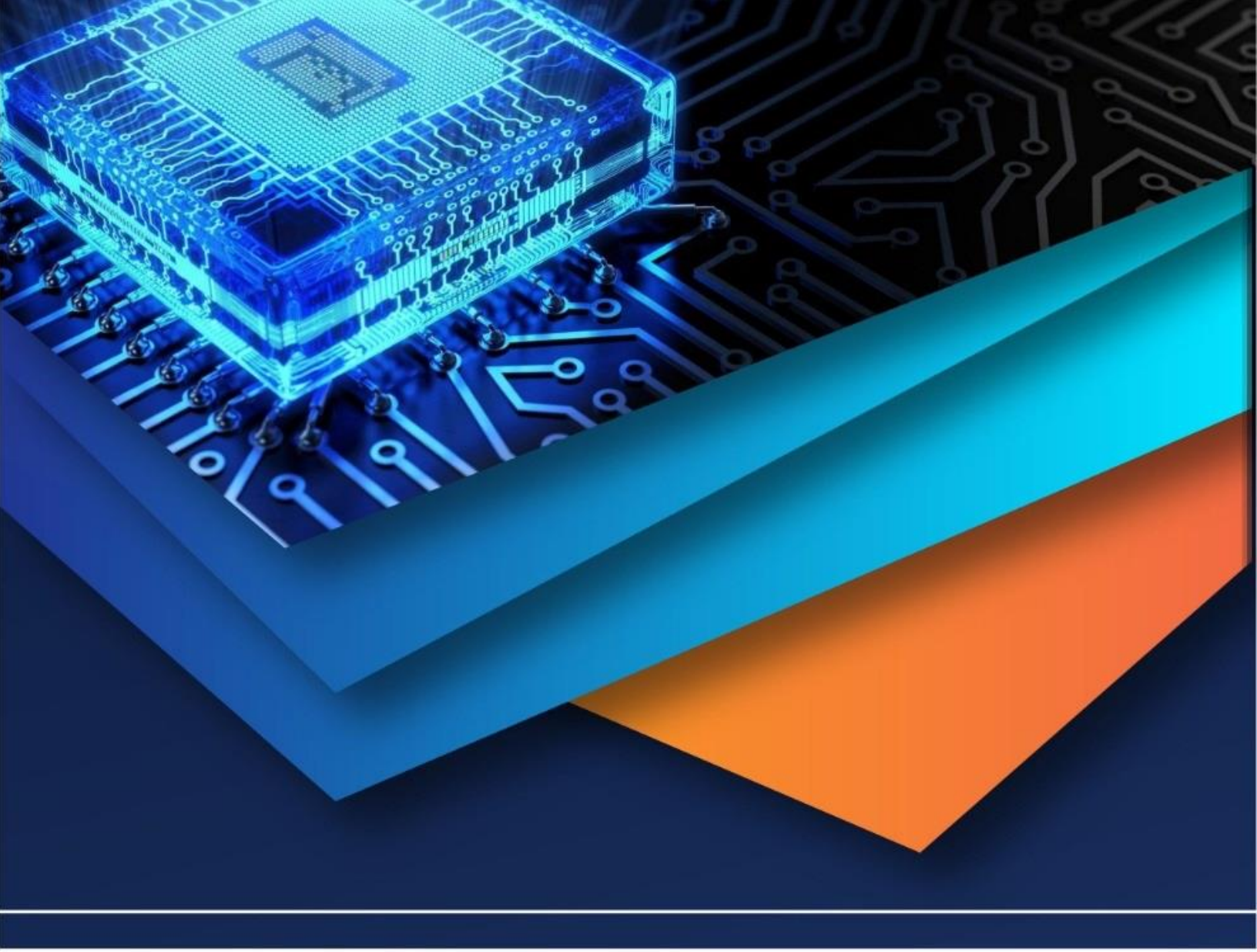

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