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Power Optimization Techniques Adopted at various Abstraction Levels in System on Chip Design - A Survey

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Abstract: ***To meet the requirements of consumers the portable electronic devices are embedded with advanced integrated System on Chip (SoC) Circuits. The complex SoC's are power hungry and needs power optimization at various levels of the chip design. Based on the observation of the power consumption, the optimization has become a real issue, and may also be the limiting factor of future growth. This paper provides the details of different types of power dissipation and their major causes. Further, the paper focus on the different aspects in which power can be optimized. The beginner gets an idea during the design flow what are the causes of power consumption and at which level of abstraction need to be concentrated to reduce power. It also provides advantage and disadvantages associated with power optimization. And summary describes which abstraction levels results in how much power savings and error percentage.***

Keywords: Power consumption, optimization, dissipation, abstraction levels, power savings

I. INTRODUCTION

Energy efficiency is a critical feature of modern electronic systems because of the desirability of portable devices, the need for reliability and performance, the need to extend battery life, the need to minimize package costs etc. With the growing trends in technology, complexity is also increasing which led to a high-power consumption. Two opposing constraints in VLSI architecture are limited area and high performance. The tasks of the Integrated Circuit (IC) designer was involved in the trading of those constraints. There are several technical factors, because of which the power optimization has become important. The Moore's theory illustrates that the number of chips in a device doubles every eighteen to twenty-four months due to which the cost of transistor per chip is also increasing and further which results in cost of maintenance. Therefore, observing all this trends, power optimization has become a major cause for concern in all the design and architecture levels. In general, if the power optimization is done at the design and architecture levels then the power savings will be increased. Figure -1 clearly shows how the transistor size is decreasing with the year passing [1].

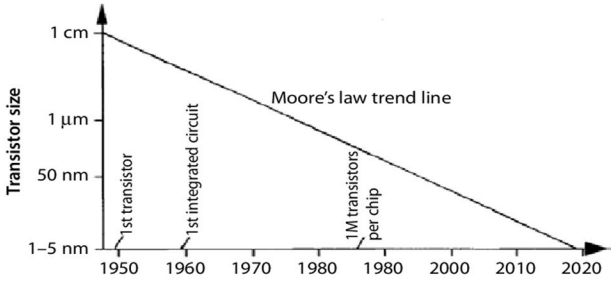

Figure1:Moore's Theory-Transistor Size versus year

II. NEED FOR POWER OPTIMIZATION

With the advent of technology in Soc design, power consumption has become a challenge in modern days. As almost all portable devices run on battery power. When technology continues to reduce its complexity, power problems are getting more and more complicated. Thus, designers are required to choose suitable techniques that meet application and product requirements. The increase in power dissipation is due to the increase in temperature which further can be a cause for a breakdown in certain devices, this results in extra cost for repairing it. Thus, VLSI Designers are considering power as a major cause for design failures in various abstraction levels. Therefore, power optimization in every field of technology has become an extreme cause for concern.

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III. TYPES OF POWER DISSIPATION

The average power [3] consumed in a device has been categorized into three types and equation-1 is used to calculate the average power.

$P_{avg} = P_{dynamic} + P_{static} + P_{short\ circuit}$ …… (1)

where,

P_{avg}- Average power dissipation

$P_{dynamic}$ - Dynamic power dissipation

$P_{short\ circuit}$ -Short circuit power dissipation

A. Dynamic Power

Dynamic power is defined as whenever the signal in the circuit's changes, those changes cause some dissipation of power. This can be observed in figure -2, when pullup transistor is on, the capacitor C_L charges to V_{DD} and when pulldown transistor is on, capacitor C_L discharges to ground. Thus, changes in the signal when the capacitor charges and discharges is the result of dynamic power dissipation. Dynamic power dissipation [3] is given by the formula shown in equation 2.

$$P_{dynamic} = \alpha C_l V_{dd}^2 f \quad (2)$$

Where α is known as the switching activity factor, C_L is known as load capacitance, V_{dd} is the supply voltage, f is the clock frequency.

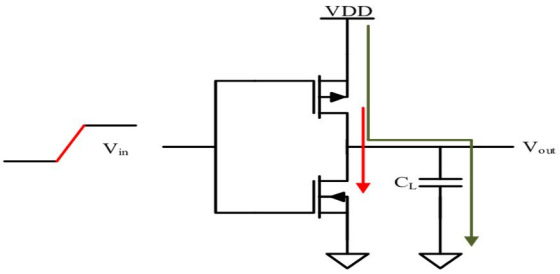

Figure 2: Dynamic power dissipation when capacitor $C_L$charges through V_{dd} and discharges through ground [13]

B. Short circuit power

During signal transitions, short circuit current occurs in a CMOS gate when both the pull-up transistor and pull-down transistor are ON, which results in a direct connection between Vdd and GND. This short circuit power can reflect more than 20 per cent of the total dissipation of electricity. It also applies to switching frequencies. As the frequency of the clock increases, the transition frequency increases. Figure -3 shows the pathway for the short circuit power. The expression for static power dissipation [3] is given by:

$P_{static} = I_{sd} V_{dd}$ ----------(3)

where I_{sd} is the short circuit current path, V_{dd} is the supply voltage.

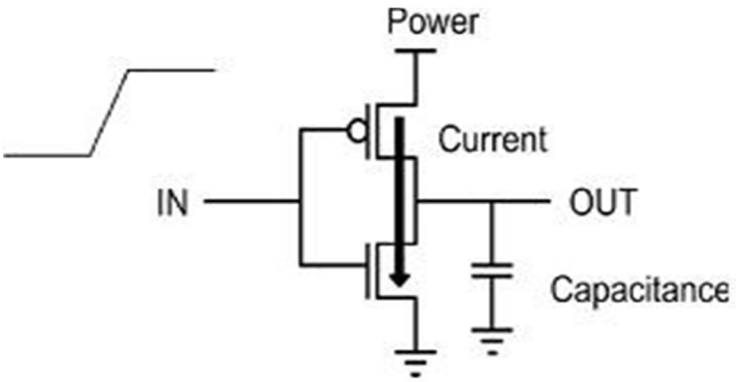

Figure 3: Short circuit path from V_{dd} to ground in short circuit power dissipation. [13]

C. Static Power

Static power is something which is dissipated even when no signal transitions are occurring. These mainly occur due to leakage effects, so even if the transistors are off(non-conducting), small amount of current continues to flow due to which leakage power will always be there and cannot be avoided, but it can be reduced by using some techniques. The expression for the static power dissipation [3] is given by:

$$P_{static} = I_{leakage} . V_{dd} \quad (4)$$

where $I_{leakage}$ is the leakage current path in static power dissipation and V_{dd} is the supply voltage.

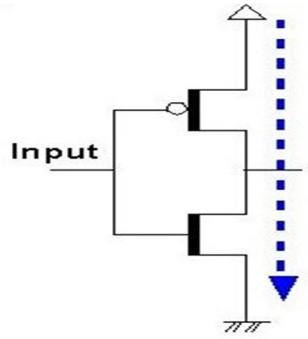

Figure 4: Leakage current in static power dissipation [15]

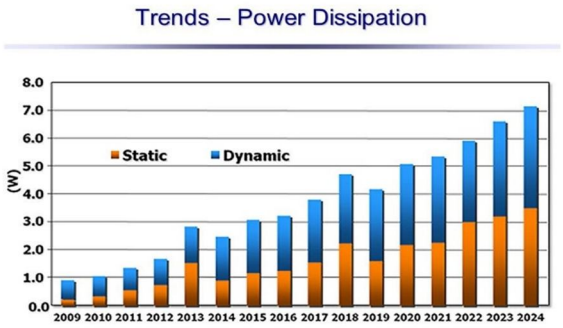

Figure 5: Power Dissipation Trends over years [16]

IV. ABSTRACTION LEVELS IN SOC DESIGN

Power optimization is achieved at various levels of abstraction. The block diagram illustrates the different abstraction levels and in each of these there should be power optimization. Further in the paper a detailed description of power optimization at different abstraction levels have been discussed. The figure (6) shows the power savings in each of the abstract levels. The system, algorithm and architecture levels are considered to be the high level synthesis and therefore, it is necessary to optimize power at these early stages of design because they have high power saving potential due to which a huge amount of power dissipation can be minimized.

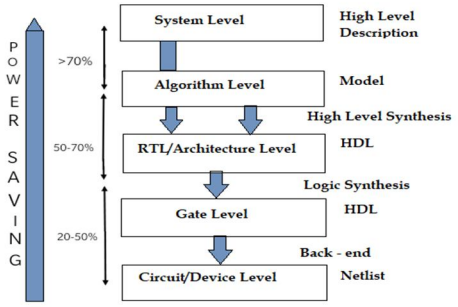

Figure 6: Abstract Levels with power saving capability

V. POWER OPTIMIZATION TECHNIQUES

Power optimization techniques at various levels are

A. *System Level*

System level is also known as the high-level description model. In this abstraction level, various factors are taken care off such as the formation of the design process and chip size. The results obtained after this level are the approximate values in size, power, speed and various functions needed for further design process. Techniques used for system level power optimization are:

1) *Adaptive Voltage Scaling:* Adaptive Voltage Scaling is a type of closed loop dynamic power minimization technique. It is used to vary the voltage supply to a memory chip to suit the power requirements of the chip during its operation. AVS function is to provide voltage supplied to the chip due to which its power consumption changes continuously to match the workload and the different chip parameters. The main advantage of AVS is that it directly adapts the voltage that is present on the chip and this makes it useful in real-time applications as well as chip to chip fluctuations that arises as the chip grows old. AVS saves about 55% of the dynamic power dissipation as compared to dynamic voltage scaling.

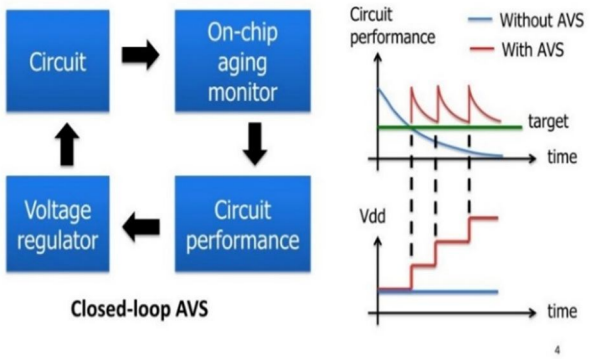

Figure 7: AVS Block diagram with waveform [14]

In AVS the on-chip conditions are measured, and the target and voltage frequency are calculated. By using Adaptive voltage scaling technique, we can reduce the power dissipation to a great extent. Figure (7) shows the process of AVS technique with waveforms.

2) *Loop Unrolling Technique:* Loop unrolling is a well-known method for enhancing system efficiency on average cases. This strategy consists of simulating the loop body for a certain couple of iterations in order to minimize branch and jump overhead and to reduce the amount of increment / decrement operations, providing additional code if necessary, to validate exiting corner cases. Certain programs are there in which instructions are needed for incrementing a pointer or a index to a certain value. When an optimizing programmer or assembler can pre-calculate offsets for each independently named array vector, these may be explicitly inserted into the machine code instructions, thereby having no extra arithmetic operations at program execution. In table 1 we can observe that how the code changes when loop unrolling technique is applied to it.

Table 1: Example for Loop Unrolling

Normal Loop	Loop After Unrolling

int x;
for (x=0; x<100; x++)
{
delete(x);
}
	int x;
	for (x=0; x<100; x++)
	{
	delete(x);
	delete(x+1);
	delete(x+2);
	delete(x+3);
	delete(x+4);
	}

Therefore, the table 2 below shows that the number of clock cycles decreases as the loop enrolling technique for low power is applied. By this technique, a lot of energy is saved resulting in the power optimization to a great extent.

Table 2: Decrease in number of clock cycles and the improvement with loop unrolling [9]

Application	# of Clock Cycles		Improvement / (%)
	No Loop Unrolling	With Loop Unrolling	
Bubble Sort	8,498	6,886	18.96
Bit String	278,755	215,810	22.58
Bit Count	199,700	172,550	13.60
Bit Shifter	525,650	368,855	29.83
Encryption	18,573	16,952	8.73
CRC32	2,560,026	1,792,030	30.00

B. Algorithm Level

In system level power consumption, the algorithm can have direct or indirect influence on it. The direct impact on power includes issues such as complexities in an algorithm and the counting operations whereas the other issues like concurrency in the computations have indirect impact on it.

Both the low power algorithms and the algorithms that can be driven towards low power are discussed here.

1) *Low Power Algorithms:* At algorithm level, there are three major factors that leads to or we can say affects power consumption directly includes the algorithm complexity, regularity and its precision.

a) *Complexity*: There are several ways to measure the complexity of an algorithm and one such type of measure is the counting operation. As each operation during execution consumes enough power, which becomes helpful for us to keep a track on the quality of algorithms for low power. Another important such measure includes the size requirement for an algorithm storage and the number of accesses for accessing the data. Therefore, algorithms that minimize operation count as well as access to memory and size for storage requirements are more frequently used for implementation of low power devices.

b) *Regularity*: The regularity of an algorithm affects complexity as well as power consumed by the control hardware device and by its interconnection network. Regular algorithms tend to have regular communication pattern and thus makes the use of interconnect networks efficiently, since same network can be used repeatedly many times for different parts of the algorithm.

c) *Precision:* To satisfy the precision requirements of an algorithm, the system architecture must have to have a sufficiently large word length. Even the algorithms that performs same function also have different word length requirements varying from algorithm to algorithm. As word length affects the power and performance, so, when selecting an algorithm for low power, the precision required to implement that algorithm should be considered.

2) *Algorithms for Low Power Architectures:* In this section, how an algorithm maps onto the architecture for low power is discussed. Two important methods for low power architecture includes concurrency and locality or modularity.

a) *Concurrency*: This processing method is used for power reduction by increasing the performance for lower voltage operation and, hence its power. If the algorithm has not enough concurrency while executing on the architecture, this strategy is useless. Algorithmic transformations can also help in increasing the concurrency in an algorithm. It includes pipelining, timing reoccurrence, expression replication, and algebraic conversions.

b) *Modularity*: This is other important method for low power architecture is to reduce its locality or modularity through control devices, hardware processors and memories. An efficiently working distributed processing structure can be obtained by increasing the algorithm modularity. Exploiting the locality of the architecture should be according to its modular algorithm to obtain low power architecture.

C. Architecture Level

The impact of low power techniques can be found to be more significant at the architecture level (high level) as compared to the gate level (low level). Architecture is also called as the register transfer level (RTL) of abstraction, including the blocks like adders, flops, memories, and controllers. There are techniques that can be used for avoiding waste and area as well as performance for power at this level. Basically, these techniques include concurrent processing, partitioning, power management etc.

1) *Concurrent Processing*: It is the most important technique used for reducing the power consumption as it directly affects the area and performance for power. Some important concurrent techniques for improving power performance are parallelism, pipelining, and partitioning.

a) *Pipelining*: Pipelining is a concurrent processing technique that can be used to reduce power consumption. A pipelining example is shown in figure 8.

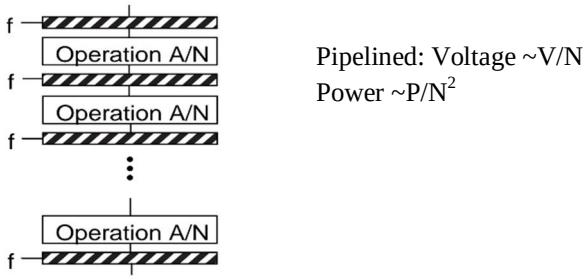

Figure 8: Pipelining for low power [19]

In this situation, pipeline registers are placed in structure to achieve concurrency, which results in forming a N stage pipelined structure of processor (say A). For maintaining throughput, it requires to sustain clocking frequency and ignoring the overhead of pipelined register, capacitance also remains constant. The computational requirements between pipeline registers are reduced. Instead of performing overall computation, within one clock cycle, it calculates for every clock cycle. This will reduce the supply voltage and thus, also reduces the dynamic power consumption. It also has some demerits as it incurs power and area overhead. But the area overhead incurs in pipelining is less than that of the parallelism.

b) *Partitioning*: For low power design locality must be present. Partitioning is one such method that helps in increasing locality. To reduce power consumption, consider the partitioning of processors and memory. As distributed processing method while operating has more efficiency of power saving as compared with a single processor. As in a processor, distributed memories are more power efficient than the one in shared. In general, total amount of power that has been consumed for memory access directly depends upon the total amount of data stored in that memory. If this total amount is reduced by partitioning/dividing the memory, then the power requirement will also be reduced for memory access.

D. Gate Level

Gate Level power optimization is much easier task because in this level of abstraction the design has been broken down to predefined gates and logic for which there are accurate libraries. Gate-level is much closer to the final chip than the RTL-level and therefore the power estimation is more accurate. At the gate level, the power consumption is also presented in more detail, per gate and not per larger block, as in the RTL-level estimation of power. Some of the techniques used at the gate level for power optimization are:

1) *Clock Gating*: Clock Gating is a widely used and relatively simple method for effective reduction of dynamic power. This technique is used to reduce power dissipation in the domain through clock pulse blockage. It is hierarchically implemented to improve the flexibility to control the power consumption during functional operation. The figures below depict how clock gating technique works. In the figure 10, glitches that are present due to the unpredictable behaviour of the enable signal which can further cause some problem. So to get rid of these glitches, clock gating with a latch is implemented due to which gclk signal is synchronous and therefore the previous glitches do not appear and this can be observed in figure 11.

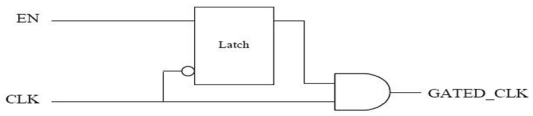

Figure 9: Clock gating circuit with a latch [21]

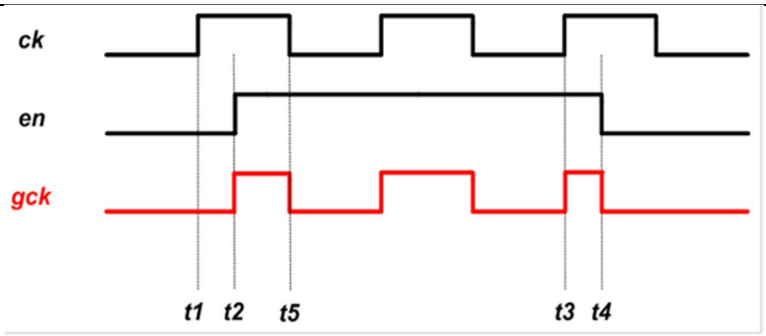

Figure 10: Output waveform without a latch [11]

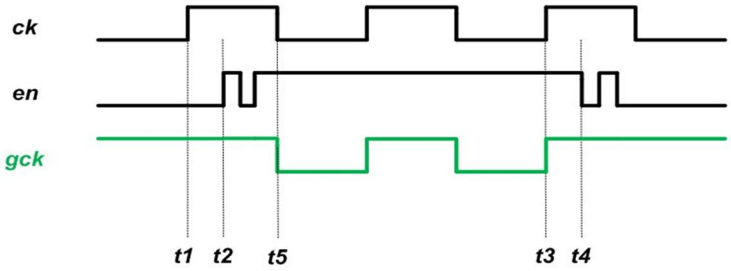

Figure 11: Output waveform with a latch [11]

2) *Power Gating*: Dynamic power has been the main concern of design engineers over the last few decades due to the fastening of the system clock and frequency. But in the future, VLSI 's power architecture predicts that static power will become a dominant component of the power architecture. Power gating is a technique that effectively mitigates leakage losses and becomes a major static power reduction technique.

Merits of Power Gating

a) Control gates are good for reducing leakage capacity. It is a strategy in which circuit blocks that are not in service are momentarily switched off to reduce the total leakage of the chip.

b) The CMOS switches that supply power to the circuitry are controlled by the power gate controllers

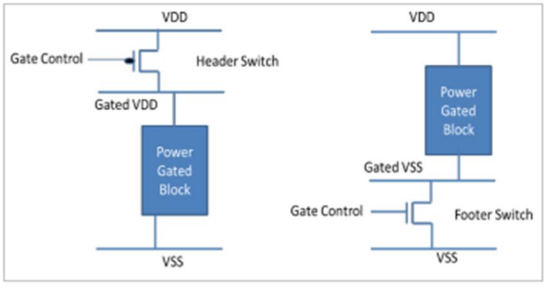

Figure 12: Power Gating circuit diagram [12]

E. Circuit Level

At the lower levels like circuit/device level, many techniques are available that helps in reducing the power consumption. Some of these optimization techniques are discussed here to reduce dynamic, static and short circuit power.

1) *Transistor Stacking Effect:* The transistor stacking is a technique used at the circuit level for leakage power reduction when used in active mode. The subthreshold leakage current decreases whenever two or more transistors in a stack is in off condition, this effect is known to be as stack effect. This leakage current decreases because of transistor stacking effect and increases source voltage that in-turn reduces subthreshold leakage current exponentially. Thus, a lot of leakage power is saved, by placing a greater number of transistors in the stack. A forced stacking can also be done by replacing the single transistor by two transistors of the width half that of single transistor to reduce power leakage. Figure-13 shows the stacking by force.

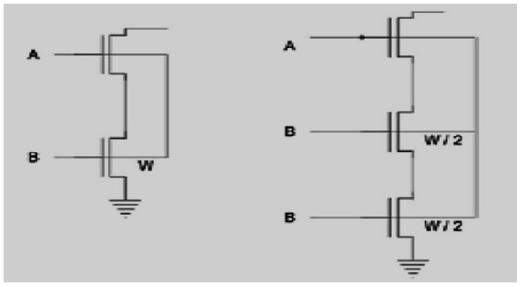

Figure 13: Forced stacking by using two transistors of half width (W=W/2 + W/2) [2]

2) *Dual Threshold CMOS (DTCMOS):* DTCMOS (CMOS dual threshold) has been shown to be an efficient way of minimizing consumption of leakage sub-thresholds. In this technique the gate and body of the transistors are connected such that the leakage doesn't occurs while the transistor is switched off. Thus, from the table below it can be observed that the DTCMOS is efficient in providing power saving of 98%.

Table 3: Power Saving Efficiency of different CMOS [8]

Technique	Power Saving	Delay	Area
MTCMOS	10%	4.6-8.4%	2%
VTCMOS	50%	25%	1%
DTCMOS	98%	44%	0

VI. ADVANTAGES AND DISADVANTAGES OF POWER OPTIMIZATION

The Table 4 brings out the comparison of the power savings, speed, and error percentage at various abstraction levels. Table 5 highlights the advantages and disadvantages associated with power optimisation techniques at various levels.

Table 4: Power Saving, Speed & Error rate at different levels [2]

Abstraction Levels	Power Savings	Speed	Error Percentage
System Level	>70%	Seconds	>50%
Algorithm Level	40-70%	Minute	25-50%
Architecture Level	25-40%	Minutes	15-30%
Gate Level	15-25%	Hour	10-20%
Circuit/Device Level	10-15%	Hours	5-10%

Table 5: Advantages & Disadvantages of power optimization

Optimization Techniques	Advantages	Disadvantages
Adaptive Voltage Scaling	Efficient in power saving, Better performance than DVFS.	Speed is effected.
Loop Unrolling	Program efficiency increases, reduces loop overhead.	If program size increases , it can cause increase in instruction cache.
Concurrency	Helps in avoiding inconsistent data.	Unless algorithm has enough concurrency ,this method is useless.
Modularity	Reduced costs ,high quality assembly and fabrication	Excessive/Poor modularity results in code which is difficult to read.
Pipelining	Instruction Throughput is increased.	Pipelining is not suitable for all kinds of instructions, design is complex.
Partitioning	Increase locality for low power design.	Incurrs area overhead.
Clock Gating	Reduces the switching frequency by disabling the clock when not in need.	Static power may increase,delay also increases.
Power Gating	Reduces leakage power	Increases layout area and propagation delay
Transistor Stacking	Saves leakage current, easy to implement and fabricate.	Increase in propagation delay.
DT-CMOS	Minimizes sub threshold leakage.	It requires more area

VII. CONCLUSION

In VLSI Design, dynamic power dissipation is much more than static power dissipation. Transistor activities are the cause of much larger dynamic power dissipation. Using reliable power optimization techniques at each abstraction level has become an important task for the designers. Through this paper it can be concluded that of all the abstraction levels, RTL and System level tends to save much power. The tolerance limits are more relaxed at RTL level as compared to Gate level. The several hours which are required to synthesize the design and to compute other levels, RTL power analysis can be completed in minutes. As RTL Level is the high-level synthesis, it provides the capacity to analyze large designs as a result power that is wasted from the interactions between various blocks can be isolated. At the System and RTL level, to reduce power the required sequential modifications are to be made. RTL Level is the micro-architecture level. With the help of this technique, wastage can also be avoided, locality exploitation and other key factors for power optimization. Therefore, if the power dissipation is maintained at higher level, then very much amount of power is saved which further will help to save costs and other maintaining equipments.

VIII. ACKNOWLEDGEMENTS

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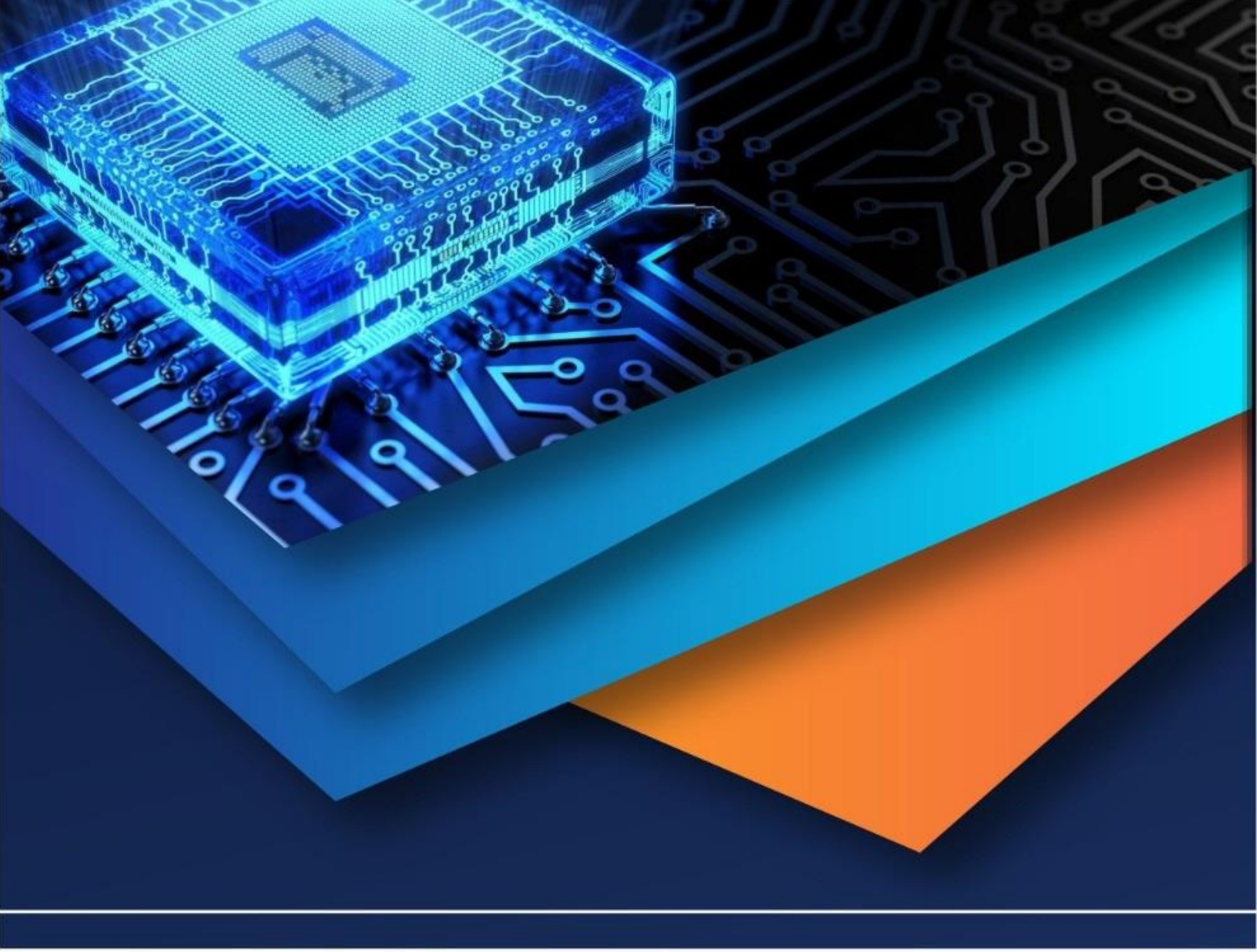

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