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Design of High Voltage Integrated Class-F Amplifier for Ultra Sound Transducers

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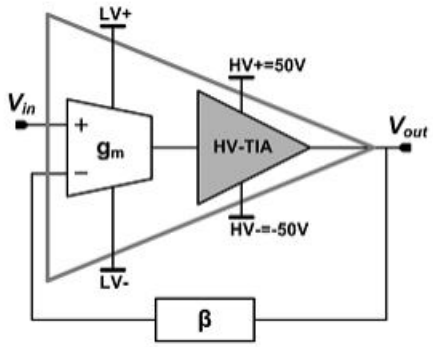
Abstract— Pulsers are usually adopted in ultra sound applications due to their efficiency. On the other hand, amplifiers would enable apodization profiles with high resolution; beams with low harmonic content and instantaneous changes in transmit energy between pulses. Their use is rather limited when relying on a discrete technology approach, due to high manufacturing costs and space occupation. In view of an increased level of integration, the availability of a BCD technology, capable of watts level driving at high frequency, encourages investigation of linear amplifiers, the topic of this work. Advantages in terms of reliability, space and cost would derive. The proposed amplifier, closed in a feedback loop, uses a high low-voltage transconductor driving a high voltage trans-impedance stage operating in class-B. Device parameters vary with signal amplitude making circuit analysis involved. Techniques to analyze large signal frequency response, distortion and stability are proposed in this paper leading to useful design insights.
Keywords --BCD technology, class-B, descriptive function, high-voltage ICs, linear amplifier, ultrasound.

I. INTRODUCTION

There are major trade-offs to be considered when designing ultrasound front-end circuits. Performance parameters in the front-end circuit components affect diagnostic performance—and conversely, system configuration and objectives affect the choice of components. It is essential for designers to understand the specifications that are of particular importance, their effect on system performance, and how they are affected by integrated-circuit (IC) design trade-offs—in terms of integration and semiconductor process technology—that will limit user design choices. Awareness of these considerations will help the designer to achieve the most advantageous system partitioning. Real time ultra-sound imaging systems have been available for more than thirty years. Nonetheless, considerable advancement in the functions of ultra-sound systems and beam-formers is presently underway.



Block diagram of proposed amplifier

The renewed interest is determined by a potential increase in device volumes, with low cost ultra-sound devices recently hitting the market, and by the ever increasing rates when data are transferred from the array to the electronics in reception. Integration and advanced electronics, e.g. including microelectro-mechanical systems, are playing a key role. In this work, we address the design of transducer's drivers which need to be capable of high output powers up to the MHz frequency range. Pulsers are usually adopted because of the high efficiency and simplicity. Linear amplifiers are nonetheless very attractive enabling apodization pro files with high resolution, beams with low harmonic content and instantaneous changes in transmit energy between pulses. But their use is today rather limited because of the high manufacturing costs, power dissipation and space constraints. Block diagram of proposed

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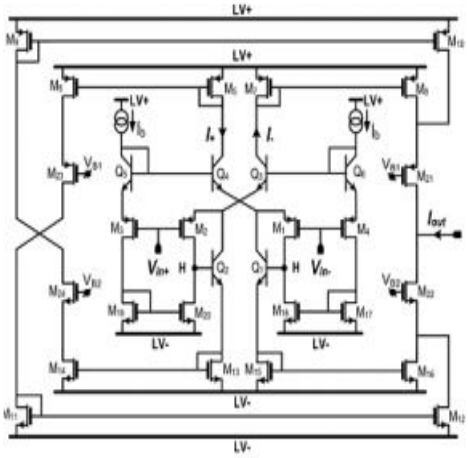
amplifier

II. OPERATIONAL AMPLIFIER IN BCD-SOI TECHNOLOGY

The adopted BCD6-SOI technology has two poly and four metal layers and embeds 5 V npn bipolar devices and 0.35 CMOS transistors with a nominal supply of 3.5 V. Power DMOS-Fets used in the design have 1 minimum channel length and support a maximum of 100 V. The maximum cut-off frequencies, at the overdrive voltage of 2.5 V, are 6 GHz and 2.2 GHz for nDMOS and pDMOS, respectively. The trans-impedance stage devices operate under the maximum supply voltage of 50 V but for minimum quiescent power consumption, devices are all biased in sub-threshold (class-B). The transconductor uses the 3 V low voltage supply in order to save power consumption while using large biasing current for maximum.



Schematic of the transconductor.

The amplifier uses two different supplies and a unity current gain buffer bridges transconductor to trans-impedance stage. The input transconductor is in class-AB, with peak output currents larger than biasing current to meet the tight slew rate requirements with limited power dissipation. The detailed schematic is reported in Fig. 2. The input pair uses bipolar transistors for maximum. The combination of pMOS and npn devices replaces pnp, not available in this technology. The drawback of this solution is the relatively low frequency of the pole at the base resistance and capacitance of respectively, mandate in frequency compensation to have a stable closed-loop amplifier response

III. ANALYSIS OF THE LARGE SIGNAL GAIN AND FREQUENCY RESPONSE

The simplified schematic is shown in the figure. Two batteries provide a level shift equal to the threshold voltage of M10, M12 emulating the role of diode connected devices in Figure. The buffer is required to provide low output impedance making the overall amplifier response robust against variations of the load, made by the parallel combination of 100 resistor and 150 pF capacitor. The output transistors have to be sized wide enough to deliver the required peak output current to the load while keeping the applied voltage within safe operating limits. The approach is commonly applied to the analysis of tuned RF circuits, where a sharp resonant load rejects harmonics. Comparison of the analytical results against circuit simulations will show that analysis through the describing function leads to very accurate results also for broadband amplifiers, as in our case, where harmonics are not or eventually mildly attenuated. If is the output stage transconductance describing function, expressions for gain Av and 3 dB bandwidth are given by

$$Av = ((Gm*Rl)/(1+Gm*Rl)).....1$$

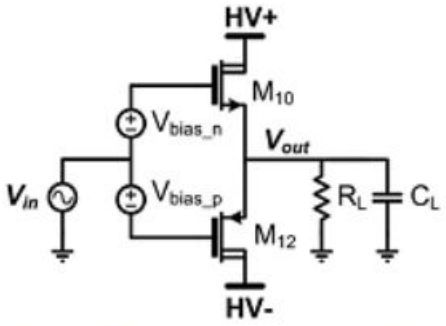
$$f\text{-}3\ dB,buff = 1/((2pi*Cl)*((1/Cm)//Rl)) = Gm/(2pi*Cl).....2$$

Assuming square-law mosfet models, the output stage current Iout (t) is given by \

$$Iout(t) = \beta n/2 *VOD\ 2 *sin2\ (w0t)\ 0<=W0t< \boldsymbol{\pi}$$

The calculated low frequency gain is compared against the results of transient circuit simulations in Figure assuming the nominal

load components and the device dimensions derived previously. For, calculations and simulations are in very good agreement. For the simulated gain does not fall to zero, as predicted, but saturates at around 6 dB. In this region the amplifier has a linear behavior, i.e. the gain is flat and independent of the output voltage, due to the sub-threshold current conduction, neglected in the analysis.



Simplified schematic of the output buffer

Trans-impedance stage : Assuming negligible output conductance of M5 and M8, the trans-impedance stage behaves as an integrator with the following transfer function:

$$Vout = Iin/(2pi*fc) *Av$$

where Av is the buffer gain, Cx is the parasitic capacitance at node X and Iin is the signal current delivered by the low-voltage transconductor. If Gm is the transconductance of the low-voltage stage, and Iin = Gm * Vin the gain-bandwidth product of the complete amplifier is estimated as:

$$GBW = Gm * Av /2piCx$$

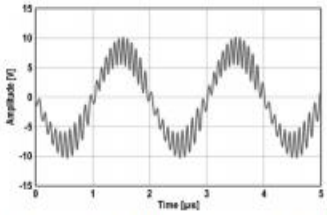
The higher the signal amplitude the lesser the input referred capacitance because bootstrap of is more effective. The describing function can be applied to estimate the frequency location of the secondary poles introduced by the commongate and current-mirror devices under large signal operation. As an example, and pole frequency for the pMOS diode connected device of the mirror reported in Figure, are given by:

$$Gm =0.2pi(\beta*Iin)\ 1/2\ Fp = 0.1\ ((\beta*Iin)\ 1/2/Cp)$$

It can be verified that also all other poles are at least one decade beyond 7 MHz, thus assuring a trans-impedance single pole lowpass closed loop shape.

IV. STABILITY

Class B operation determines signal dependent circuit parameters mandating further insight to assess closed loop stability conditions. Instability manifests itself as a relatively small signal superimposed to the desired output signal, as shown by the simulated transient waveform in Figure. We can imagine a small sinusoid of amplitude and angular frequency superimposed to the large driving signal at with amplitude. For the analysis we refer to the block diagram of the closed-loop amplifier in Figure.



Transient output voltage showing instability

V. CONCLUSIONS

Linear operational amplifiers for transducers driving in ultrasound applications are very attractive improving the quality of diagnostic systems. On the other hand, their use is rather limited because they are usually realized with discrete components resulting in large manufacturing costs. In this work, we have leveraged the availability of a BCD-SOI technology and investigated

the design of high voltage swing linear amplifier. The analysis carried out in-depth has provided insight useful for circuit design, able to assess large-signal gain and frequency response, distortion and stability. Experiments are in good agreement with simulations and models and show that amplifier performances are adequate for the application. The analysis presented in this paper provides also design keys toward improvement to wider operating frequency and/or lower distortion.

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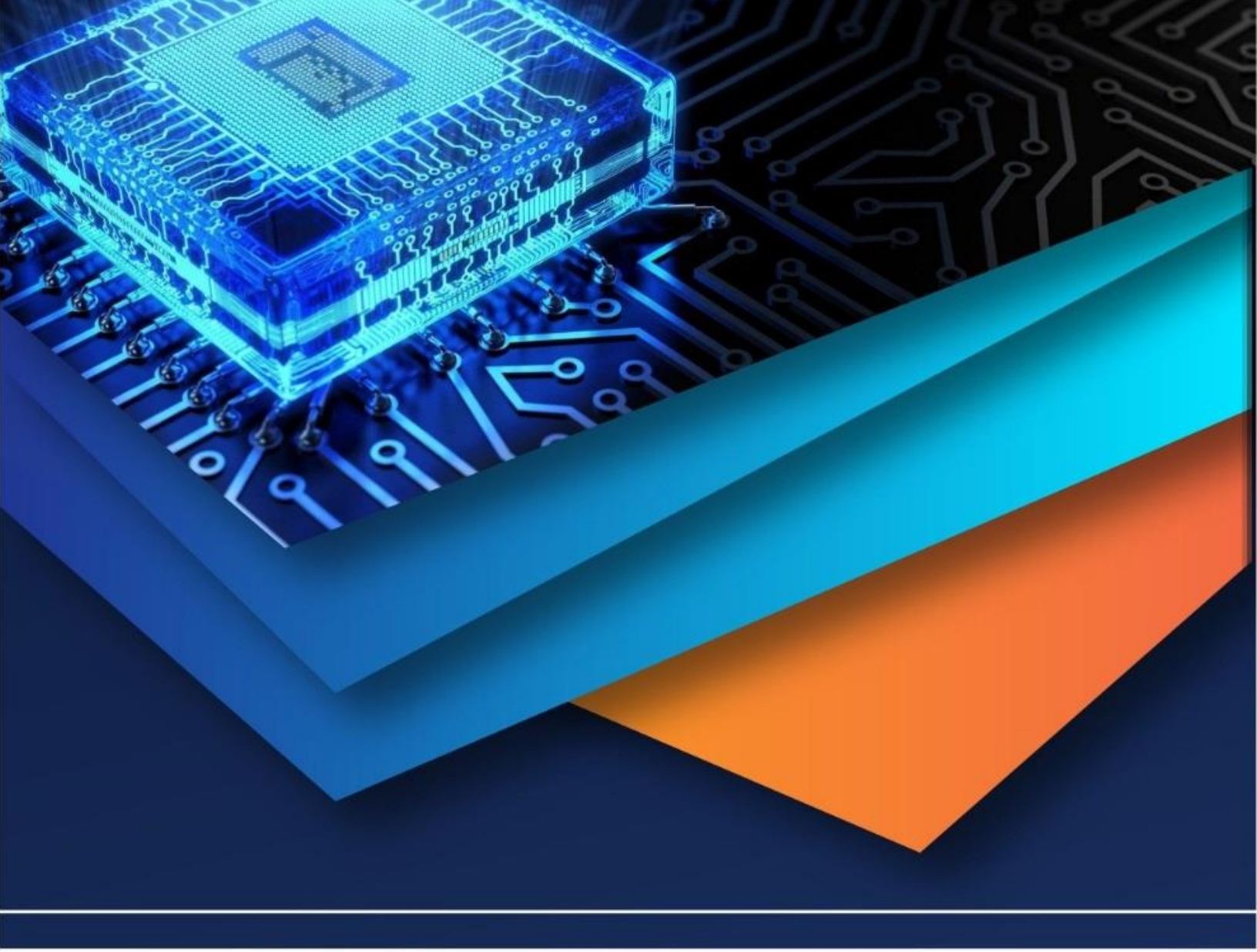
REFERENCES

[1] S. Cochran, A. Bernassau, D. Cumming, C. Demore, M. Desmulliez, and J. Sweet, ―Future integration of Silicon Electronics with miniature piezoelectric ultra-sonic transducer and array,‖ in Proc. Ultrasonics Symp., San Diego, CA, USA, December 2010, pp. 1108–1116.
[2] GE Healthcare, Vscan Data Sheet 2010 [Online]. Available: www. gehealthcare.com
[3] J. H. Sweet, D. Hutson, S. Cochran, and A. Bernassau, ―Concepts and issues in piezo-on-3D silicon structures,‖ Sensor Rev., vol. 29, no. 4, pp. 326–332, 2009.
[4] K. Chen, H.-S. Lee, A. P. Chandrakasan, and C. G. Sodini, ―Ultrasonic imaging transceiver design for CMUT: A three-level 30-Vpp pulse-shaping pulser with improved efficiency and a noise-optimized receiver,‖ IEEE J. Solid State Circuits, no. 99, pp. 1– 12, Aug. 2013.



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