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Power Efficient Fir Filter Design

Ranjini.C, Thiruvenkadam.S

PG scholar, VLSI design, HOD,IT Department,
P.A College of Engineering and Technology,
Tamilnadu, India

Abstract: ***Finite Impulse Response (FIR) digital filter is basic component in communication systems and in many digital signal processing (DSP). FIR filter is broadly used in portable application with small area and low power. In this work by using multiple control signal decision logic and amplitude detection logic we can reduce the power of FIR filter. In FIR filter extensive variations occur in input data and in coefficient. The filter order is dynamically changed in accordance with amplitude of both filter input data and filter coefficients. The power of the proposed FIR filter is reduced by 5mW from previous fir filter.***
KeyWords: **Finite impulse response (FIR), approximate filtering, low power filter, reconfigurable design**

I.INTRODUCTION

Demand for the low power digital signal processing (DSP) is increasing day by day. Finite impulse response (FIR) is the major operation used in the DSP. A general FIR filter of order N can be expressed as equation (1):

$$y(n) = \sum_{i=0}^{N-1} b_i x(n-i) \ldots\ldots\ldots\ldots (1)$$

Where N denotes the length of FIR filter,b_i denotes the *i*th coefficient, and *x(n – i)* is the input data at the time instant *n – i*. In large DSP application FIR filter with considerably large number of taps are required. Reducing the area and power ingestion is the main intention of many previous papers while maintaining the fixed filter order[1]–[3]. In those papers add and shift operations are applied to the FIR filter structure to minimize the number of addition and subtraction.

The main drawback come across for those approaches are that once the filter architecture is decided, the coefficients cannot be changed so that these techniques are not relevant FIR filter with programmable coefficients. For the design of low power digital filter [5], [6], approximate signal processing [4] is used. [6] Shows that the energy quality characteristics of FIR filter can be improved by sorting both the data samples and filter coefficients before the convolution operation. Area efficient FIR filter [base] design in achieved with the help of faithfully rounded truncated MCMA.

Real time sorting of all incoming samples are very difficult. Reconfigurable FIR filter architectures [7]-[9] are used for low power implementations or to recognize several frequency responses by means of a single filter [10].

A area and power efficient FIR filter architecture is designed, where the filter order can be changed with respect to the amplitude of both filter coefficient and the inputs. Area of FIR filter is reduce using the concept of faithfully rounded truncated MCMA and the power can be reduce by cancelling unwanted multiplication operation.

II. EXISTING FIR FILTER ARCHITECTURE

The direct form of FIR filter is adopting for this project. The direct form of a FIR filter is as shown in fig.1.where all products in *bi* × *x [n –i]* are summed up with MCMA module.

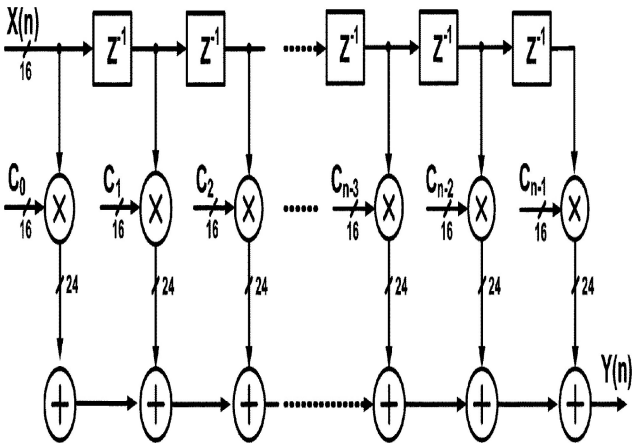

Fig -1: Architecture of Direct form FIR filter.

The existing method will efficiently collect all the partial products (PP) into a single PPB matrix with carry- save addition. It is more efficient than accumulating individual

multiplication for each product. This operation will reduce the matrix height to two, followed by a final carry propagation adder.

Faithfully rounding and truncating method of operation is implemented in the FIR filter to reduce the number of arithmetic operation. The total error in arithmetic operation introduced in this method is not larger than one ulp. The most recent truncated multiplier design is as shown in the fig.2.

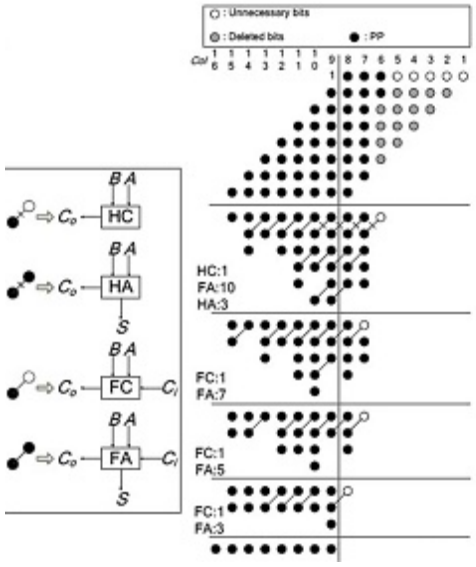

Fig -2: improved version of truncated multiplier designs using the approach in [12].

In the improved version of truncated multiplier designed using the approach [13] can delete more PPBs which leads to the reduction in area cost. This multiplier made a single row of PPBs undeletable and also the elimination of the PPB consists of deletion and rounding. By using the improved version of truncation design an architecture of MCMA with truncation (MCMAT) which removes the unnecessary PPBs as shown in fig 3.In fig 3 the L-shaped block with white circles represents the undeletable PPBs. Gray color circles represents the deletion of PPBs. The crossed circles represent the rounding of resultant bits after PP compression. All the offset and bias constants required including the sign bit modifications are represented in the last row of PPB matrix.

III. PROPOSED FIR FILTER STRUCTURE

Fig 1 shows the direct form FIR filtering operation performs the convolution, the weighted summations of input sequences. Low pass, high pass and band pass filters are using the convolution operation to realize frequency selective application. The FIR filter power consumption and its amount of computation is directly proportional to its order. So that we can achieve significant power saving by reducing the filter order by turning off some of the multiplier. The degradation of filter performance should be considered when we change the filter taps.

Coefficients of a typical 25-tap low pass FIR filter is shown in fig 4. The central coefficient c_{12} has the largest value in 25- tap filter and the amplitude of the coefficient decreases as$k$ becomes more distant from the centre tap.

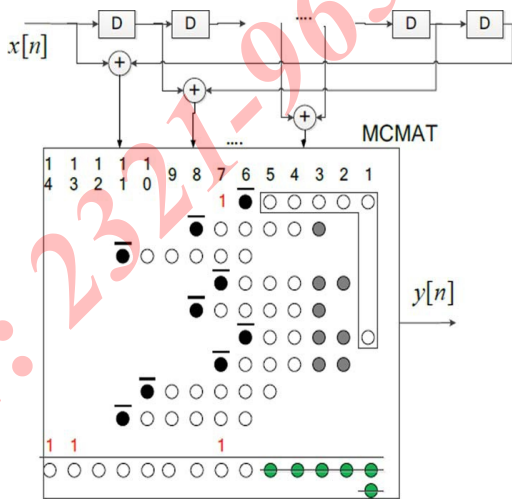

Fig -3: Overall FIR filter architecture using multiple constant multipliers/accumulators with faithfully rounded truncation (MCMAT).

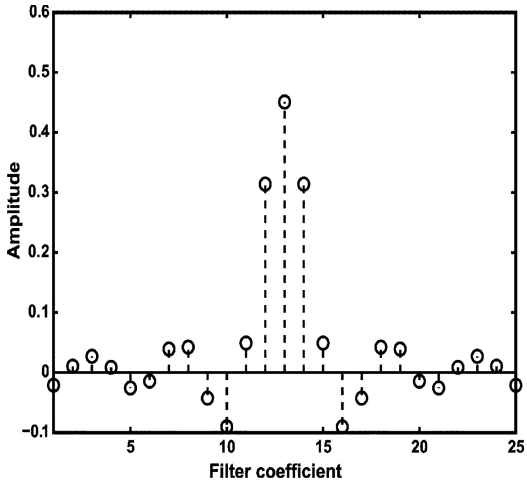

Fig -4: Amplitude of the 25-tapequi-ripplefiltercoefficients.

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The FIR inputs *x(n)* are multiplied with the coefficients therefore the amplitude of the inputs are also changes. If the amplitudes of both the coefficient and data input of a FIR filter are small then the multiplication of those two numbers are proportionately small. Thus we can turn off the corresponding multiplier has negligible effect on the filter performance.

DSP application are widely using the two's compliment data format, if one or both of the multiplier input has negative value, multiplication of two small values gives rise to large switching activities, which is due to the series of 1's in the MSB part. Power saving can be achieved by cancelling the multiplication of two small numbers with negligible degradation in filter performance.

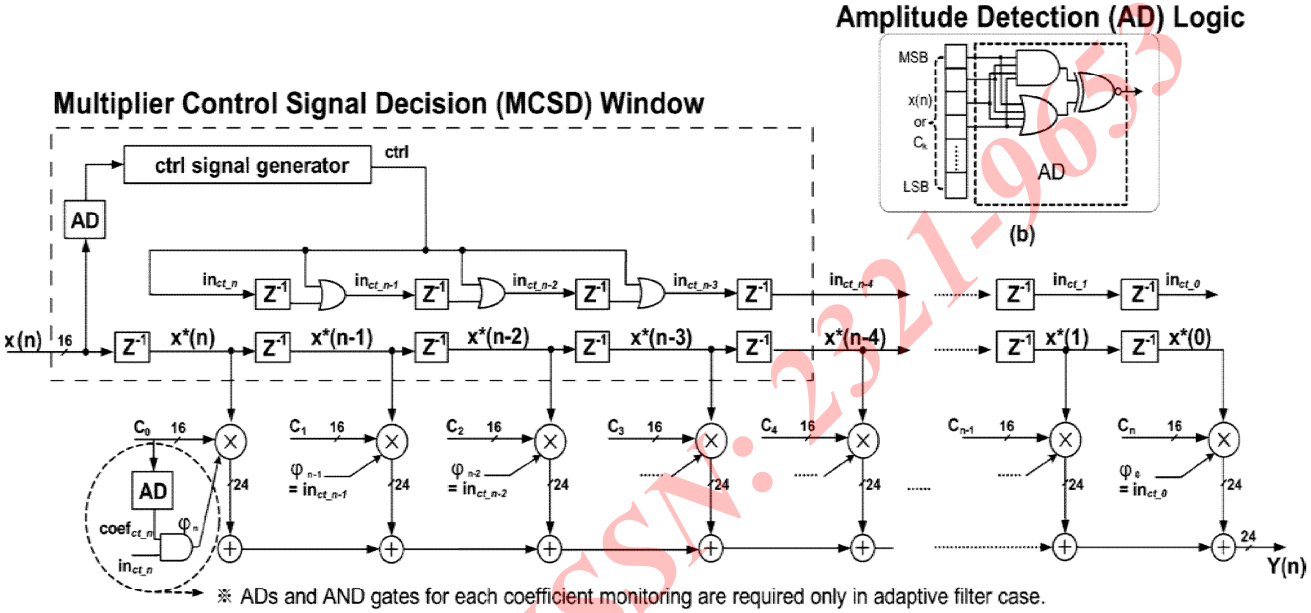

Fig -5: a) Proposed reconfigurable FIR filter architecture.(b)Amplitude detection logic (AD).

Generally in the fixed width FIR filter full operand bit-width of the multiplier is not used. When the bit-width of filter input and the filter coefficient are 16, the multiplier generates 32 bit outputs. By considering the circuit area of following adder, the LSB of the multiplier outputs are truncated or rounded off, which incurs quantization error. For example in fig 1, we have used 24 bits. When we turn off the multiplier in the FIR filter, if we can carefully select the input and coefficient amplitudes such that the multiplication of those two numbers are as small as the quantization error, filter performance degradation can be made negligible.

Considering the threshold of the input is x_{th} and the coefficient is c_{th}. We can turn off the multiplier for cancelling the multiplication operation in FIR filter by considering the threshold. If the threshold of the *x(n)* and c_k are lesser than its threshold value, the corresponding multiplier can turn off. When we determine x_{th} and c_{th}, the trade-off between filter performance and power savings should be carefully considered.

IV.PROPOSED ARCHITECTURE

The architecture of a proposed FIR filter is shown in fig 5(a). To scrutinize the amplitude of data input *x(n)*and also the coefficient c_k, an amplitude detector (AD), in fig 5(b) is used. If the amplitude of the one or both multiplier input signals are smaller than the threshold then we can cancel the corresponding multiplication operation. The output of the AD is set to 1 when the absolute value of $x(n)$ is smaller than the input threshold x_{th}. The design of AD is dependent on the input threshold x_{th} , where the fan-in's of AND and OR gate are decided by x_{th}. If x_{th} and c_{th} have to be changed adaptively due to designer's considerations, AD can be implemented using a simple comparator.

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Switching activity on the internal node capacitance is a main factor which affects the dynamic power consumption of CMOS logic gate. In this proposed reconfigurable FIR filter, we can turn off the multiplier according to the amplitude of each input. If the amplitude of the input *x(n)* rapidly changes for every cycle, the multiplier will turn on and off continuously, which produces continuous switching activities.

To control this switching problem we are using multiplier control signal decision (MCSD) window in fig 5(a). MCSD generate control signal *ctrl*, which counts the number of input samples smaller than x_{th} are counted and multipliers are turned off only when m consecutive input samples are smaller than x_{th}. In the fig 5(a) *m* denotes the size of MCSD. The detailed diagram of *ctrl* signal generator design is as shown in fig 6. If an input signal smaller than x_{th} comes in then the output of the AD is set to "1", then the counter is counting up.

Only the first gate of the multiplier is modified and once the is set to "1", there is no switching activity in the following nodes and multiplier output is set to "0". The area overhead for the proposed reconfigurable filter are flip-flops for $in_{ct\text{-}n}$ signals, AD and *ctrl* signal generator inside MCSD and the modified gates in fig 7 for turning off multiplier. Those overheads can be implemented using simple logic gates, and a single AD is needed for input $x(n)$ monitoring as specified in Fig. 3(a). Consequently, the overall circuit overhead for implementing reconfigurable filter is as small as a single multiplier.

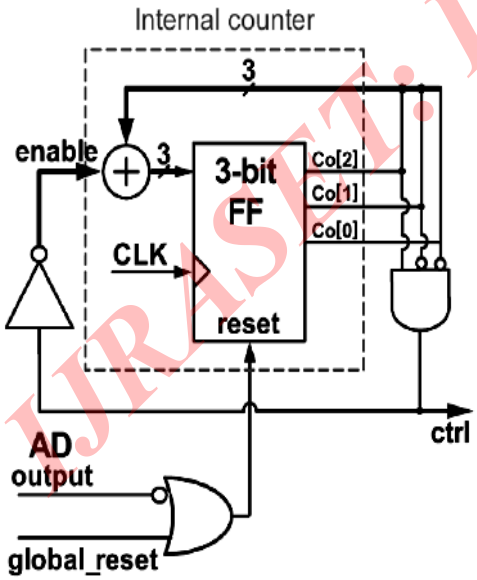

Fig -6: Schematic of *ctrl* signal generator. Internal counter sets *ctrl* signal to "1" when all input samples inside MCSD are smaller than $x_{th.}$

The *ctrl* generator changes to "1"after the counter reaches m which shows that m successive small inputs are observed and multipliers are set to turn off. To decide the multiplier operation by monitoring the value of c_{th} and x_{th}, one additional bit $in_{ct\text{-}n}$ in fig 5 is added. The additional bit is controlled by *ctrl* and also the $in_{ct\text{-}n}$ accompanies the data all the way in the subsequent flipflops to shows that the input sample and the coefficients are smaller than x_{th} and c_{th} respectively. The $in_{ct\text{-}n}$ signal is fixed inside the MCSD; it does not change outside the MCSD and hold the amplitude information of the input signal. For the synchronization process between $x^*(n)$ and $in_{ct\text{-}n}$, add a delay component infront of the first strap in fig 5(a) since once clock latency is needed due to the counter in MCSD.

In case of the adaptive filter more ADs are needed for monitoring the amplitudes of each coefficient as shown in fig 5(a). However, in the FIR filter with fixed or programmable coefficients, since we know the amplitude of coefficients ahead, extra AD modules for coefficient monitoring are not needed.

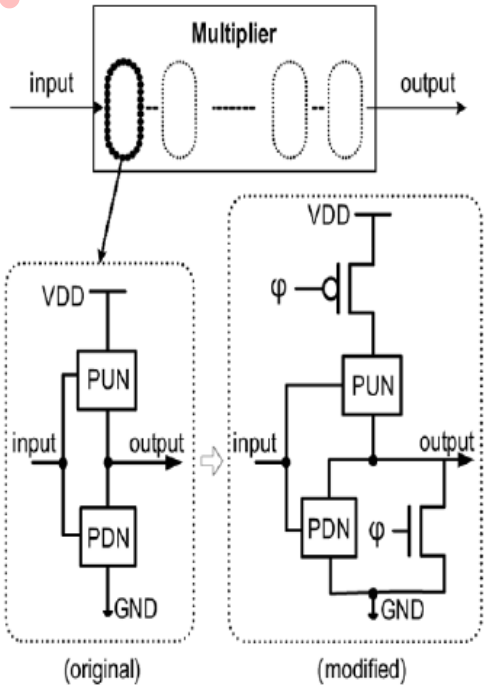

Fig 7. Modified gate schematic to turn off multiplier

After comparing the input and coefficient are smaller than x_{th} and c_{th}, respectively, the multiplier is turned off by setting

the output$\varphi_n$signal to "1". By using the simple technique discussed [11] in fig 7, the multiplier can be turned off easily and the output is enforced to "0". Fig 7 shows, if the control signal φ_n is "1" then the PMOS turns off and NMOS turns off, the gate output is enforced to "0" irrespective of the input. If the φ_n value is "0" then the gate will functions like a normal gate.

IV. SIMULATION RESULTS AND COMPARISON

Simulation result of FIR filter by using the two software Xilinx ISE 8.1 and Modelsim 6.3f is given below. The simulated waveform output of FIR filter is as shown below in fig 8. The simulation results are taken by using modelsim 6.3f version software. We generate a output for four tap FIR filter with clk input. The coefficient values are fixed.

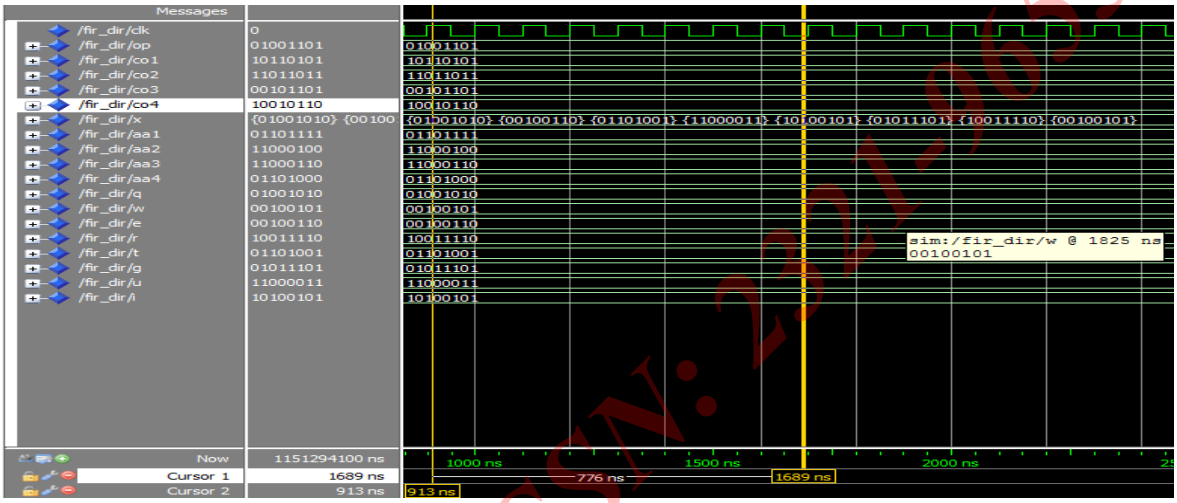

Fig .-8: Simulation Result of FIR filter

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		103
Vccint 1.80V:	54	97
Vcco33 3.30V:	2	7
Inputs:	8	15
Logic:	30	55
Outputs:		
Vcco33	0	0
Signals:	0	0
Quiescent Vccint 1.80V:	15	27
Quiescent Vcco33 3.30V:	2	7

Thermal summary:	
Estimated junction temperature:	27C
Ambient temp:	25C
Case temp:	27C
Theta J-A:	17C/W

Fig -9: Power analysis of proposed FIR filter

The power usage of the proposed FIR filter is as shown below in fig 9. The power consumption value can be found by using the Xilinx ISE 8.1 software. Power usage of this proposed FIR filter is 103mW and this is comparatively less than the power usage of previous FIR filter. And also the delay also has been reduced from 2.636 ns to 1.568 ns.

COMPARISON

	By using Existing method	By using proposed work
POWER	108mW	2.636ns
DELAY TIME	103mW	1.568

V.CONCLUSION

In this paper, we tend to propose less power reconfigurable FIR filter design to permit economical trade-off between the filter performance and computation energy. Within the projected reconfigurable filter, the input data measures are monitored and therefore the multipliers within the filter turned off once each the coefficients and inputs square measure sufficiently small to mitigate the result on the filter output. Therefore, the projected reconfigurable filter dynamically changes the filter order to attain important power savings with minor degradation in performance. Power savings and filter performance degradation square measure diagrammatical as robust functions of MCSD window size, the input and coefficient thresholds, and input signal characteristics. The projected theme achieves power savings up to 41.9% with but around 5.34% of space overhead with terribly sleek degradation within the filter output. The projected approach may be applicable to alternative areas of signal process, wherever a correct trade-off between power savings and performance degradation ought to be rigorously thought-about. the concept bestowed during this paper will assist within the style of FIR filters and its implementation for low power applications.

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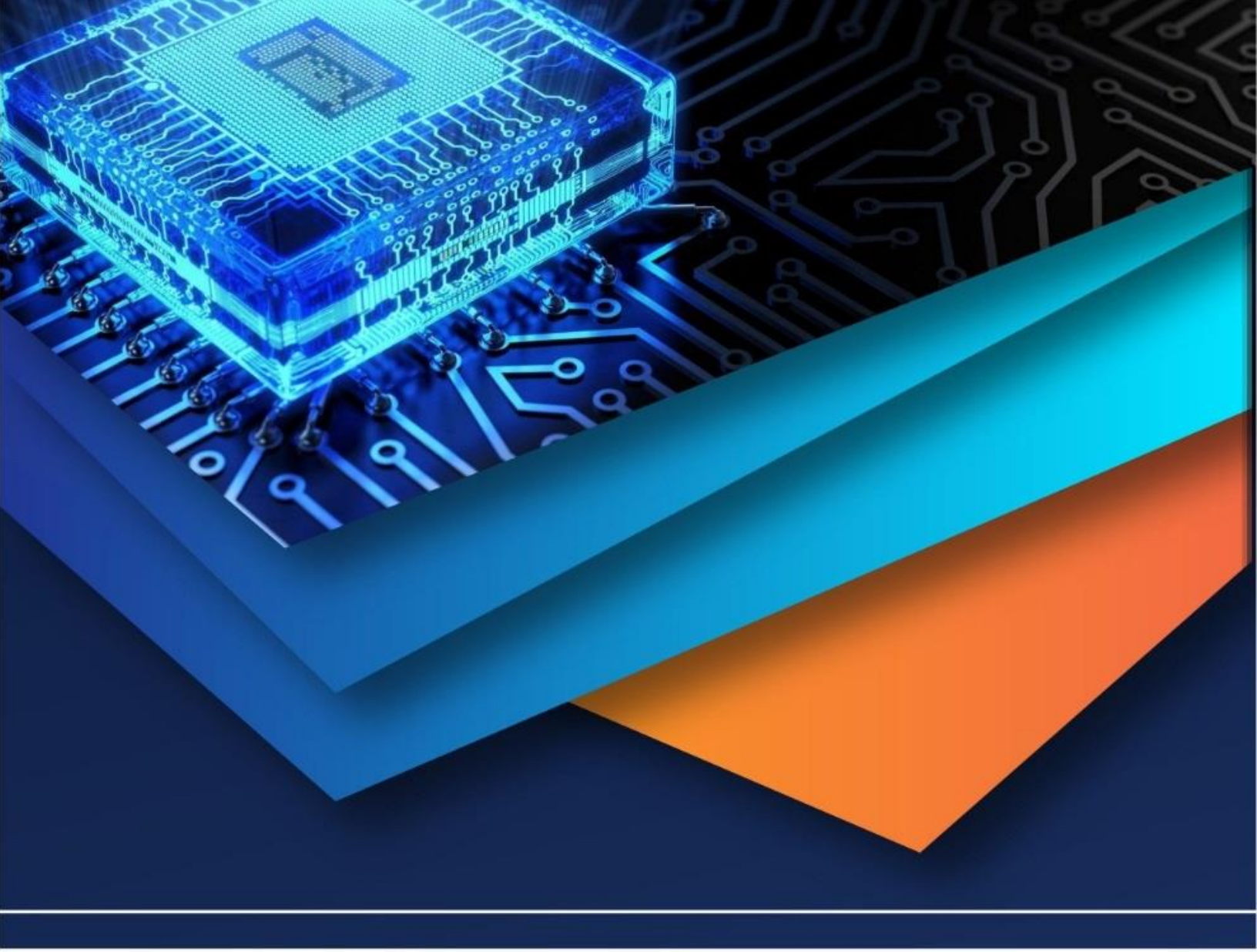
BIOGRAPHIES

Ranjini.c received the B.E. and. degrees in electronics and communication engineering from Anna University, Chennai, in 2012 and doing the M.E degree in VLSI Design in the Anna University ,Chennai. Her research interest includes low power circuit and system design for digital signal processing and digital communications.

Dr.Thiruvenkadam.S, He received the B.E. degree in Electrical and Electronics Engineering from Bharathiar University in1999, the M.E. degree in Power Systems from Annamalai University in 2004 and completed his Ph.D. in Power Distribution System reconfiguration at Anna University in 2012, Coimbatore, India. Currently, he is working as a HOD in the Department of IT in P.A. College of Engineering and Technology, Tamilnadu, India. He is a member of IEEE and Life Member of ISTE. His research interests include software frame work, power distribution systems, digital control techniques for power electronic circuits and power distribution systems.



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