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Regulating-Speed PFC Bridgeless Buck–Boost Converter-Fed BLDC Motor Drive With Fuzzy Controller

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Abstract — This paper proposes a power factor corrected (PFC) to converter- fed brushless direct current (BLDC) motor drive. A PFCBL buck–boost converter is designed to work in discontinuous inductor current mode (DICM) to offer an inherent PFC at ac mains. The working of the proposed drive is calculated over a wide range of speed control and unstable supply voltages with improved power quality at ac mains. The obtained power quality indices are within the acceptable limits of international power quality standards. For low-power applications a power factor corrected (PFC) bridgeless buck–boost converter-fed brushless direct current (BLDC) motor drive as a cost-effective solution. a single voltage sensor is used by controlling the dc link voltage of the voltage source inverter (VSI) in BLDC motor speed control. This provides the operation of VSI at fundamental frequency switching by using the electronic commutation of the BLDC motor which offers reduced switching losses. A Bridgeless (BL) configuration of the buck–boost converter is proposed which offers the elimination of the diode bridge rectifier, thus reducing the conduction losses associated with it. The performance of the proposed drive is simulated in MATLAB/Simulink.

Index Terms—Bridgeless (BL) Buck–Boost Converter, BLDC) Motor, Discontinuous Inductor Current Mode (DICM), Power Factor Corrected (PFC), Power Quality

I. INTRODUCTION

The need of the brushless direct current (BLDC) motor in these applications is becoming very common due to features of high efficiency, high flux density per unit volume, less maintenance requirements, and least electromagnetic-interference problems. Efficiency and cost are the main concerns in the growth of low-power motor drives targeting domestic applications such as fans, water pumps, blowers, mixers, etc. These BLDC motors are not controlled to household requirements, but these are suitable for other applications such as medical equipment, transportation, HVAC, motion control, and many industrial tools. A BLDC motor has three phase windings on the stator and permanent magnets on the rotor. an electronic commutation based on rotor position is used rather than a mechanical commutation so it is called as an electronically commutated motor. Because it avoids disadvantages like wear and tear and sparking of brushes and commutator assembly, Power quality problems have become important issues to be considered due to the recommended Control of harmonics in supply current by various international powerqualitystandards.

For class-A equipment (< 600 W, 16 A per phase) which includes domestic equipment, IEC 61000-3-2 restricts the harmonic current of different order such that the total harmonic distortion (THD) of the supply current should be below 19% [7]. Many topologies of the single-stage PFC converter are reported in the literature which has gained importance because of high efficiency as compared to two-stage PFC converters due to low component count and a single switch for dc link voltage control and PFC operation [9], [10].

The choice of mode of operation of a PFC converter is a critical issue because it directly affects the cost and rating of the components used in the PFC converter. The continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are the two modes of operation in which a PFC converter is designed to operate [9], [10]. In CCM, the current in the inductor or the voltage across the intermediate capacitor remains continuous, but it requires the sensing of two voltages (dc link voltage and supply voltage) and input side current for PFC operation, which is not cost-effective. On the other hand, DCM requires a single voltage sensor for dc link voltage control, and inherent PFC is achieved at the ac mains, but at the cost of higher stresses on the PFC converter switch; hence, DCM is preferred for low-power applications [9], [10]. The conventional PFC scheme of the BLDC motor drive utilizes a pulsewidth-modulated voltage source inverter (PWM-VSI) for speed control with a constant dc link voltage. This offers higher switching losses in VSI as the switching losses increase as a square function of switching frequency. As the speed of the BLDC motor is directly proportional to the applied dc link voltage, hence, the speed control is achieved by thevariable

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dclinkvoltage ofVSI.Thisallowsthefundamental frequency switching of VSI (i.e., electronic commutation) and offers reduced switching losses. Singh and Singh [11] have proposed a buck–boost converter feeding a BLDC motor based on the concept of constant dc link voltage and PWM-VSI for speed control which has high switching losses. A single-ended primary-inductance converter (SEPIC)-based BLDC motor drive has been proposed byFig. 1. Proposed BLDC motor drive with front-end BL buck–boost converter.

These can provide the voltage buck [13] or voltage boost [14], [15] which limits the operating range of dc link voltage control have proposed a BL buck–boost converter but use three switches which is not a cost-effective clarification. A new family of BL SEPIC and Cuk converters has been reported in the literature [17]–[21] but requires a large number of components and has losses associated with it. This paper presents a Fuzzy based PFC - BL buck–boost converter-fed BLDC motor drive with variable dc link voltage of VSI for improved power quality at ac mains with minimized components.

II. CONVENTIONAL PFC BL BUCK–BOOST CONVERTER-FED BLDC MOTOR DRIVE

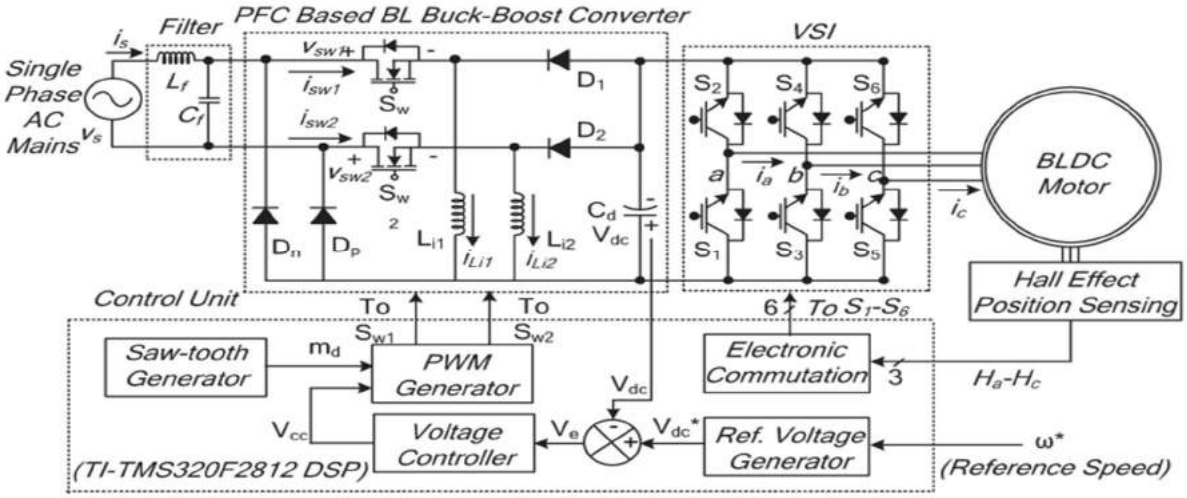

Fig. 1 shows the proposed BL buck–boost converter-based VSI-fed BLDC motor drive.

The parameters of the BL buck–boost converter are designed such that it operates in discontinuous inductor current mode (DICM) to achieve an inherent power factor correction at ac mains. The speed controlmotor is achieved by the dc link voltage control of VSI using a BL buck–boost converter. This reduces the switching losses in VSI due to the low frequency operation of VSI for the electronic commutation of the BLDC motor. The performance of the proposed drive is evaluated forawiderangeofspeedcontrolwithimprovedpowerqualityatacmains.Moreover, the effect of supply voltage variation at universal ac mains is also studied to demonstrate the performance of the drive in practical supply conditions. Voltage and current stresses on the PFC converter switch are also evaluated for determining the switch rating and heat sinkdesign.hardwareimplementationoftheproposedBLDCmotordriveis carried out to demonstrate the feasibility of the proposeddriveoverawiderangeofspeedcontrolwithimprovedpowerquality at ac mains.

The comparison is carried out on the basis of the total number of components (switch—Sw, diode—D, inductor—L, and capacitor—C) and total numberof components conducting during each half cycle of supply voltage. The BL buck [13] and boost [14], [15] converter configurations are not suitable for the required application due to the requirement of high voltage conversion ratio. The proposed configuration of the BL buck–boost converter has the minimum number of components and least number of conduction devices during each half cycle of supply voltage which governs the choice of the BL buck–boost converter for this application.

III. OPERATING PRINCIPLE OF PFC BL BUCK–BOOST CONVERTER

The operation of the PFC BL buck–boost converter is classified into two parts which include the operation during the positive and negative half cycles of supply voltage and during the complete switching cycle.

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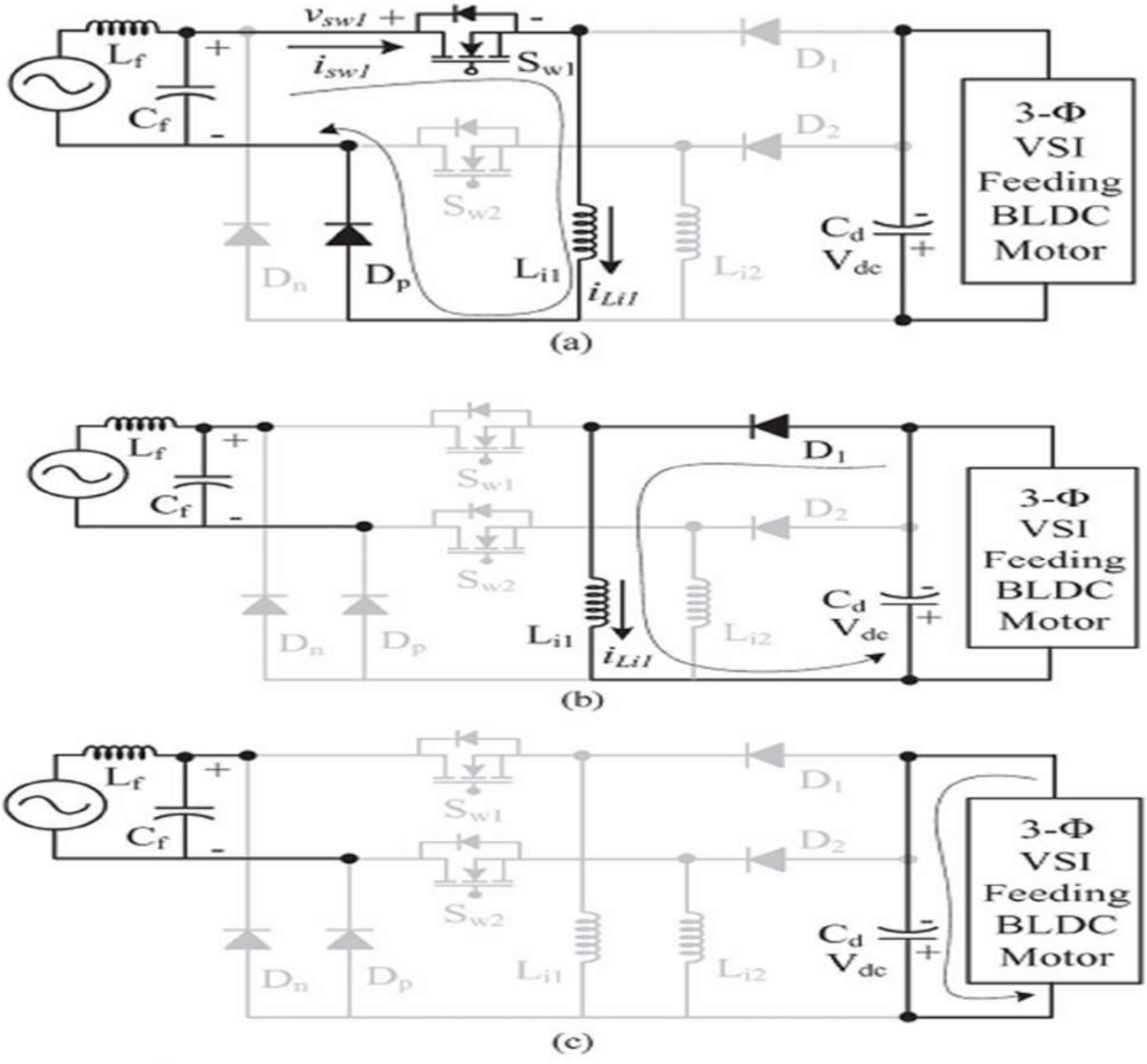
A. Operation During Positive And Negative Half Cycles Of Supply Voltage

In the proposed scheme of the BL buck–boost converter,switchesSw_1andSw_2operateforthepositiveandnegative half cycles of the supply voltage, respectively. During the positive half cycle of the supply voltage, switch Sw1, inductor Li_1, and diodes D_1 and D_p are operated to transfer energy to dc link capacitor Cd as shown in Fig. 2(a)–(c). Similarly, for the negative half cycle of the supply voltage, switch Sw_2, inductor Li_2, and diodes D_2 and Dn conduct as shown in Fig. 3(a)–(c). In the DICM operation of the BL buck–boost converter, the current in inductor Li becomes discontinuous for a certain duration in a switching period.

B. Operation During Complete Switching Cycle

Three modes of operation during a complete switching cycle are discussed for the positive half cycle of supply voltage as shown hereinafter.

1) Mode 1: In this mode, switch Sw1 conducts to charge the inductor Li1; hence, an inductor current iLi_1 increases in this mode as shown in Fig. 2(a). Diode Dp completes the input side circuitry, whereas the dc link capacitor Cd is discharged by the VSI-fed BLDC motor as shown in Fig. 3(d).



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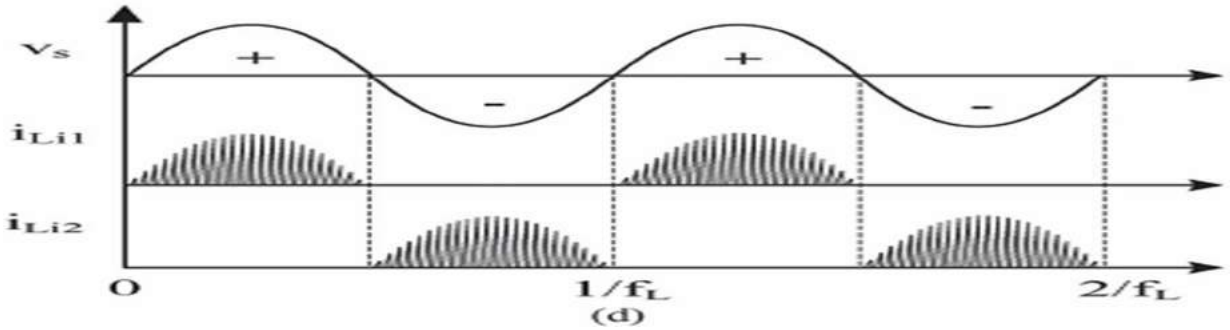


Fig. 2. Operation of the proposed converter in different modes (a)–(c) for a positive half cycle of supply voltage and (d) the associated waveforms. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Waveforms for positive and negative half cycles of supply voltage.

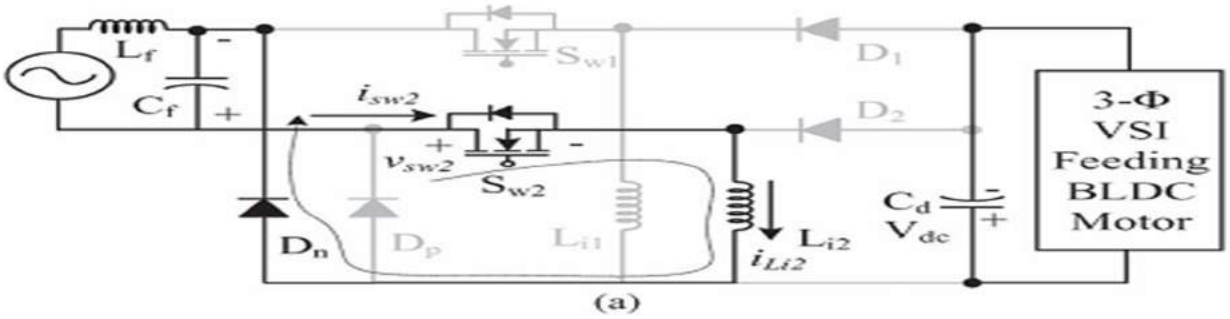
2) Mode 2: As shown in Fig. 2(b), in this mode of operation, switch Sw1 is turned off, and the stored energy in inductor Li1 is transferred to dc link capacitor Cd until the inductor is completely discharged. The current ininductor Li1 reduces and reaches zero as shown in Fig. 3(d).

3) Mode 3: In this mode, inductor Li_1 enters discontinuous conduction, i.e., no energy is left in the inductor; hence, currentiL_{i1}becomeszerofortherestoftheswitchingperiod.Asshown in Fig. 2(c), none of the switch or diode is conducting in this mode, and dc link capacitor Cd supplies energy to the load;hence,voltageVdcacrossdclinkcapacitorCdstartsdecreasing. The operation is repeated when switch Sw_1 is turned on again after a complete switching cycle

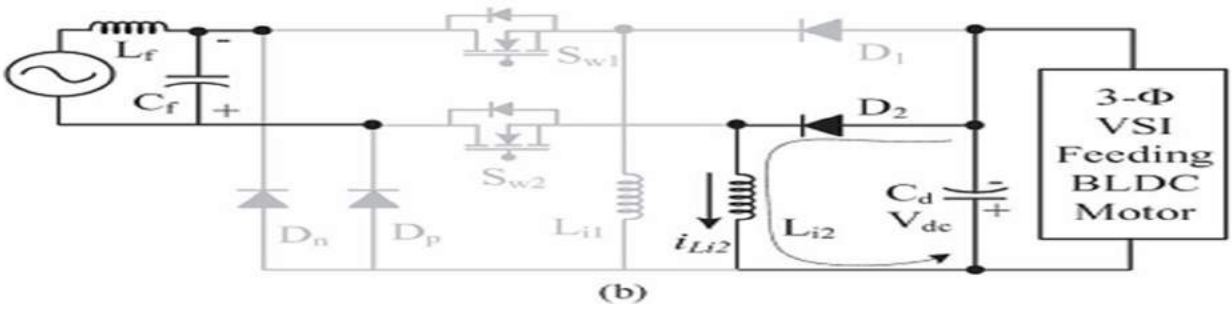
Similarly, for the negative half cycle of the supply voltage, switch Sw2, inductor Li2, and diodes Dn and D2 operate for voltage control and PFC operation.

IV. DESIGN OF PFC BL BUCK–BOOST CONVERTER

A PFC BL buck–boost converter is designed to operate in DICM such that the current in inductors Li_1 and Li_2 becomes discontinuous in a switching period. For a BLDC of power rating 251 W (complete specifications of the BLDC motor are given in the Appendix), a power converter of 350 W (Po) is



Mode1.



Mode2.

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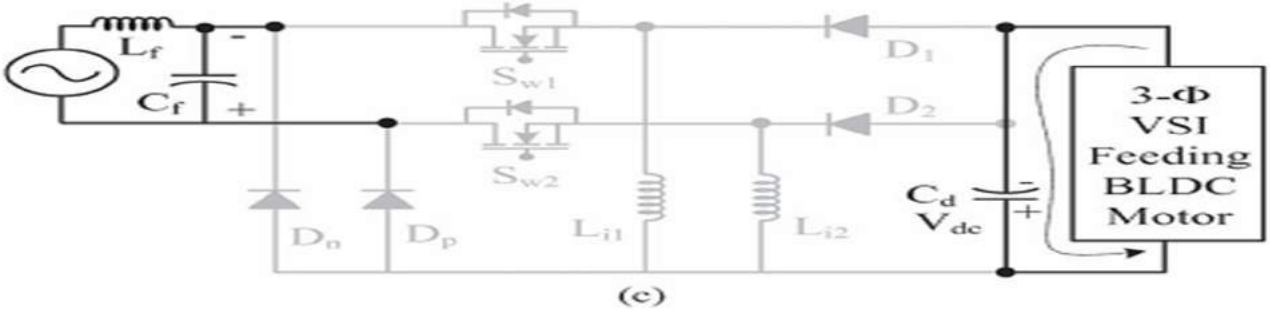
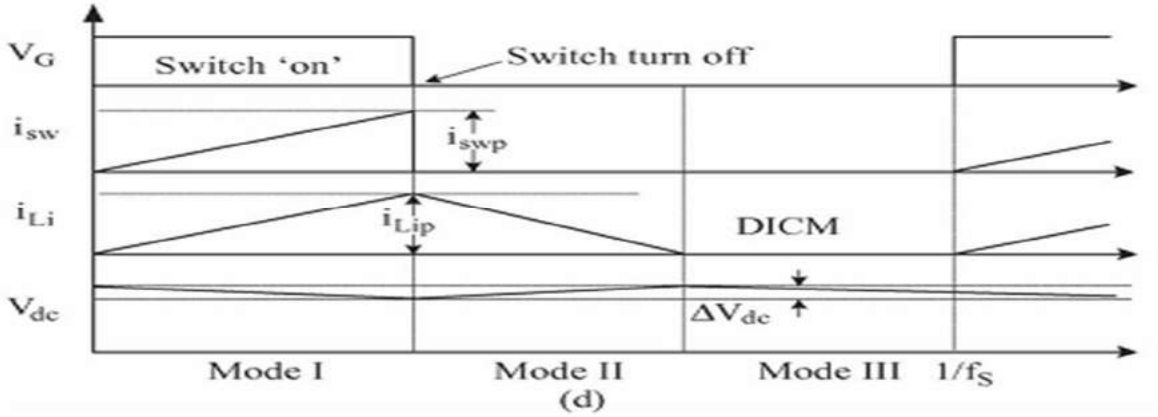


(c)

Mode3.



(d)

Fig. 3. Operation of the proposed converter in different modes (a)–(c) for a negative half cycle of supply voltage and (d) the associatedwaveforms.(modes1,2,3,4)

For a supply voltage with an rms value of 220 V, the average voltage appearing at the input side is given as [4]

$$Vin = 2\sqrt{2}Vs/\pi \quad . \quad (1)$$

The relation governing the voltage conversion ratio for a buck–boost converter is given as [2]

$$d = Vdc/Vdc + Vin. \quad (2)$$

The proposed converter is designed for dc link voltage control from 50 V (Vdcmin) to 200 V (Vdcmax) with a nominal value (Vdcdes) of 100 V; hence, the minimum and the maximum duty ratio (dmin and dmax) corresponding to Vdcmin and Vdcmax are calculated as 0.2016 and 0.5025, respectively.

A. Design Of Input Inductors (Li_1 and Li_2)

The value of inductance Lic1, to operate in critical conduction mode in the buck–boost converter, is given as [2]

$$Lic1 = R(1-d)2/2fs \quad (3)$$

where R is the equivalent load resistance, d is the duty ratio, and fs is the switching frequency. Now, the value of Lic1 is calculated at the worst duty ratio of dmin such that the converter operates in DICM even at very low duty ratio. At minimum duty ratio, i.e., the BLDC motor operating at 50 V (Vdcmin), the power (Pmin) is given as 90 W (i.e., for constant torque, the load power is proportional to speed). Hence, from (4), the value of inductance Licmin corresponding to Vdcmin is calculated as

$$Lic_{min} = V\ 2\ dc_{min}/P_{min}(1-d_{min})^2/2f_s \quad (4)$$

The values of inductances Li1 and Li2 are taken less than 1/10th of the minimum critical value of inductance to ensure a deep DICM condition [24]. The analysis of supply current at minimum duty ratio (i.e., supply voltage as 220 V and dc link voltage as 50 V) is carried out for different values of the inductor (Li1 and Li2). Fig. 4 shows the supply current at the input inductor's value as Lic, Lic/2, Lic/5, and Lic/10, respectively. The supply current at higher values of the input side inductor is highly distorted due to the inability of the convertertooperateinDICMatpeakvaluesofsupplyvoltages. Hence, the values of inductors Li1 and Li2 are selected around 1/10th of the critical inductance and are taken as 35 μH. It reduces the size, cost, and weight of the PFC converter.

B.Design Of DC Link Capacitor (Cd)

Thedesignofthedclinkcapacitorisgovernedbytheamount of the second-order harmonic (lowest) current flowing in the capacitor and is derived as follows. For the PFC operation, the supply current (is) is in phase with the supply voltage (vs). Hence, the input power Pin is given as [22]

$$Pin = \sqrt{2}V_S Sin\omega t * \sqrt{2}IS Sin\omega t = V_S I_S(1-Cos2\omega t) \quad (5)$$

wherethelattertermcorrespondstothesecond-orderharmonic, which is reflected in the dc link capacitor as

$$i_C(t) = -V_S I_S V_{dc} Cos2\omega t. \quad (6)$$

The dc link voltage ripple corresponding to this capacitor current is given as [22]

$$\Delta V_{dc} = 1/C_d \int i_C(t)dt = -I_d/2\omega C_d Sin2\omega t. \quad (7)$$

For a maximum value of voltage ripple at the dc link capacitor, Sin(ωt) is taken as 1. Hence, (7) is rewritten as

$$Cd = Id/2\omega\Delta Vdc. \quad (8)$$

Now, the value of the dc link capacitor is calculated for the designed value Vdcdes with permitted ripple in the dc link voltage (ΔVdc) taken as 3% as

$$Cd = Id\,2\omega\Delta Vdc = \frac{Po}{Vdcdes}2\omega\Delta Vdc \quad (9)$$

C. Design Of Input Filter (L_f and C_f)

A second-order low-pass LC filter is used at the input side to absorb the higher order harmonics such that it is not reflected in the supply current. The maximum value of filter capacitance is given as [25]

$$Cmax = Ipeak\,\omega LVpeaktan(\theta) \quad (10)$$

where Ipeak, Vpeak, ωL, and θ represent the peak value of supply current, peak value of supply voltage, line frequency in radians per second, and displacement angle between the supply voltage and supply current, respectively. Hence, a value of Cf is taken as 330 nF. Now, the value of inductor Lf is calculated as follows. The value of the filter inductor is designed by considering the source impedance (Ls) of 4%–5% of the base impedance. Hence, the additional value of inductance required is given as

$$L_f = L_{req} + L_s \Rightarrow 1/4\pi^2 f^2_c C_f = L_{req} + 0.04(1/\omega L)(V^2_s/P_o) \quad (11)$$

where fc is the cutoff frequency of the designed filter which is selected as [25]

$$fL < f c < fsw. \quad (12)$$

Hence, a value of fc is taken as fsw/10. Finally, a low-pass filter with inductor and capacitor of 1.6 mH and 330 nF is selected for this particular application.

V. CONTROL OF PFC BL BUCK–BOOST CONVERTER-FED BLDC MOTOR DRIVE

The control of the PFC BL buck–boost converter-fed BLDC motor drive is classified into two parts as follows.

A. Control Of Front-End PFC Converter:

Voltage Follower Approach The control of the front-end PFC converter generates the PWM pulses for the PFC converterswitches(Sw_1andSw_2)fordclinkvoltagecontrolwithPFCoperationatacmains.Asingle voltage control loop is utilized for the PFC BL buck–boost converter operating in DICM. A reference dc link voltage (V ∗ dc) is generated as

$$V * dc = kv\omega * \quad (13)$$

where kv and ω∗ are the motor's voltage constant and the reference speed, respectively. The voltage error signal (Ve) is generated by comparing the reference dc link voltage (V ∗ dc) with the sensed dc link voltage (Vdc) as

$$V_e(k) = V^*_{dc}(k) - V_{dc}(k) \quad (14)$$

where k represents the kth sampling instant. This error voltage signal (Ve) is given to the voltage fuzzy controller to generate a controlled output voltage (V_{cc}). Finally, the output of the voltage controller is compared with a high frequency sawtooth signal (md) to generate the PWM pulses as For vs > 0; if md <Vcc then Sw_1 = 'ON' if md ≥ Vcc then Sw_1 = 'OFF' For vs < 0; (if md <Vcc then Sw_2 = 'ON' if md ≥ Vcc then Sw_2 = 'OFF').where Sw_1 and Sw_2 represent the switching signals to the switches of the PFC converter.

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B. Control Of BLDC Motor:Electronic Commutation

An electronic commutation of the BLDC motor includes the proper switching of VSI in such a way that a symmetrical

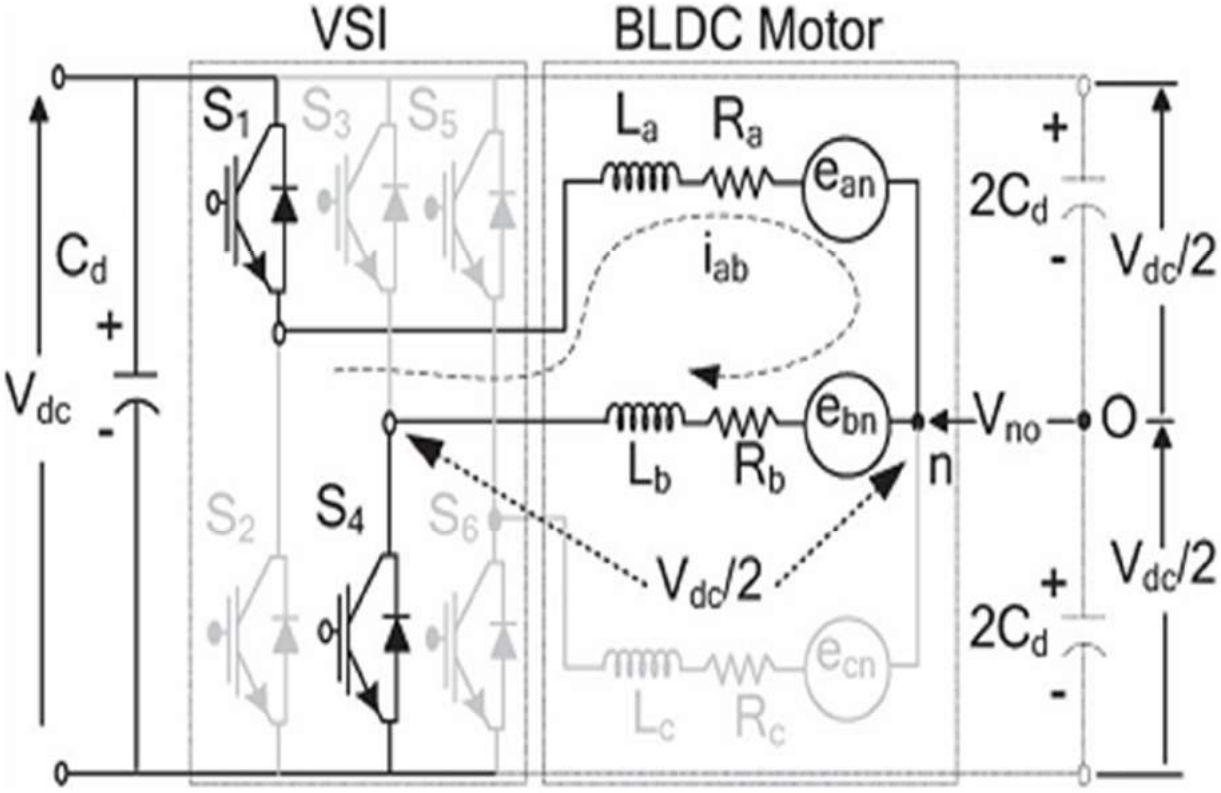

Fig. 4. Operation of a VSI-fed BLDC motor when switches S_1 and S_4 are conducting.

TABLE I SWITCHING STATES FOR ACHIEVING ELECTRONIC COMMUTATION OF BLDC MOTOR BASED ON HALL-EFFECT POSITION SIGNALS

θ (°)	Hall Signals			Switching States					
	H_a	H_b	H_c	S_1	S_2	S_3	S_4	S_5	S_6
NA	0	0	0	0	0	0	0	0	0
0-60	0	0	1	1	0	0	0	0	1
60-120	0	1	0	0	1	1	0	0	0
120-180	0	1	1	0	0	1	0	0	1
180-240	1	0	0	0	0	0	1	1	0
240-300	1	0	1	1	0	0	1	0	0
300-360	1	1	0	0	1	0	0	1	0
NA	1	1	1	0	0	0	0	0	0

dc current is drawn from the dc link capacitor for 120° and placed symmetrically at the center of each phase. A Hall-effect position sensor is used to sense the rotor position on a span of 60°, which is required for the electronic commutation of the BLDC motor. The conduction states of two switches (S_1 and S_4) are shown in Fig. 5. A line current iab is drawn from the dc link capacitor whose magnitude depends on the applied dc link voltage (Vdc), back electromotive forces (EMFs) (ean and ebn), resistances (R_a and R_b), and self-inductance and mutual inductance (L_a, L_b, and v_M) of the stator windings. Table II

showsthedifferentswitchingstatesoftheVSIfeedingaBLDC motor based on the Hall-effect position signals ($H_a - H_c$).

VI. FUZZY CONTROLLER

Fuzzy logic is a fascinating area of research because it does a good job of trading off between significance and precision something that humans have been managing for a very long time. Fuzzy logic is a method of rule-based decision making used for expert systems and process control that emulates the rule-of-thumb thought process used by human beings.

Fuzzy logic requires fuzzy set theory, in which a variable is member of one or more sets, with a specified degree of membership. Fuzzy logic allow us to emulate the human reasoning process in computers, quantify imprecise information, make decision based on vague and in complete data, yet by applying a defuzzification process, arrive at definite conclusions.

The FLC consists of mainly 3blocks

Fuzzification

Inference

Defuzzification

A. Rules

If output is +VE then input is -VE

If input is ZERO then output is ZERO

If output is -VE then input is +VE

A fuzzy controller converts a linguistic control strategy into a repeated control strategy, and fuzzy rules are constructed by expert experience database. Firstly, input voltage V_{dc} and the input reference voltage $V_{dc\text{-}ref}$ have been placed of the angular velocity to be the input variables of the fuzzy logic controller. Then the output variable of the fuzzy logic controller is presented by the control Current *I*max. To convert these numerical variables into linguistic variables, the following seven fuzzy levels or sets are chosen as: NB (negative big), NM (negative medium), NS (negative small), ZE (zero), PS (positive small), PM (positive medium), and PB (positive big) as shown in Figure.

The fuzzy controller is considered as:

For every input and output have Seven fuzzy sets.

Fuzzification using continuous universe of discourse.

Implication using Mamdani's ‘min’ operator;

De-fuzzification using the ‘centroid’ method

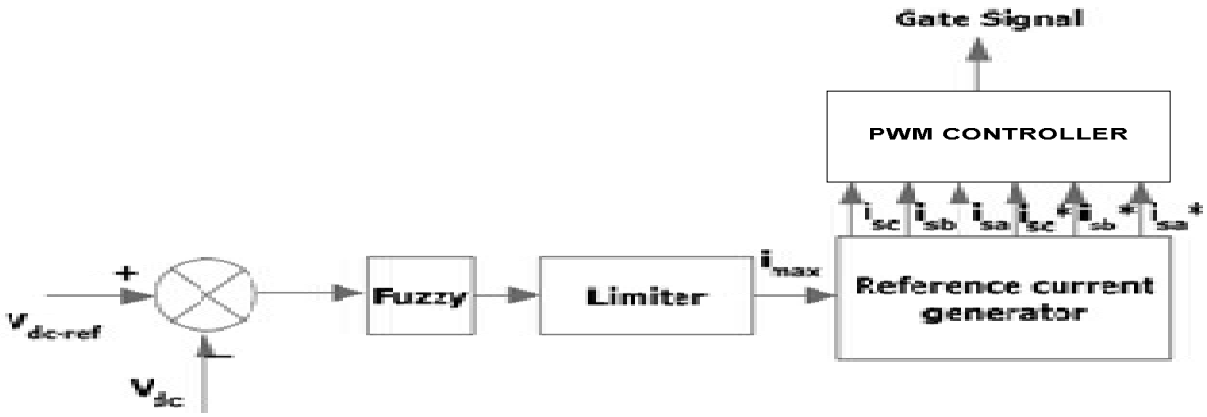

Fig.5.Conventional fuzzy controller

Rule Base: the elements of this rule base table are determined based on the theory that in the transient state, large errors need coarse control, which requires coarse in-put/output variables; in the steady state, small errors need fine control, which requires fine input/output variables. Based on this the elements of the rule table are obtained as shown in Table III, with ‘*Vdc*’ and ‘$V_{dc\text{-}ref}$’ as inputs.

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Table II Fuzzy Rules

Δe \ e	NL	NM	NS	EZ	PS	PM	PL
NL	NL	NL	NL	NL	NM	NS	EZ
NM	NL	NL	NL	NM	NS	EZ	PS
NS	NL	NL	NM	NS	EZ	PS	PM
EZ	NL	NM	NS	EZ	PS	PM	PL
PS	NM	NS	EZ	PS	PM	PL	PL
PM	NS	EZ	PS	PM	PL	PL	PL
PL	NL	NM	NS	EZ	PS	PM	PL

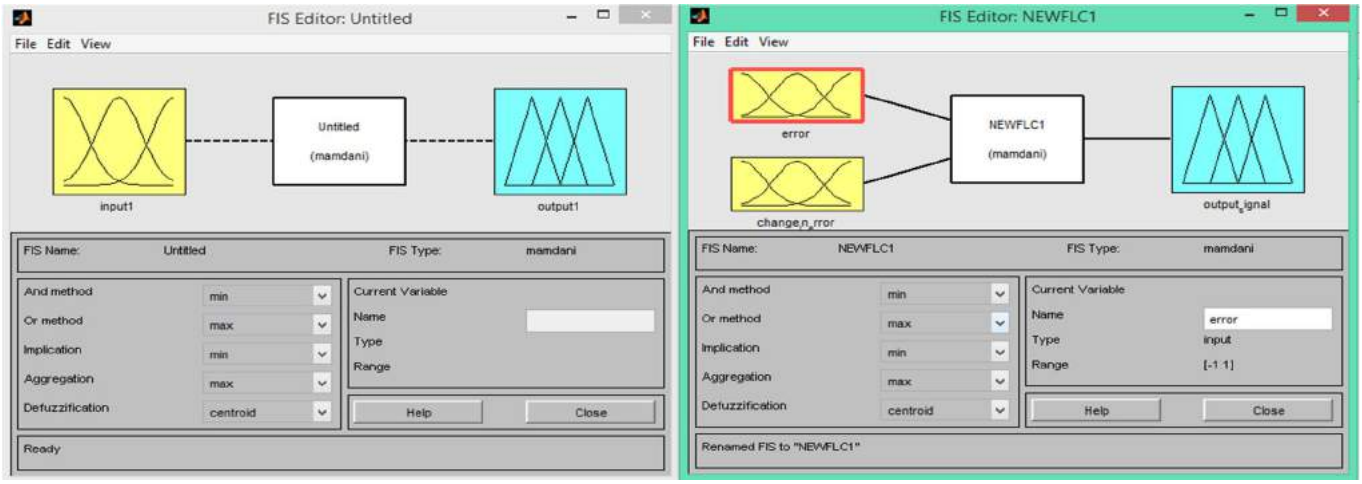

Fig.6. Fuzzy Inputs and Outputs.

VII. SIMULATION RESULTS

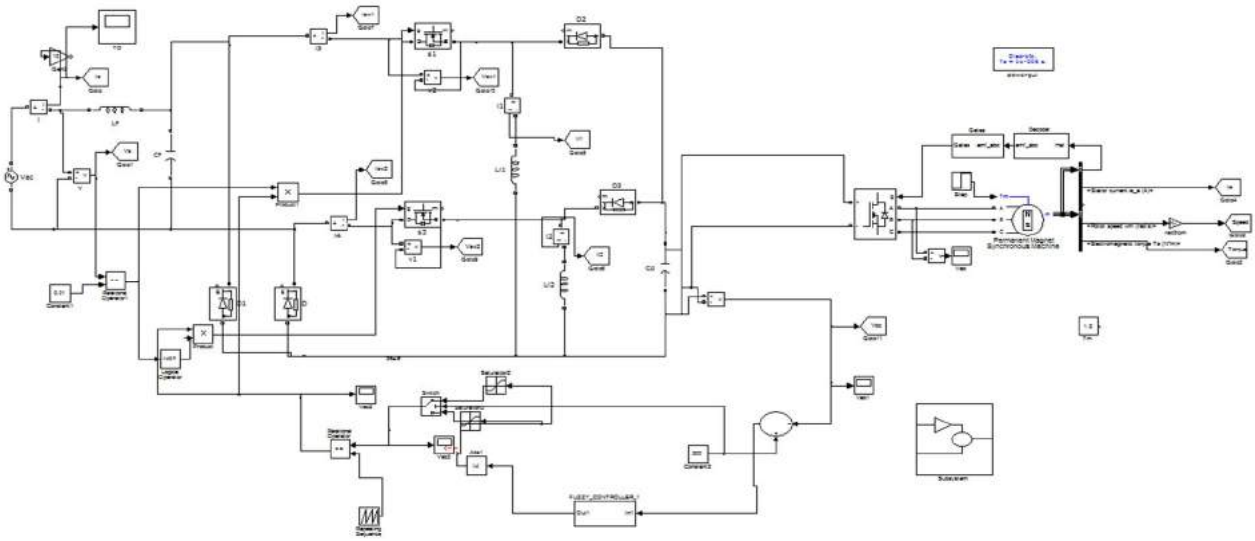

Fig. 7. Simulink ckt of praposed fuzzy logic controller with buck-boost converter fed BLDC motor drive.

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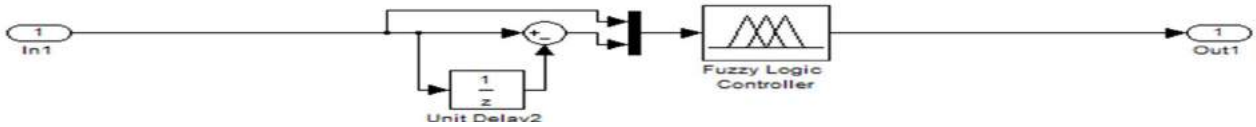
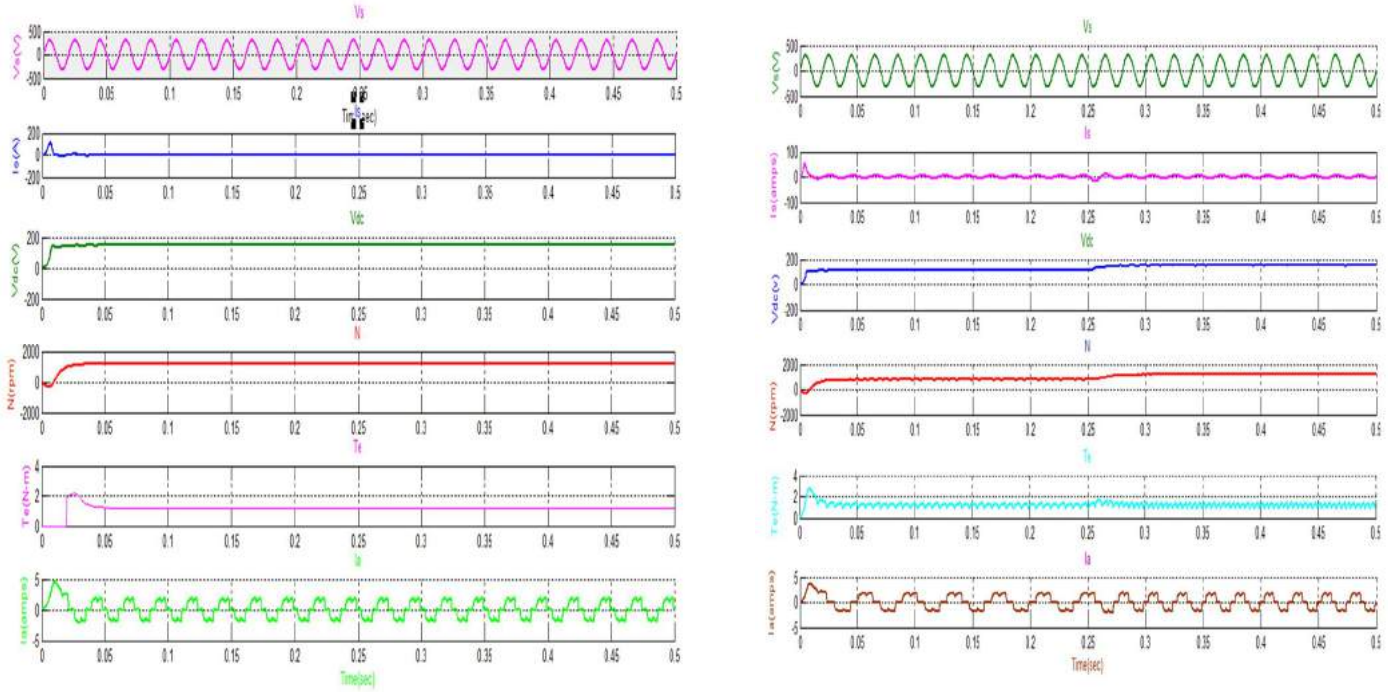


Fig. 8. Simulink fuzzy controller



(a) (b)

Fig. 9. Steady-state performance of the proposed BLDC motor drive at rated conditions. (a) starting, (b) speed control

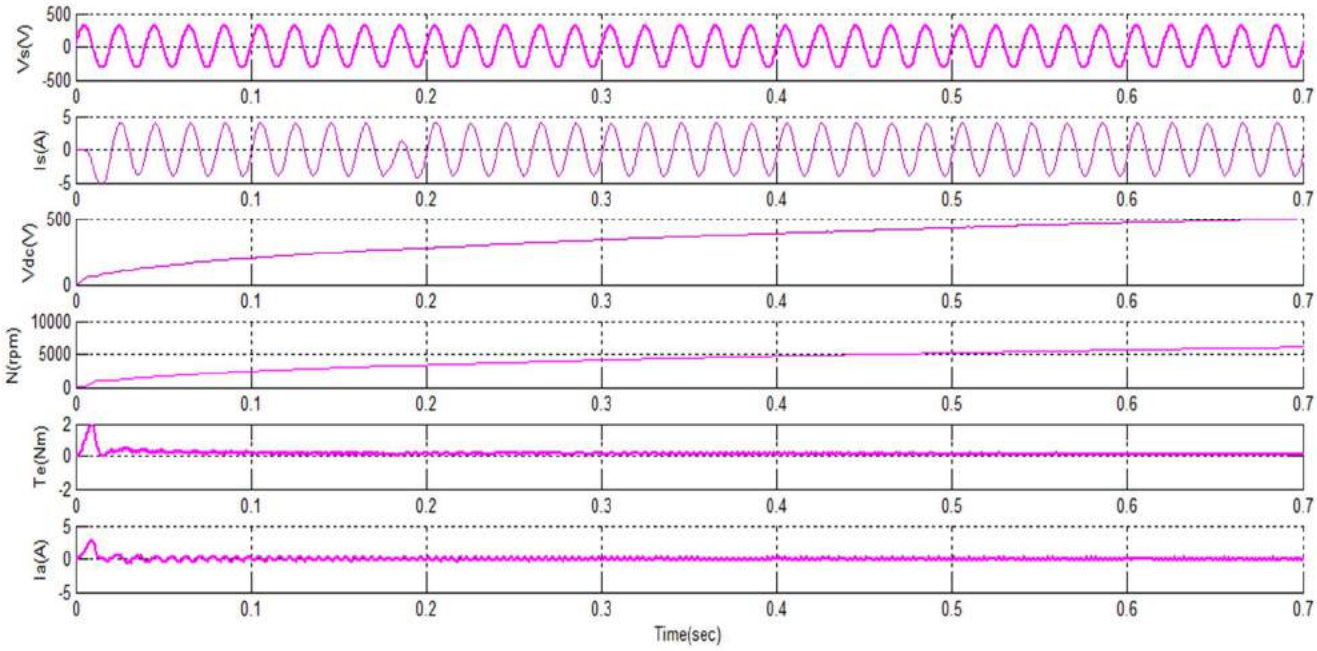


Fig. 10. Dynamic performance of praposed fuzzy logic controller with buck-boost converter fed BLDC motor drive

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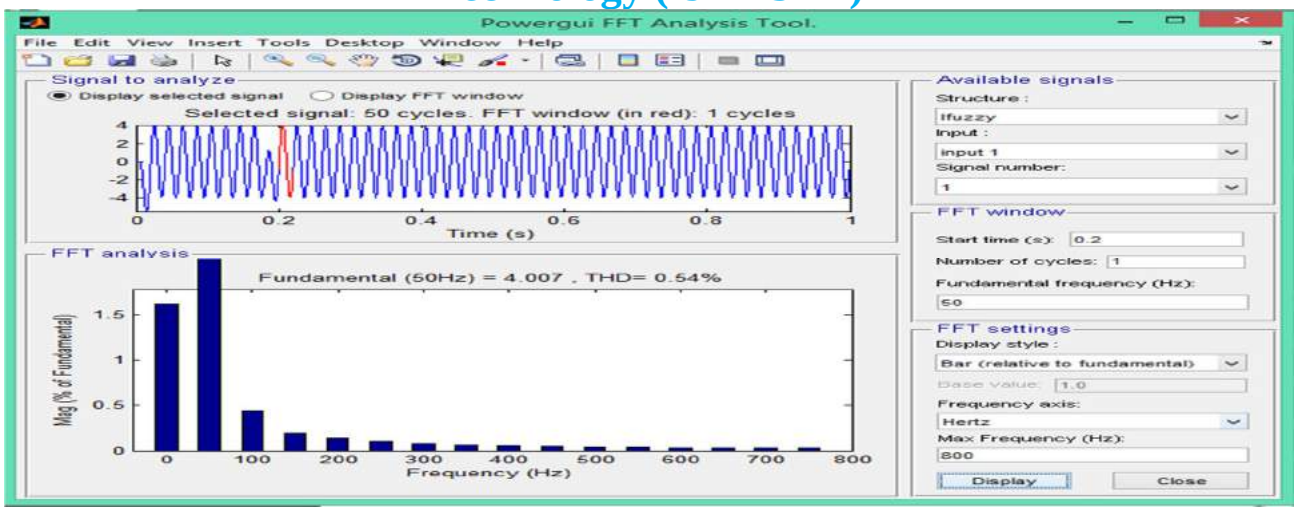

Fig11. % of the Total Harmonic Distortion of Input current.

VIII. CONCLUSION

A new method of speed control has been utilized by controlling the voltage at dc bus and operating the VSI at fundamental frequency for the electronic commutation of the BLDC motor for minimizing the switching losses in VSI. The front-end BL buck–boost converter has been operated in DICM for achieving an inherent power factor correction at ac mains. A satisfactory performance has been achieved for speed control and supply voltage variation with power quality indices within the acceptable limits by useing fuzzy logic controller with reduced THD value is 0.54%. A PFC BL buck–boost converter-based VSI-fed BLDC motor drive has been proposed targeting low-power applications and performance of the proposed drive is simulated in MATLAB/Simulink.

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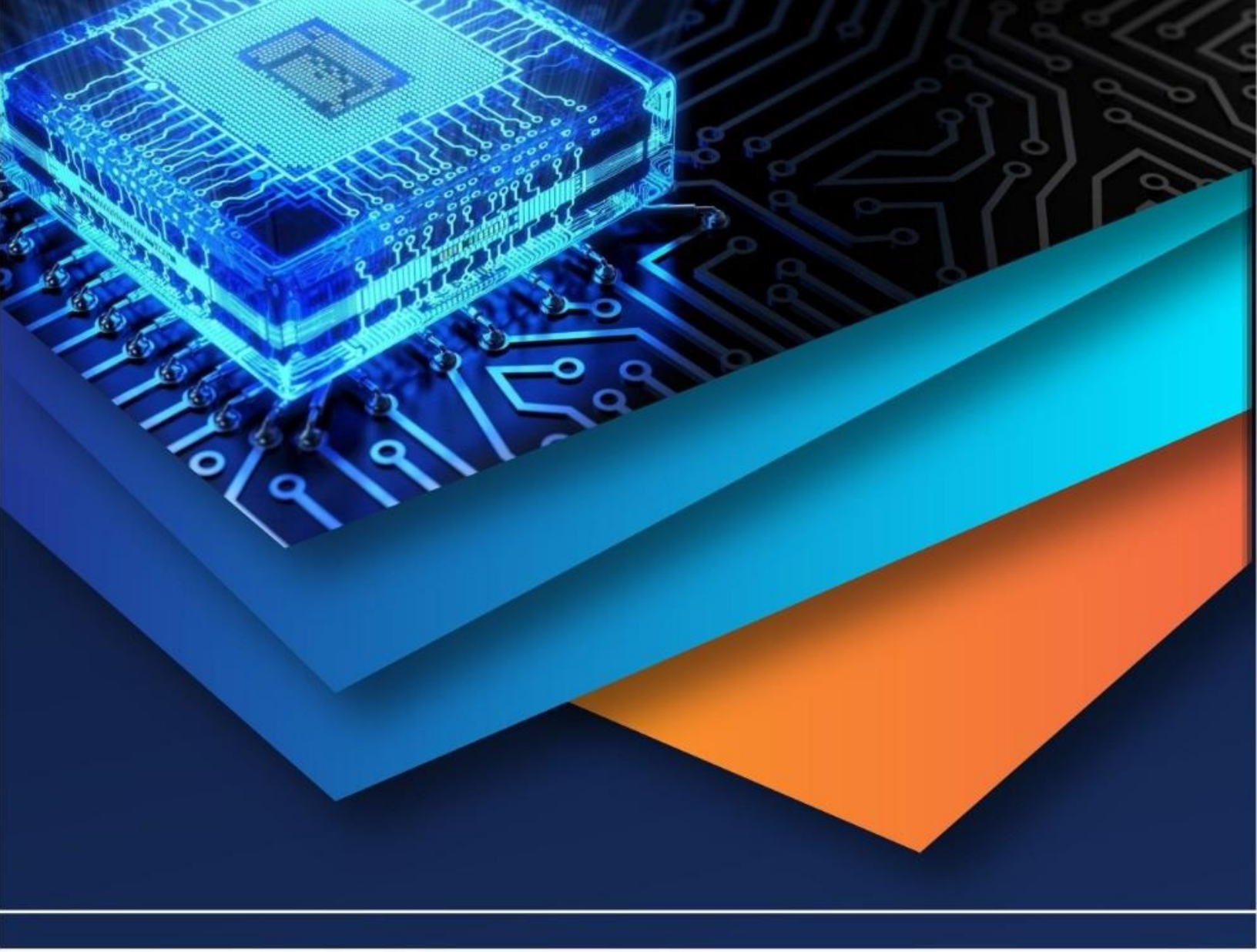

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