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Carrier based PD and POD PWM Technique for MLI

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Abstract: This paper presents the design of gate drive circuit for controlling of multilevel inverter (MLI) with Phase Disposition (PD), Phase Opposition Disposition (POD) pulse width modulation (PWM) switching control technique.
Keywords: POD, PWM, MLI

I. INTRODUCTION

A multilevel inverter (MLI) is a power electronic device which is capable of providing desired alternating voltage level at the output using multiple lower-level DC voltages as an input. Mostly a two-level inverter is used in order to generate the AC voltage from DC voltage. A two-level inverter creates two different voltages for the load i.e., if we provide Vdc as an input to a two-level inverter then it will provide +vdc/2 and –vdc/2 on output. There are several MLI topologies are available three commonly used MLI topologies are:

1) Cascaded H-bridge multilevel inverter
2) Neutral point clamped multilevel inverter
3) Flying capacitor multilevel inverter

MLI have become more attractive due to their advantages over conventional inverters. MLI has main advantages compared with the conventional inverters, the higher voltage capability and the reduced harmonic content in the output waveform due to the multiple dc levels. MLI is now preferred in high power medium voltage applications due to the reduced voltage stresses on the devices. In order, to deliver required voltage and frequency to the load MLI is to be controlled using semiconductor switches. Gating pulses are generated by comparing the reference signal with the carrier wave form. In this method sinusoidal waveform is taken as the reference signal and triangular waveform is the carrier waveform. Gating pulses are generated whenever sine wave value is higher than or equal to the triangular wave value that pass a signal that triggers the gate circuit. Conventional pulse width modulation (PWM) uses one reference waveform and one carrier waveform to generate a gate driving signal. This is the equation used to select the number of carrier waveforms.

Three-level

Carrier waveforms = n-1 where, n= number of levels

Carrier waveforms =2

Selecting three-level as shown in fig.1 and fig.3 simulation results are shown for PODPWM and PODPWM techniques.

A. PDPWM

Three-level as shown see how to generate in MATLAB.

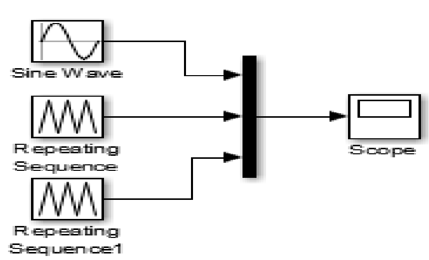

Fig.1 Design model of PDPWM for three-level

In this PD PWM, it requires N-1 number of triangular carriers which are identical and are equally displaced with respect to zero axis as shown in Fig.2.

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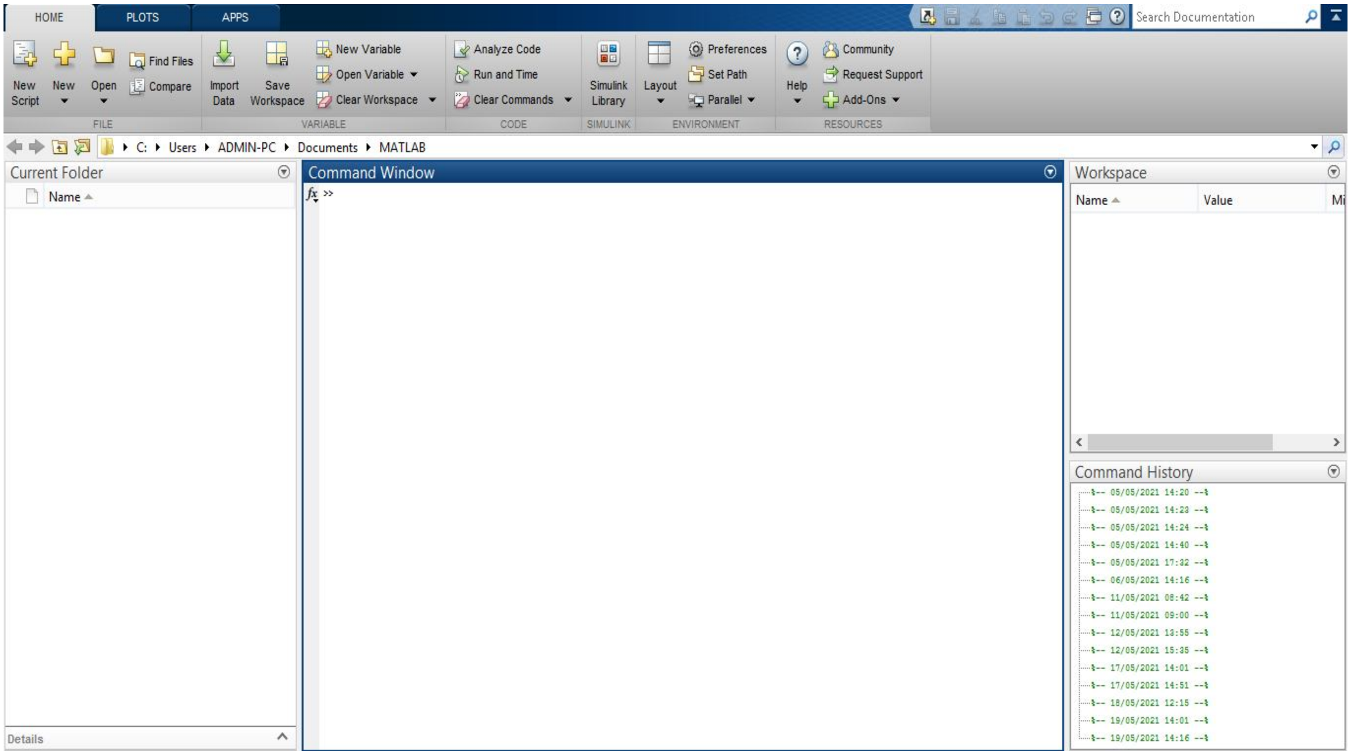
1) STEP-1

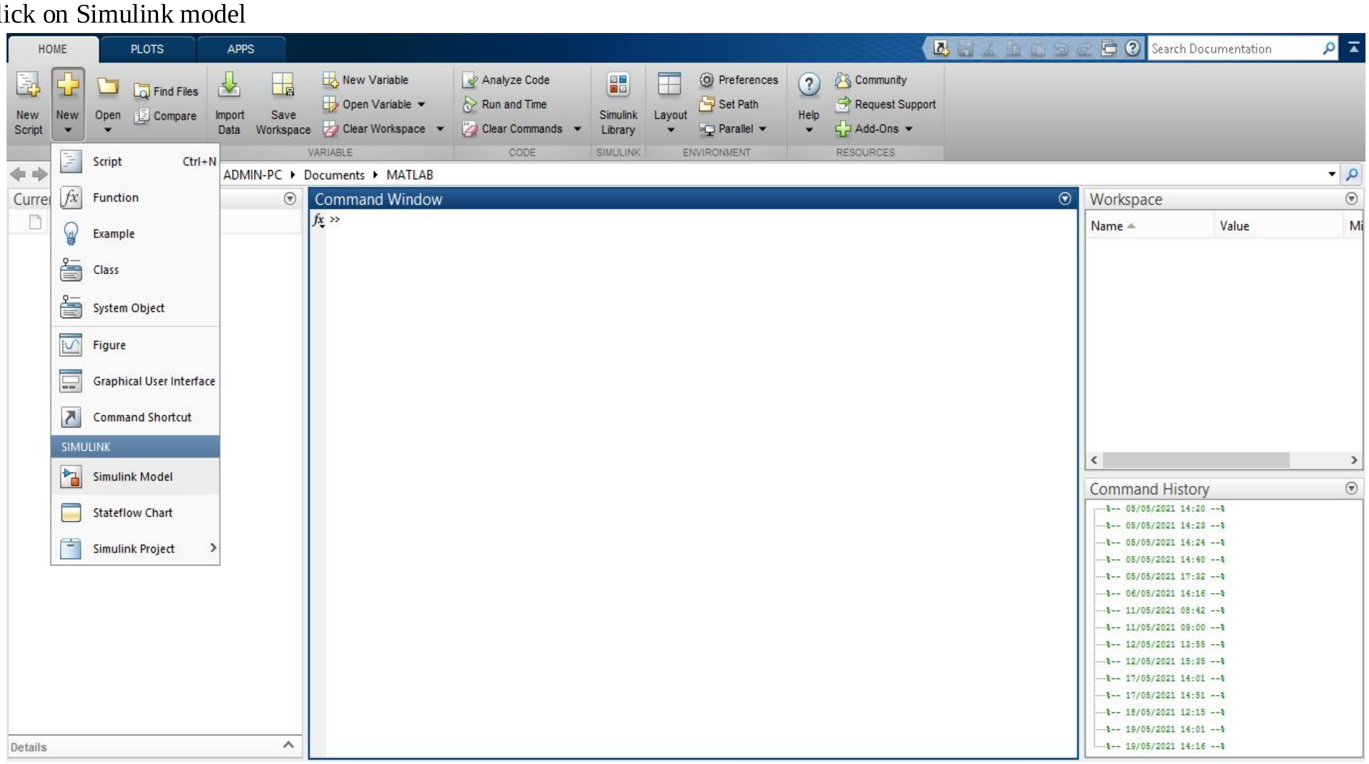
Open click on MATLAB



2) STEP-2

In order, to design a circuit model we have to select the Simulink model.

Click on Simulink model



An untitled Simulink model will be displayed

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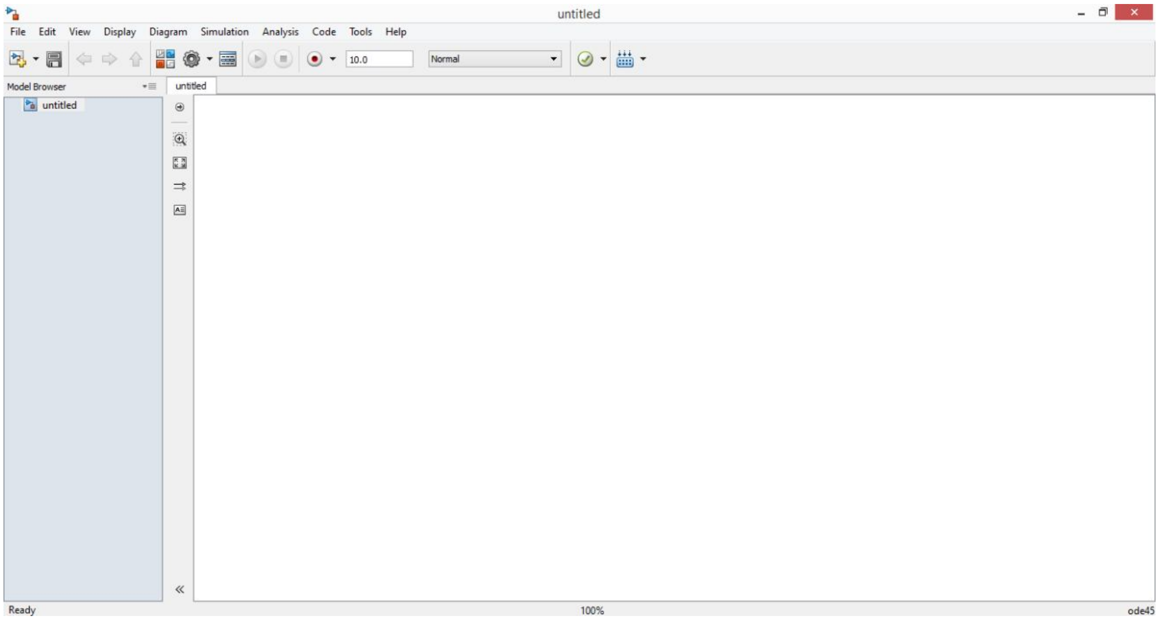
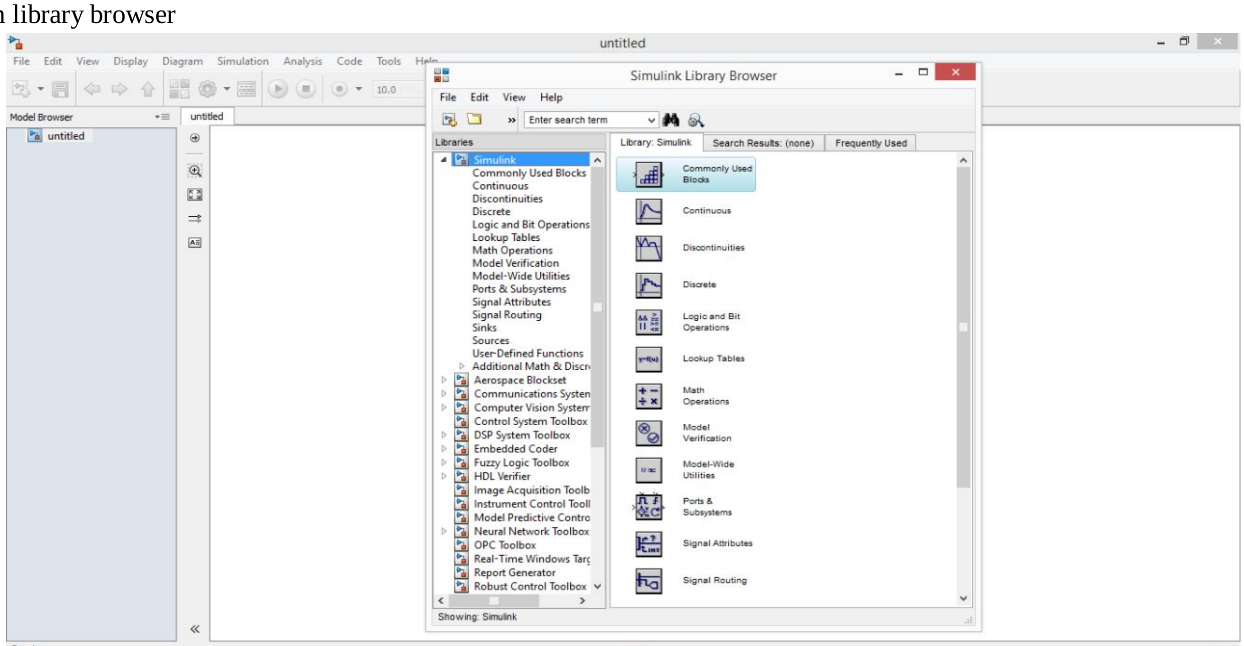


3) STEP-3

Click on library browser



That helps us to search the required component from the library drag or click on add to untitled model for assembling the components.

4) STEP-4

For developing in MATLAB these are the components we need

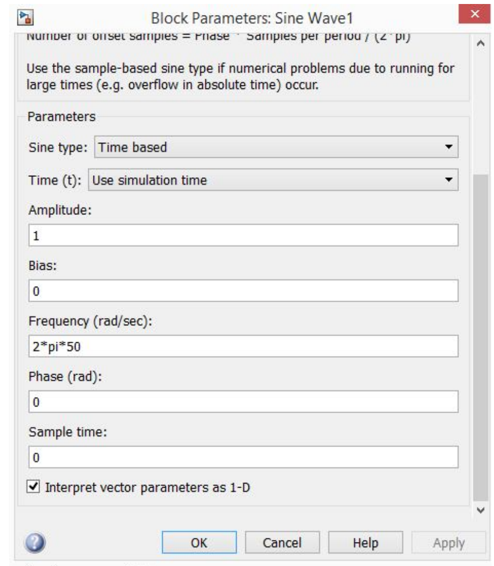
a) Sine wave
b) Repeating sequence
c) Mux
d) Scope
e) Powergui

Assemble as given in circuit.

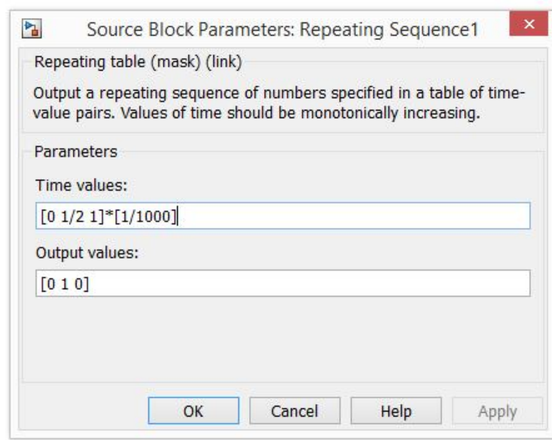
5) STEP-5

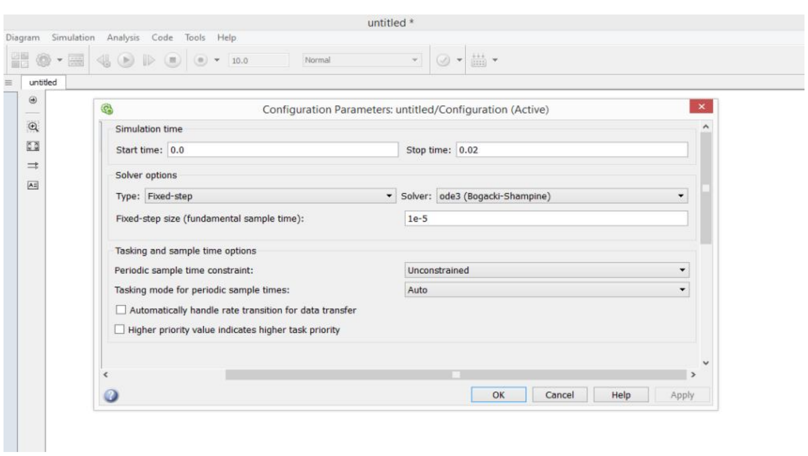
Take these parameter values you can access by double-click on respective component

Sine wave:
Frequency= 2*pi*50



Repeating sequence1:
Time values [0 1/2 1] *[1/1000]
Output values [0 1 0]
Repeating sequence2:
Time values [0 1/2 1] *[1/1000]
Output values [-1 0 -1]





Configuration parameters:
Simulation time:
Start time:0.0 stop time:0.02
Solver options-fixed step size:1e-5
In repeating sequence 1 the output values taken [0 1 0]
In repeating sequence 2 the output values taken [-1 0 -1] as we can see in below waveform.
Those are the limits given for repeating sequence

In repeating sequence 1 the output values taken [0 1 0]

In repeating sequence 2 the output values taken [-1 0 -1] as we can see in below waveform. Those are the limits given for repeating sequence.

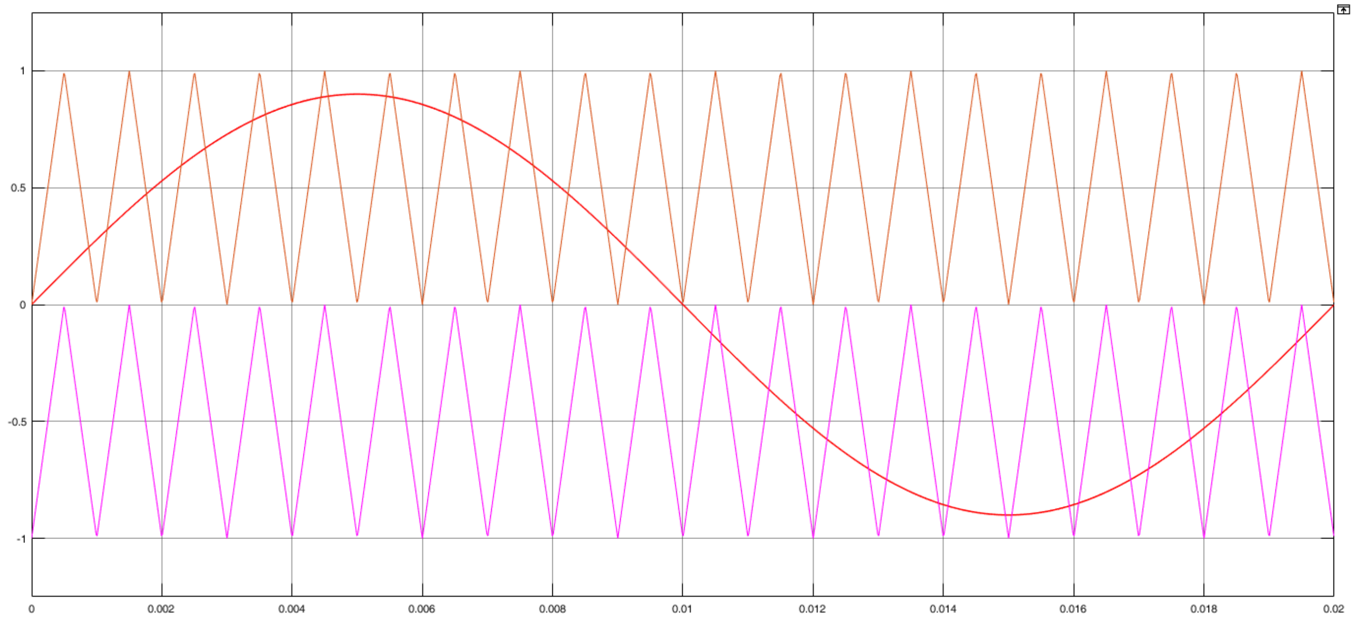


Fig.2 Simulated result of PDPWM for three-level

B. PODPWM

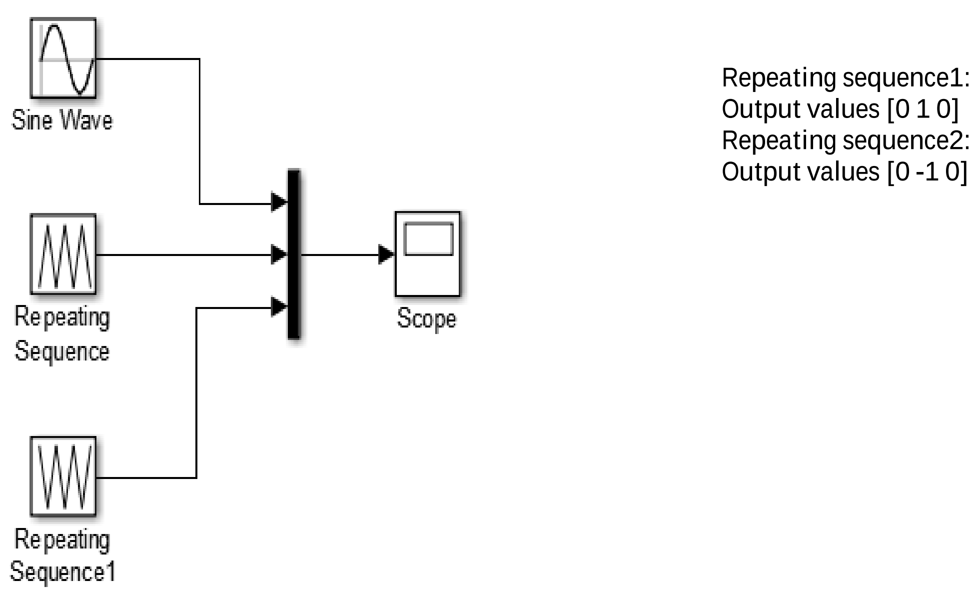


Fig.3 Design model of PODPWM for three-level

In this method, for a ‘k’ level inverter, ‘k-1’ carrier signals are used. In POD-PWM all the carrier signals above X axis are out of phase with the below signals by 180º as shown in Fig.4.

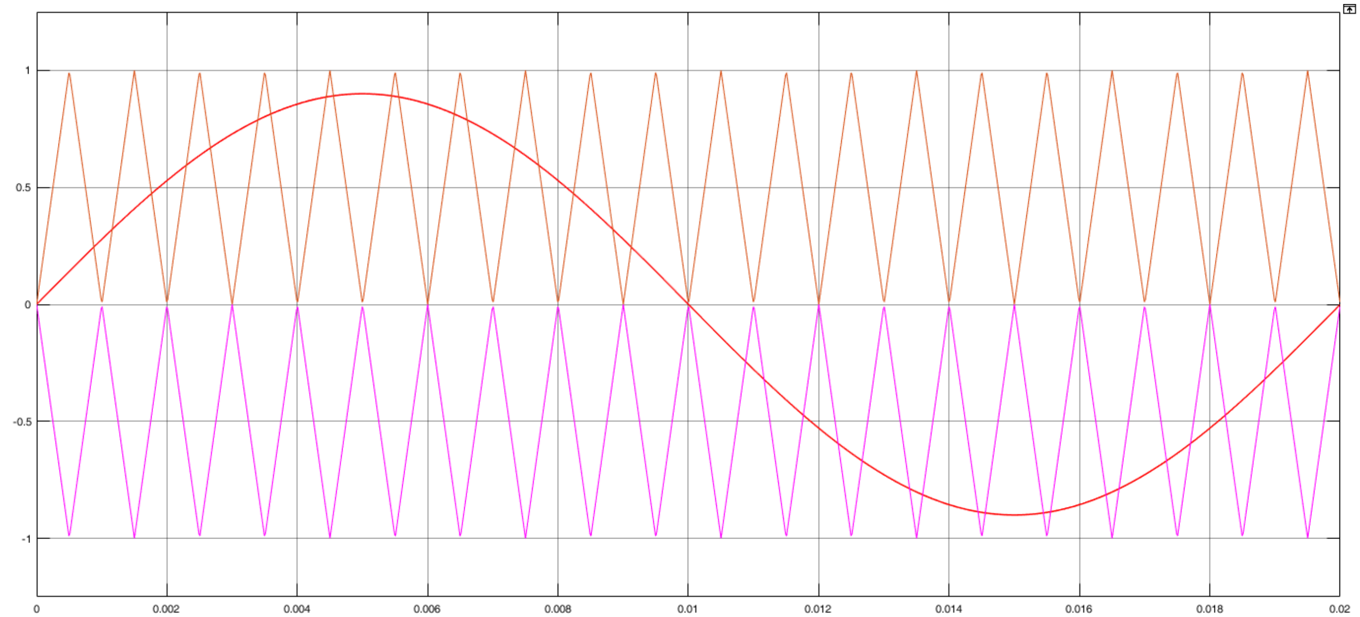


Fig.4 Simulated result of PODPWM for three-level

II. CONCLUSIONS

In this paper PD, POD pulse width modulation techniques used for latest MLI topologies are designed.

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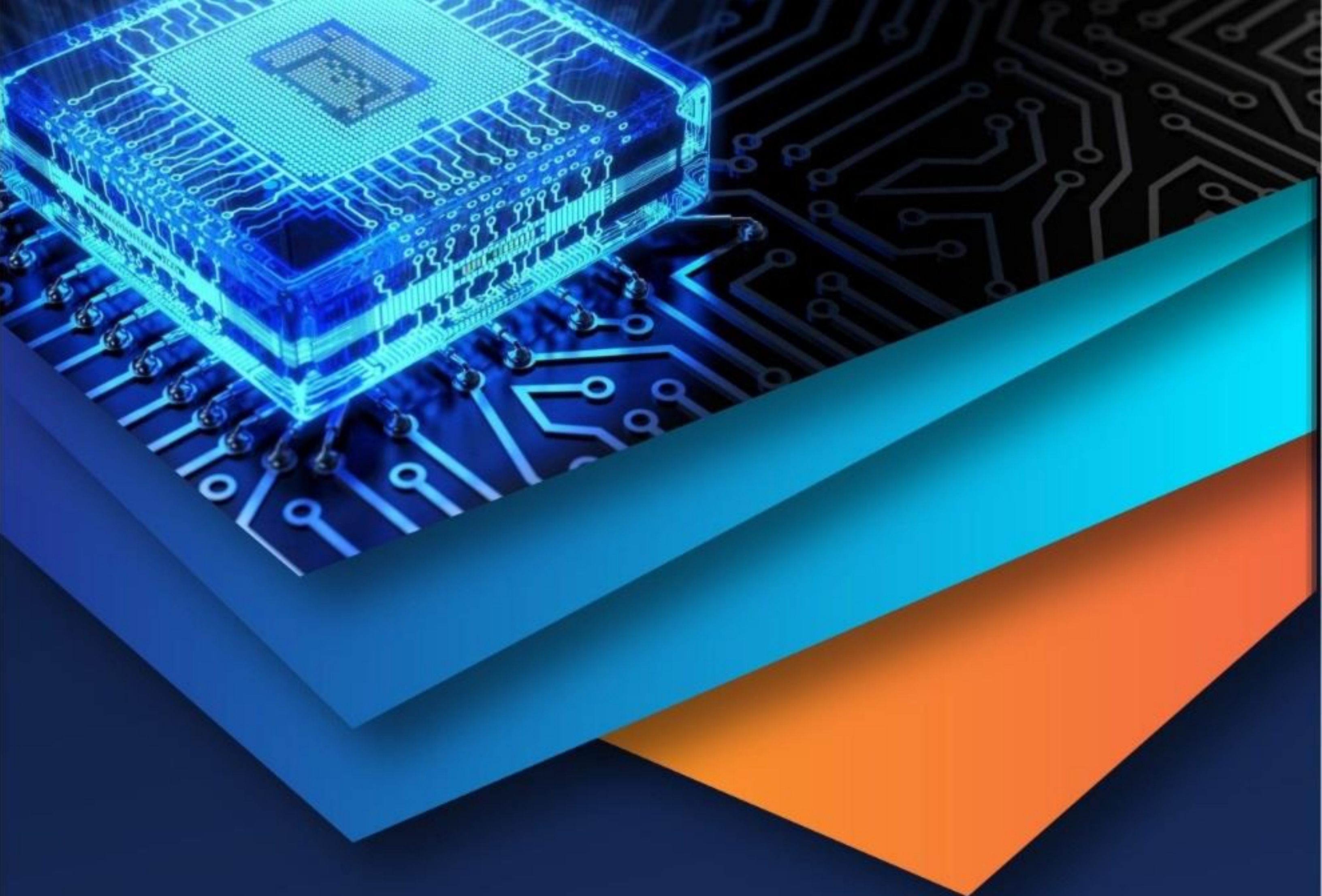

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