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Microcontroller based Automatic Power Factor Correction for Industrial Power use to Minimize Penalty

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Abstract: In this proposed system, two zero crossing detectors are used for detecting zero crossing of voltage and current. The project is meant to attenuate penalty for industrial units using automatic power factor correction unit. The microcontroller utilized during this project belongs to 8051 family. The interruption between the zero-voltage pulse and zero-current pulse is duly generated by suitable operational amplifier circuits in comparator mode is fed to 2 interrupt pins of a microcontroller. The program takes over to actuate appropriate number of relays from its output to bring shunt capacitors into load circuit to urge the facility factor till it reaches near unity. The capacitor bank and relays are interfaced to the microcontroller employing a relay driver. It displays delay between this and voltage on an LCD. Furthermore, the project is enhanced by using thyristor control switches rather than relay control to avoid contact pitting often encountered by switching of capacitors because of high in rush current.
Keyword: Power factor, AT89S51, LCD

I. INTRODUCTION

The power factor of an electrical system gives the thought about the efficiency of the system to do useful work of the supplied electrical power. A low power factor results in increase in losses and also draws penalty by the utility. Modern industries using mechanized methods suffers from low power factor because of the utilization of various electric equipment which needs more reactive power. Significant savings in utility power costs are often realized by maintaining a mean monthly power factor near unity. Utilizing shunt capacitor banks for Power Factor Correction is an exceptionally established methodology. The recent trend is to automate the switching procedure of capacitors to urge greatest advantage in real time basis. Embedded systems supported microcontrollers are often won't to monitor and control the switching of correction devices due to its dependability and execution.

II. MOTIVATION

Electricity plays an important role in almost all industries. Without it, it would be hard or nearly impossible for small and medium scale industries to do their task. But since these industries are often located at the end of the grid and operated with the use of heavy machines, they are particularly susceptible to power issues. With the constantly increasing cost of energy, these industries are struggling to get off the mark in the market. Retaining the power quality is crucial in industries to maximize production and avoid any technical problems while lowering energy cost. In the industries, any power factor over 0.95 is accepted and considered to be an efficient use of energy. The typical uncorrected power factor for a medium scale industry ranges from 0.65 to 0.8. Increase of power factor close to unity reduces penalty on the firm imposed by electrical companies. Therefore suitable correction equipment must be designed to monitor the system power factor and make the necessary improvement when it goes underneath the specified limit set as per the standards.

III. OBJECTIVES

The primary objective of the project was to design correction equipment which can monitor the power factor of an electrical load and enhance the power factor to a desired value. The research investigations were carried out with the following objectives.

A. Design a microcontroller based correction equipment to improve the power factor of the system to desired value of greater than 0.95.
B. Implement the system and monitor different electrical load models and diverse load patterns to verify the result.

IV. DESIGN METHOD

The Automatic Power Factor correction device is developed built on embedded system having 89S52 at its core. The voltage and current signal from the system is sampled and taken as input where the difference between the arrivals of wave forms indicates the phase angle difference. The difference is measured by the internal timer and calibrated as phase angle to calculate the corresponding power factor. The system power factor is compared with the desired level and the difference is measured for switching of required number of capacitors from the bank. The values of power factor and phase lag are shown on a display for convenience.

V. BLOCK DIAGRAM

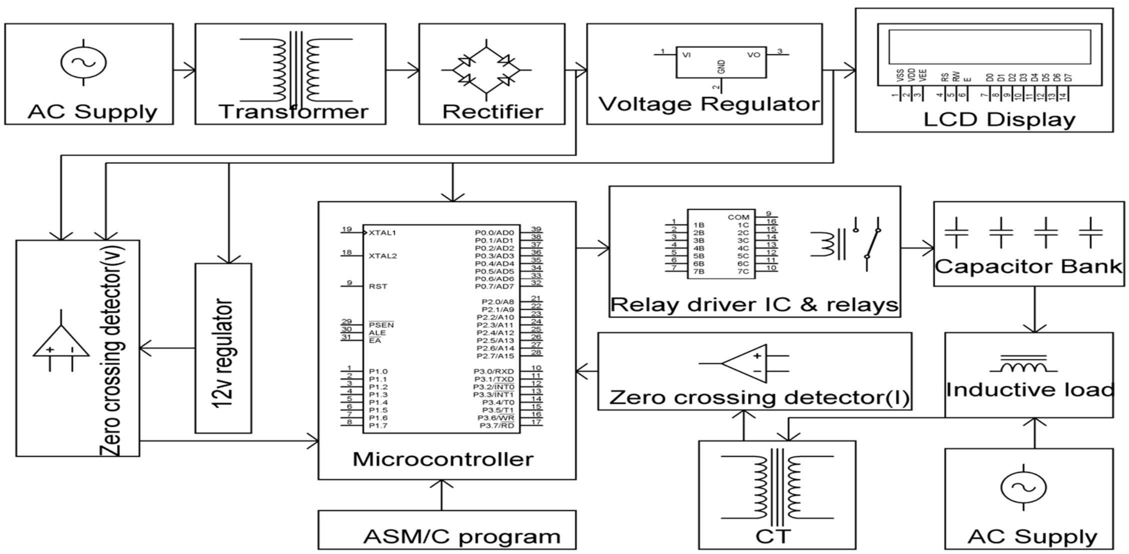
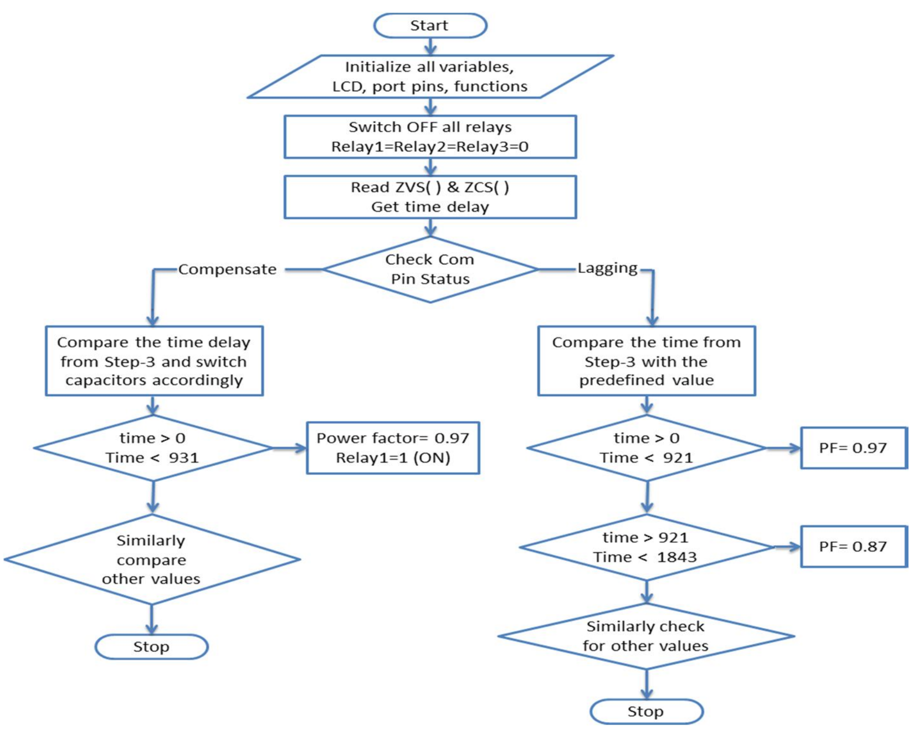


Fig 1: Block Diagram of the Connection Equipment

VI. FLOWCHART



VII. CIRCUIT DIAGRAM

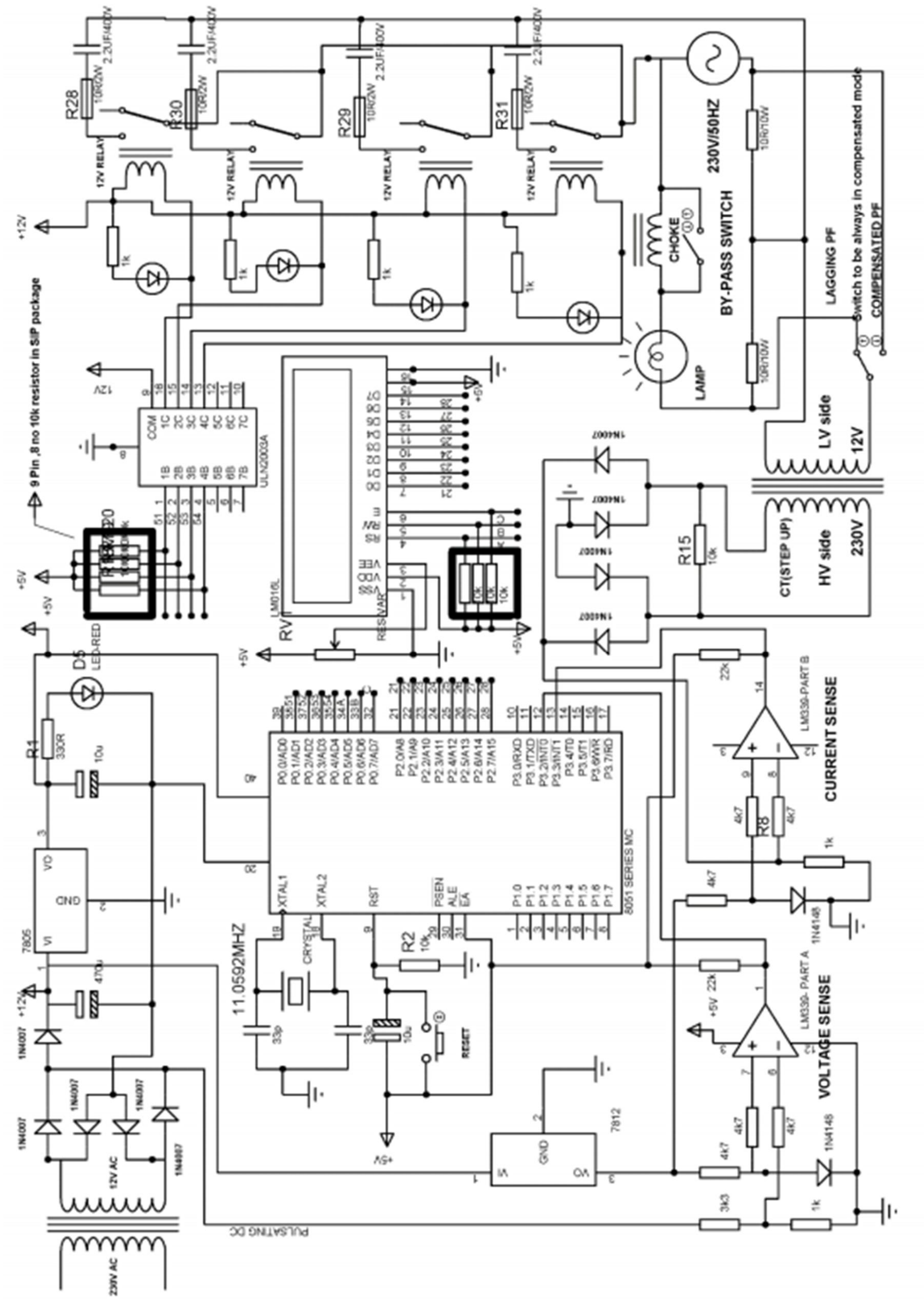


Fig 2: Complete Circuit Diagram for the Correction Equipment

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VIII. ALGORITHM

1) *Step-1:* Take input for voltage and current in the circuit.
2) *Step-2:* Measure the phase lag and calculate the power factor.
3) *Step-3:* Differentiate from the targeted power factor and calculate the reactive power requirement.
4) *Step-4:* Turn ON or OFF appropriate number of capacitors from capacitor bank depending on reactive power supplied by each step.
5) *Step-5:* Again compare the power factor with targeted PF and continue from step-1.

IX. RESULTS

A. Analysis Of Load Without Correction

The analysis of the pure restive load (R Load) and series resistive-inductive loads (Series R-L Load) was avoided using the correction equipment. The designed loads were connected through the PG08 power guard and the readings for different electrical parameters were recorded.

Sl.no	Load Type	Delay(ms)	Power Factor	Remarks
1	Pure R	0	0.99	No Correction Required
2	Series R-L	3.21	0.73	Correction Required

Table 1: Load Analysis without Correction

B. Analysis Of Load With Correction

As there's a requirement for power factor improvement for Series R-L load they were connected to the supply together with the correction equipment designed to verify the expected correction. The correction equipment is plugged in to the PG08 power guard and therefore the loads are connected to the output point of the equipment. All the three loads designed were tried and therefore the observed values were recorded.

Series R-L Load

	No Capacitor	One Capacitor	Two Capacitors	Three Capacitors
Delay(ms)	3.21	1.67	0.00	2.45(leads)
Power Factor	0.53	0.87	1.00	0.72
Improved Power Factor	0	0.31	0.38	0.1

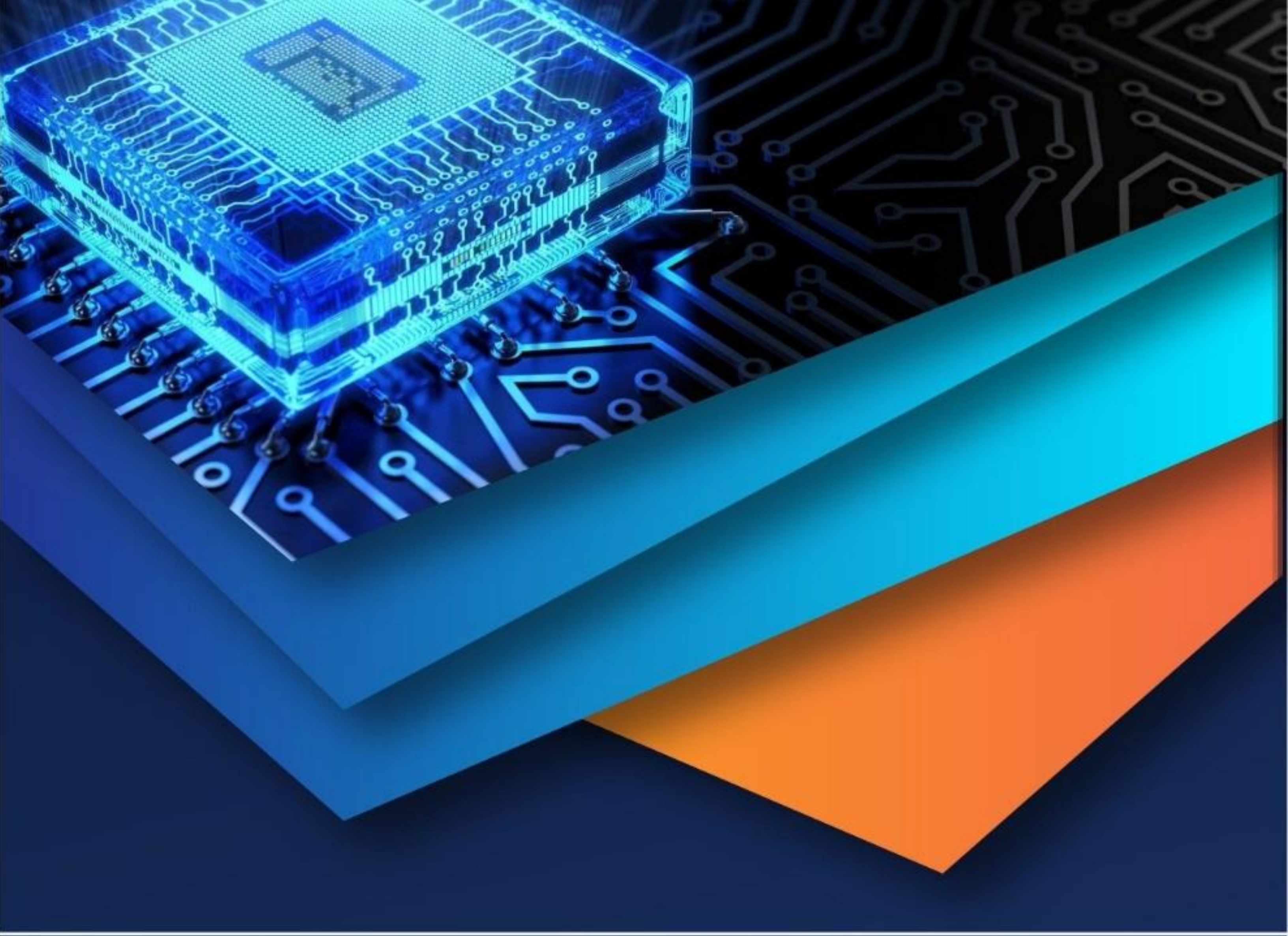
Table 2**:** Load Analysis with Correction

X. CONCLUSION

Power factor correction equipment designed based on microcontroller and capacitor banks was used for measurement and monitoring of modelled electrical load and therefore the following deductions were obtained. The power factor correction device designed had improved the power factor from 0.73 to 0.95 under the test load conditions. With the right amount of reactive power compensation, the system capacity is released as there's a decrease in current drawn. The designed equipment was studied within the laboratory scale; it can be implemented in the industries with proper protection to verify the operation during a real time environment. In automatic PF correction, if the load is changing frequently, the numerous switching of capacitor bank may cause harmonic problem. Suitable filter design also as an optimum algorithm design are often done based on the frequent load change pattern to avoid regular switching of capacitor bank.

REFERENCES

[1] McGill, T., Power Factor Correction, Eaton Corporation, 2007, pp. 24-26.
[2] Institute of Electrical and Electronics Engineers. The authoritative dictionary of IEEE standards terms. Standards Information Network, Std. 100, IEEE Press, 2000.
[3] Power Factor Correction Explained, Available at: http://www.lexelectrix.com/index.php, Accessed on: April 27, 2015.
[4] Saied, M. M., Optimal Power Factor Correction, IEEE Transaction on Power Systems, 1988, pp. 844-851.



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