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Thermal Management and Parametric Study of Flip Chip BGA using Finite Element Methods

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Abstract: ***More component density in electronic boards, more speed of VLSI circuits have led to more power dissipation of the electronic devices. Dramatic increase of applications of such circuits and devices, urges the thermal analysis and power management studies of such systems a vital design requirement. The amount of dissipated power by the chip is directly related to its temperature which is a crucial parameter in electrical behavior of electronic components, circuit performance, and reliability of the electronic system. Thermal analysis is an important part of modern electonic design thus that enables the designer to calculate the critical thermal variables as key factors in electrical analysis. There are three levels of thermal analysis: component, package or system level. In this study thermal management at each of these levels is analysed and a parametric study of the material properties and geometry of various components of the flip chip package were analysed to reduce the Junction temperature*** T_j

Keywords: Thermal management, Non-uniform power maps, FCBGA, IHS, TIM, Junction temperature, Ansys workbench.

I. INTRODUCTION

Electronic packages are interconnectable housings for semiconductor devices. The major functions of the electronic packages are to provide electrical interconnections between the IC and the board and to efficiently remove heat generated by the device. Feature sizes are constantly shrinking, resulting in increased number of transistors being packed into the device. In order to keep pace with these new advancements in silicon technologies, semiconductor packages have also evolved to provide improved device functionality and performance. Flip chip Ball Grid Array (FCBGA) packages have evolved as a most promising packing option for meeting the demands of miniaturization while offering improved performance. It replaces the peripheral bond pads of traditional wire bond interconnect technology with area array interconnect technology at the die/substrate level. A flip chip utilizes conductive heat bumps which are placed directly on the area array pads of the die surface to provide connectivity.

With chip size getting smaller and circuit densities at their highest levels, the amount of heat generated in the circuits is very significant. Heat has to be removed from the device to ensure that the device is maintained within its functional and maximum design temperature limits. The reliability of an electronic package is also affected by the high operating temperature of the device caused by the combination of ambient conditions and device power dissipation. High temperature rises can possibly cause catastrophic failure as well as long term degradation in the chip and package materials both of which eventually lead to failure. Most of FCBGA devices are designed to operate reliably within specified die temperature. To ensure this condition is met, thermal modeling is used to estimate the performance and capability of IC packages. Thermal resistance of the constituent components is the primary parameter that indicates the heat dissipation of the electronic package. Many researches have been carried out to measure and minimize the thermal resistance of the constituent components of the electronic package. This can be obtained by experimentation of a thermal test chip or by using simulation and modeling tools like Finite element methods (FEM) or computational fluid dynamics (CFD). Thermal performance of TIM, impact of cooling fans on a FCBGA were simulated and correlated with experimental data [1]. CFD Analysis of an Integrated circuit chip with non-uniform power was carried out and its thermo-mechanical properties were evaluated [2]. Impact of heatsink tilt, increase in TIM thickness on thermal performance for Bare die, Molded and Lidded FCBGA was experimentally determined [3]. Improving the thermal performance of a FCBGA using a metal cap as a heat sink in comparison to bare die was obtained by finite element methods as well as determined experimentally [4]. Non-uniform power distribution occurs when the core processor region of the die dissipates a significant fraction of the total power while the other regions of the die dissipate little power. This non-uniformity results in hot spots and large temperature gradient. The aim of this paper is to establish the impact of non-uniform power distribution on the thermal performance of the Integrated circuit (IC). Various thermal performance parameters that cause better heat dissipation and bring uniformity in the surface temperature of the IC components are studied.

A three dimensional Finite Element Model (FEM) is established with uniform and non-uniform power loading. A steady state thermal analysis is performed and the results are used to understand the impact of non-uniform power loading, design parameters such as XX, YY and material properties of the heat sink, Integrated Heat sink (IHS) and Thermal interface material (TIM) on the thermal performance of the FCBGA.

II. FLIP CHIP BGA PACKAGES

Flip chip is a packaging interconnect technology that replaces peripheral bond pads of traditional wirebond interconnect technology with area array interconnect technology at the die/substrate interface. The bond pads are either redistributed on the surface of the die or in some very limited cases, they are directly dropped from the core of the die to the surface. Because of this inherent distribution of bond pads on the surface of the device, more bond pads and I/Os can be packed into the device

Unlike traditional packaging technology in which the interconnection between the die and the substrate is made possible using wire, flip chip utilizes conductive bumps that are placed directly on the area array pads of the die surface. The area array pads contain wettable metallization for solders (either eutectic or high lead) where a controlled amount of solder is deposited either by plating or screen-printing. These parts are then reflowed to yield bumped dies with relatively uniform solder bumps over the surface of the device. The device is then flipped over and reflowed on a ceramic or organic laminate substrate. The solder material at molten stage is self-aligning and produces good joints even if the chips are placed offset to the substrates. After the die is soldered to the substrate, the gap (standoff) formed between the chip and the substrate is filled with an organic compound called underfill. The underfill is a type of epoxy that helps distribute stresses from these solder joints to the surface of the whole die and hence improve the reliability and fatigue performance of these solder joints. This interconnect technology has emerged in applications related to high performance communications, networking and computer applications as well as in consumer applications where miniaturization, high I/O count, and good thermal performance are key attributes

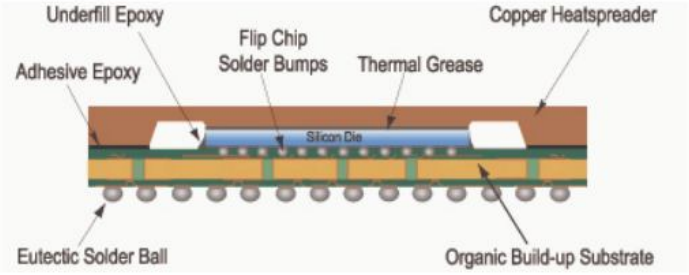


Fig. 1 Flip Chip Package

The device is then flipped over and reflowed on a ceramic or organic laminate substrate. Molten solder then forms a joint with the substrate. The gap between die and the substrate is filled with an organic compound called underfill. The underfill is usually epoxy resin. The underfill upon curing becomes hardened and exhibits high modulus and low coefficient of thermal expansion matching with that of solder joint and good adhesion towards the chip and substrate. An underfill also increases the fatigue life of a solder joint and also protects the die and solder joint from environmental conditions. An IHS attached above the die helps in spreading and dissipation of heat. Copper is commonly used material for IHS. TIM a thermal conductive material is used to provide physical contact between die and the IHS. Thermal Grease is the commonly used material. It has thermal resistance ranging from $0.1cm^{2o}C/W$ to $0.55cm^{2o}C/W$ and thermal conductivity less than 6W/m K.

III. THERMAL MANAGEMENT OF THE PACKAGE

Heat generated in the electronic package can be removed by passive methods like conduction, convection or radiation. At the The resistance to flow of electrical current through the leads, poly-silicon layers and transistors comprising a semiconductor device, results in significant internal heat generation within an operating electronic component. In the absence of some heat removal mechanisms the temperature of the components would rise and finally fail. So thermal management becomes a vital part in electronic packaging. Despite the wide variety in size, power dissipation and sensitivity to temperature, the thermal management of all microelectronic components is motivated by similar concerns and common hierarchy of design constraints. The prevention of catastrophic failure – an immediate and total loss of electronic function and package integrity – is the primary and foremost aim of electronic thermal control. Thermal management in packaging may employ different modes of heat transfer at different levels.

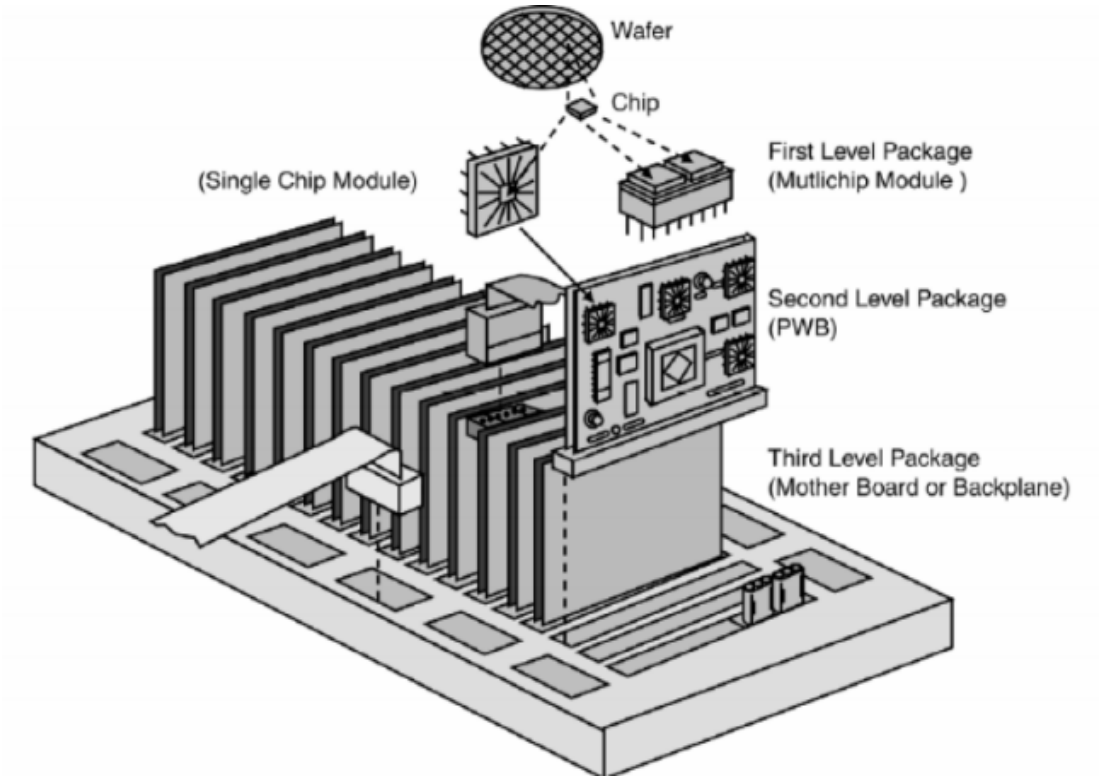


Fig. 2 Packaging Hierarchy

A. Device Level Cooling

The chip package which houses and protects the chip forms the bottom of the packaging hierarchy or first level or device level. Thermal management at this level is primarily concerned with conducting heat form the chip to the package surface and then into the printed wiring board. At this packaging level, reduction of the thermal resistance between the silicon die and the outer surface of the package is the most effective way to lower the chip temperature. The thermal resistance can be brought down by number of ways. Improved thermal performance can be obtained by using die-attach adhesives with high thermal conductivity fill materials, thermal greases, phase change materials which soften at the operating temperature to better conform to the surface of the chip and metal plate heat spreaders. The cooling can be enhanced by attaching the package to heat sink, heat pipes etc., and cooling it by either by natural convection or forced convection.

B. Package Level Cooling

In this level, heat is removed both by conduction in PWB and by convection to the ambient air. Use of printed wiring board with thick, high conductivity power and ground planes or embedded heat pipes, provides improved thermal spreading at this level of packing. Heat sinks are often attached to the back of printed wiring board. There are many systems where convective cooling is not possible; instead, heat must be conducted to the edge of the PWB. Attachment of heat sink or a heat exchanger at this edge then serves to remove the accumulated heat.

C. System Level Cooling

At system level it involves the use of active thermal control measures, such as air handling systems, refrigeration systems or heat pipes heat exchangers and pumps. Based on the application it is possible to cool the rack or module by relying on natural circulation of heated air. Accurate thermal analysis of a complex electronic system including several packages, discrete elements, printed circuit boards, connectors and mechanical parts, heat sinks and cooling mechanisms, and covering cases is almost impossible with currently available thermal simulation software, because of its complexity and the large number of thermal characteristics and the excessive amount of unnecessary information carried in the output of the analysis. The alternative solution is to separately, generate the compact model of packages, boards, and other parts of the system and use them as the building blocks of the thermal model of the system. This system level model is then used to generate the thermal variables at the desired locations within the system.

IV. FINITE ELEMENT METHOD

A Three dimensional model of the FCBGA is modeled using Ansys workbench. Table 1 specifies the dimensions of the FCBGA Package considered. Table 2 shows the material properties of the constituent components of the FCBGA.

TABLE I
DIMENSIONS OF COMPONENTS

Component	Dimension(mm)
Substrate	60x60x1
Epoxy-solder	25x25x0.05
Die	25x25x0.75
TIM-1 (between Si and IHS)	25x25x0.15
IHS	25x25x2
TIM-II (between IHS and HS)	25x25x0.15
Heat sink	100x100x2

TABLE III
MATERIAL PROPERTIES OF COMPONENTS

Item	Thermal Conductivity (k in W/m/^{o}c)		
	k_x	k_y	k_z
Substrate	40	40	1.5
Epoxy solder	0.3	0.3	2.5
Die	120	120	120
TIM-I,II	3	3	3
IHS	401	401	401
Heat sink	401	401	401

A. Geometry Creation

A 3-D model of FCBGA was modelled in Ansys workbench. The following components from top to bottom were considered for the analysis with the dimensions specified in the table 1. Heat sink, TIM2, IHS, TIM1, die, epoxy-solder, substrate. The material properties of the components are specified in the table 2.

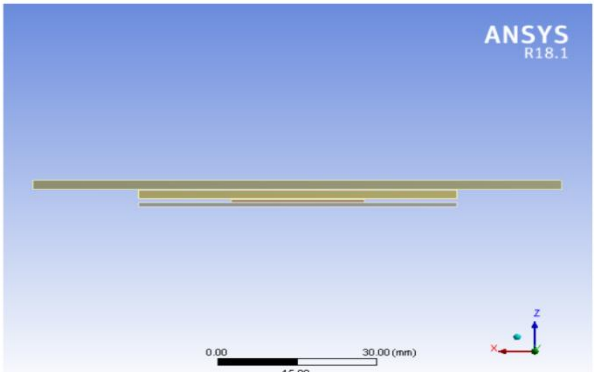


Fig. 3 3D model of the FCBGA

B. Mesh Generation

The model was then meshed. as shown in Figure 4. The model contains mapped Quadrilateral elements. As the thickness of the TIM layer is very less compared to the thickness of the IHS, Heat Sink and substrate, Sweep Method was used to have different element size in X, Y direction and Z-direction. Atleast 3 elements were considered in the least thickness components, so as to have an accurate convergence in the solution.

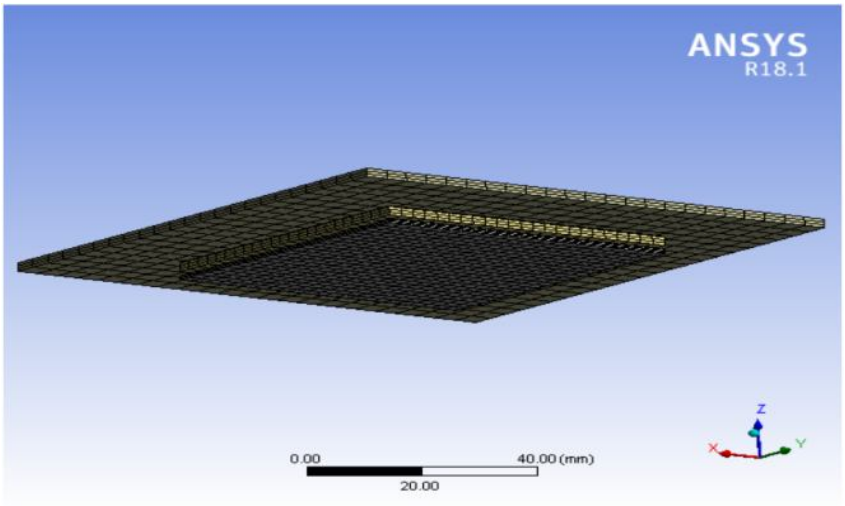


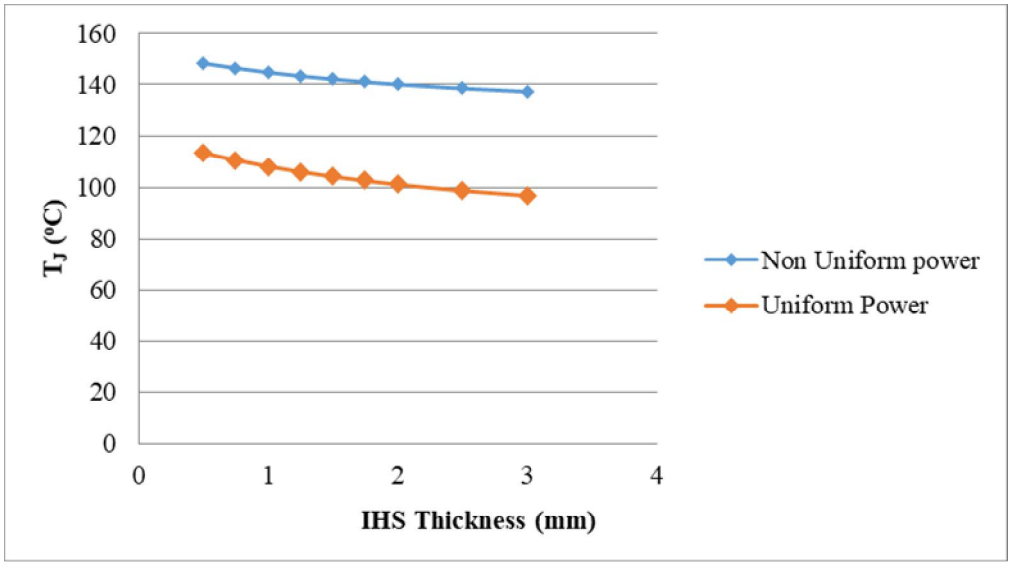
Fig. 4 Meshed Model of FCBGA Package

V. PARAMETRIC STUDY OF GEOMETRY AND MATERIAL PROPERTIES OF THE FLIP CHIP PACKAGE

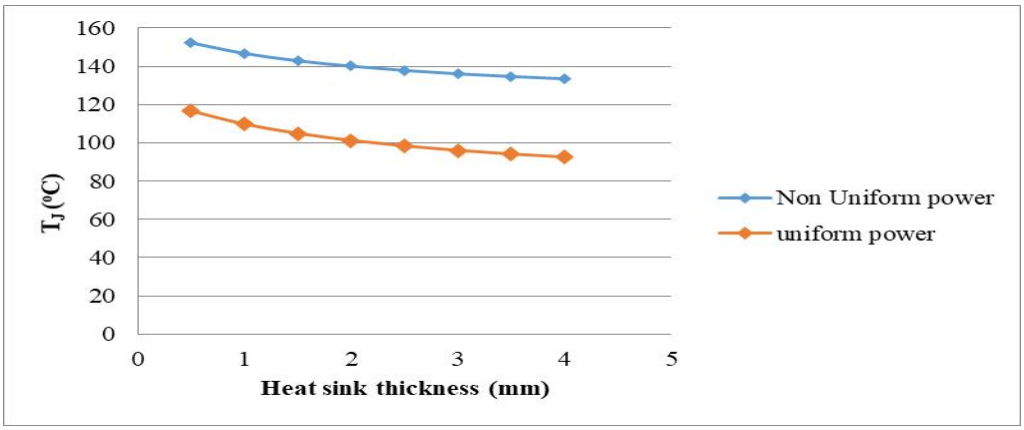
A parametric study is conducted to find the impact of geometrical and material properties of IHS, Heat sink, TIM, silicon in reducing Tj and temperature uniformity. First the effect of changing geometry of the components is analysed, then the impact of materials properties of IHS and TIM are evaluated.

A. Effect of Changing Geometry Of Components

In this paper, the change in Tj w.r.t variation in IHS, Heat sink and silicon thickness, keeping the thermal conductivity constant is observed. The Heat sink thickness is varied between 0.5 to 4 mm, IHS thickness is varied between 0.5 to 3 mm and silicon thickness is varied from 200 to 700 microns. For this study, conductivity of TIM is 3W/mK, IHS and Heat sink is 401W/mK. From the figure 5 it is evident that increase in IHS thickness from 0.5mm to 3mm has reduced max T_j from 148°C to 137°C and increase in Heat sink thickness from 0.5mm to 4mm has reduced Tj from 152°C to 134°C . Variation in silicon thickness does not have a significant impact on component temperature for the assumed power on the die.



(a)



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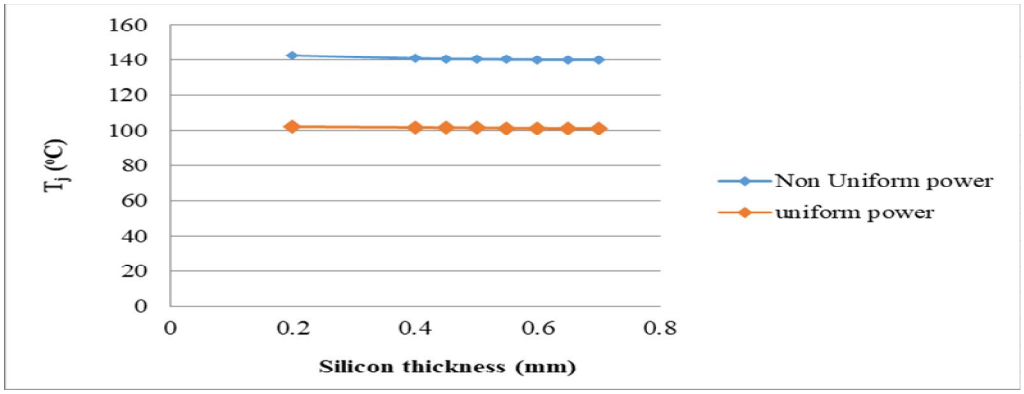

(c)

Fig. 5 (a). IHS thickness Vs T_j (b). heat sink thickness Vs T_j (c). Silicon thickness Vs T_j

B. Effect of Material Properties of IHS and TIM

In this paper, change in Tj w.r.t. the variation in thermal conductivity of IHS and TIM was analyzed. The conductivity of IHS was varied for different anisotropy factors i.e. the component temperatures were noted with different in-plane (kx,y) to out of plane (kz) thermal conductivity ratios of IHS.

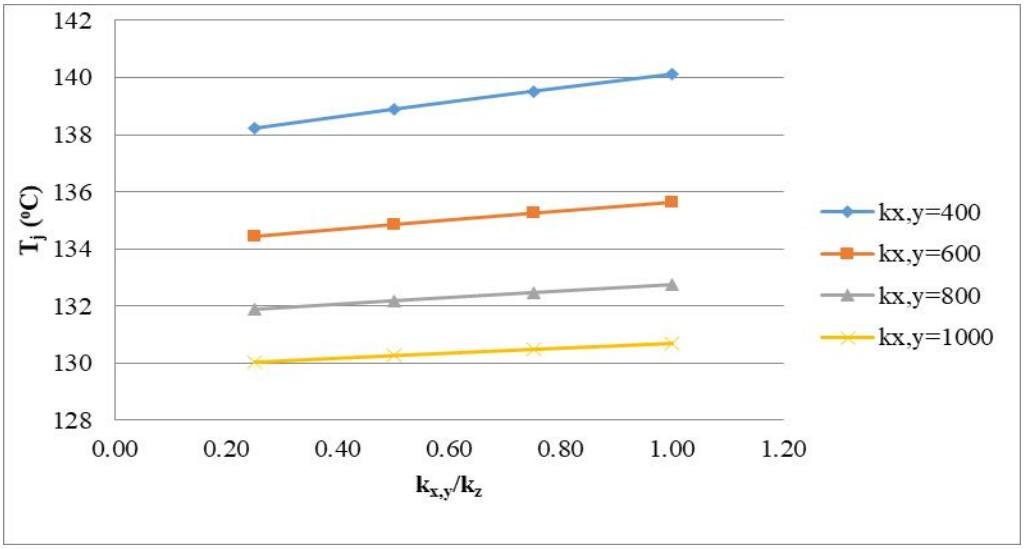

Fig.6 IHS conductivity Vs T_j

C. Effect of conductivity of TIM

From the Figure 6 it can be noted that as the in-plane conductivity of IHS(kx,y) increase, out of plane conductivity is less significant in dissipation of heat. We see that the slope of kx,y=1000 is lesser than the kx,y=400 for different anisotropy ratios. So materials with large anisotropy factors are highly preferable which will dissipate heat away from hotspots in the in-plane direction thus protecting the components underlying them from excessive heat. Adding reinceforments of large conductivity like graphene fibres can bring about temperature uniformity in the die.

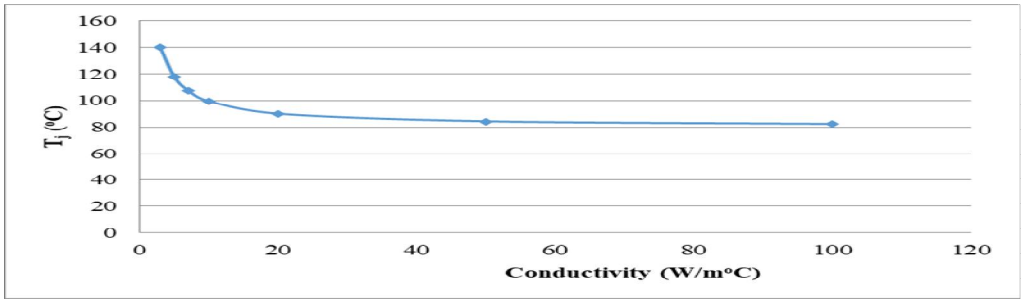

Fig. 7 Conductivity of TIM Vs T_j

Varying the thermal conductivity of TIM (k_{TIM}) from 3 W/mK to 50 W/m K has reduced T_j from 140.1°C to 84.4°C. This is well below the T_j of uniform power. From Figure 7 it is evident that T_j decreases exponentially when k_{TIM} is varied from 3 W/m K to 20 W/mK. Thus it can be inferred that k_{TIM} has a significant role in bringing down the temperature. T_j and Temperature uniformity for in-plane conductivity of IHS 1000 W/mK and K_{TIM} 10W/mK are 94.9°C and 28.6°C respectively.i.e. Tj has reduced by 45°c and 55% reduction in the temperature uniformity. The future work may be aimed at by using materials of high anisotropy factor as IHS material and enhancing conductivity of TIM by adding graphene fillers or flakes of varying volumetric fraction for better thermal performance of electronic packaging.

VI. RESULTS AND DISCUSSIONS

In this paper an attempt to find the significance of the different levels of packaging hierarchy in reducing the junction temperature Tj were analysed for a flip chip BGA. A parametric study was done to identify how different thermal performance characteristics of the constituent components affect Tj and Temperature uniformity of the die. Tj was evaluated by varying the geometry of the heat sink, IHS and silicon. Increasing the thickness of Heat sink and IHS has considerably reduced Tj. The impact of variation in silicon thickness was negligible. Tj was evaluated by parametrizing IHS with different anisotropy factors. When in-plane conductivity (kx,y) of IHS was at 1000 W/mK, the effect of conductivity across the plane(kz) was negligible. So reinforcing the traditionally used material, copper with highly conductive longitudinal fibers can substantially reduce Tj and temperature uniformity. By varying the k_{TIM} from 3 W/mK to 50 W/mK the Tj was well below that of uniform power map. From this it is evident that advanced TIM materials like solder TIMs, graphene fillers with conductivity more that 50 W/mK will help in better cooling of the device. Future work may be aimed at identifying potential composite materials for electronic applications. Future work may also include predicting the performance of thermal grease with addition of graphene particles or graphene flakes which have exceptionally high conductivity. Also studies aiming at the optimization of heat sink design for better heat dissipation may be taken up.

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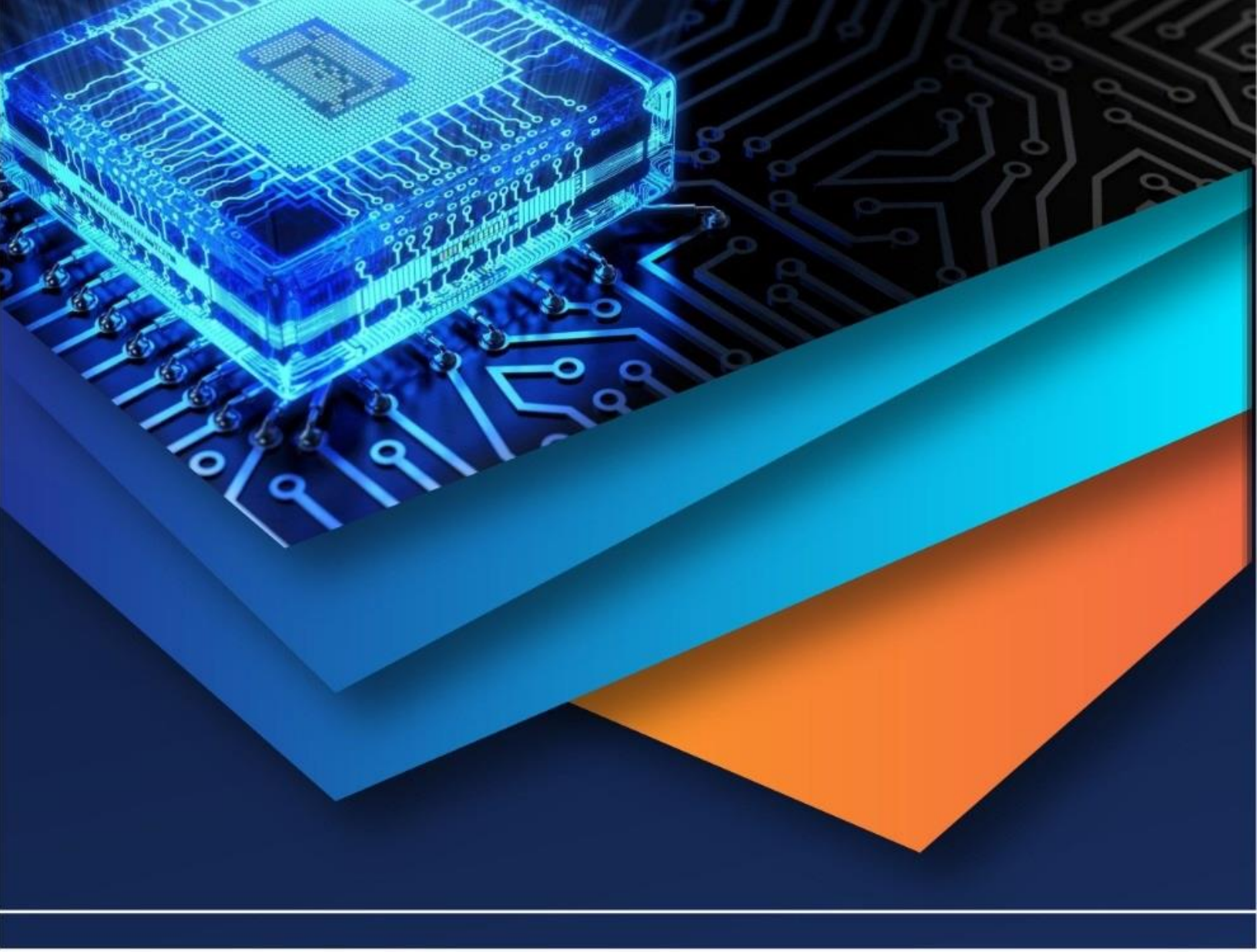

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