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A 129-level Asymmetrical Cascaded H-Bridge Multilevel Inverter with Reduced Switches and Low THD

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Abstract: ***The multilevel inverter is a power conversion device which is uses multiple dc sources to provide required alternating current level. It is can be used for medium to high power applications. This paper presents a 129 level asymmetrical cascaded H-bridge multilevel inverter with reduced switching components and higher THD. The proposed inverter uses multiple dc sources with voltage ratio 1:1:2:4:8:16:32. The proposed inverter uses voltage reference technique to control the switching components of the topology. The comparative analysis of 129 level ASCHBMLI and conventional inverter topologies have been presented. The main advantages of the proposed topology is lower switching components, lower losses, and lower THD without the need of filter. MATLAB/SIMULINK software is used to perform simulation and analyse the performance of the proposed topology.***
Keywords: Multilevel Inverter (MLI), Asymmetrical Cascaded H Bridge Multilevel Inverter (ASCHBMLI), Cascaded H Bridge (CHB), MATLAB, Total Harmonic Distortion (THD).

I. INTRODUCTION

The basic function of Inverters is to convert DC electricity to AC electricity, for uses in either stand-alone systems or to connect dc source to AC grid. The Multilevel inverters are power electronic method to generate multiple level AC voltages from multiple medium voltage, dc sources. The multilevel inverters were first invented in 1979, as a three level MLI. It gained popularity due its high-power capability and lower THD, lower electromagnetic interference. Due its vast applications, including FACTS drives, VAR control, HVDC, renewable systems etc., MLIs are popular. today more commercial products are based on MLIs. Thus, there is increased efforts in developing multilevel inverters by changing its topology to obtain superior performance, decreased switching losses, lower THD, lower components requirement etc. There are several topologies having distinctive features. Fig.1 shows different multilevel topologies.

The Multilevel inverters are classified into 3 basic types:

A. Diode clamped multilevel inverter
B. Flying capacitor multilevel inverter
C. Cascaded multilevel inverter

The diode-clamped multilevel inverter consists of clamping diode to generate multiple voltage levels through different phases to the capacitors which are connected in series. It requires (n-1) main dc link capacitors and (n-1)(n-2) diodes, where 'n' is number of levels required. Some of the advantages of Diode clamped multilevel inverter are that it has high efficiency for fundamental frequency, it can be used for high voltage back-to-back inter-connection or an adjustable speed drive. However, diode clamped MLI suffers from various limitations.
The maximum output voltage obtained is limited to one half of input DC voltage. The number of diodes required is quadratically equal to number of levels, thus it requires a large number of diodes to generate high number of levels, disturbed charge balance for more than three levels etc.
The Flying capacitor (FC) topology uses a large number of capacitors of equal value. The topology requires a total number of (n-1)(n-1)/2 capacitors per phase and (n-1) main bus capacitors. The main advantage of the Flying capacitor topology is that the phase redundancy is achievable for balancing voltage levels of capacitors.
The flying capacitor topology suffers from high switching losses, limited output voltage, requirement of large number of capacitors, complex start-up etc.

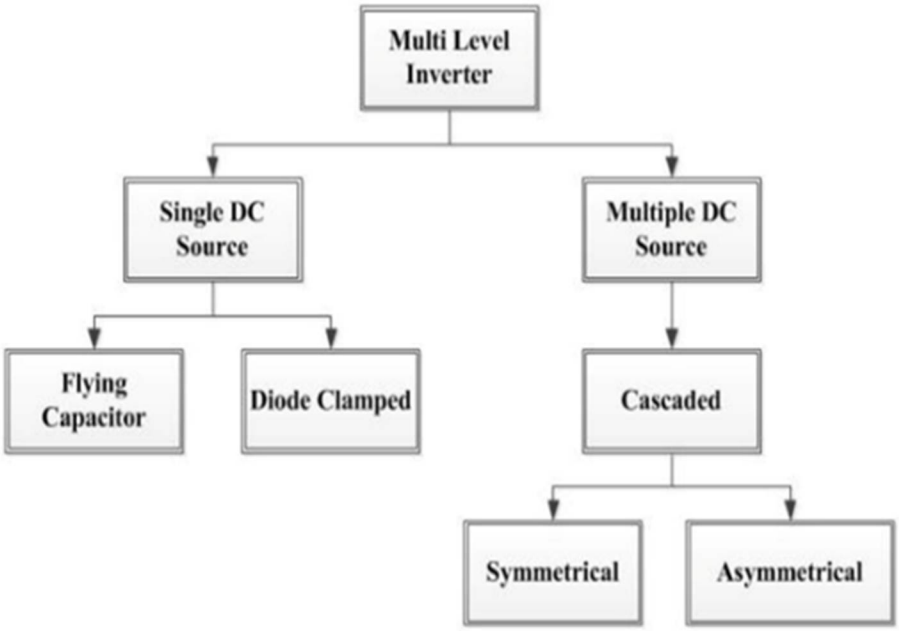


Fig.1 Basic Classification of Multilevel Inverter

The H-bridge topology derives its name from graphical representation of the circuit. A H-bridge consist of four active switches that can give positive, zero or negative polarity outputs to load depending on the switching conditions given to the switches. The cascaded H Bridge MLI consists of multiple DC sources and it is manipulated for various renewable energy sources like photovoltaic, fuel, biomass, etc. soft switching is employed to avoid bulky resistor-capacitor combinations. The advantages of this topology is modular design which makes the manufacturing of inverter, quicker and cheaper than other alternatives. The Cascaded H-Bridge inverters (CHB) are further classified into two categories. Symmetrical CHBMLI uses dc sources of equal magnitude (1:1:1:1:1:1:1). Hence it requires more dc sources to get higher levels. Asymmetrical CHBMLI uses dc sources of unequal magnitude in the order of (1:1:2:4:8:16:32). It allows synthesis of higher output voltage level with same number of sources as compared to symmetrical CHBs. The major advantage of ASCHBMLI is its ability to create higher voltage levels by using lesser number of DC sources.

The proposed topology uses 7 dc sources with dc source voltage ratio of 1:1:2:4:8:16:32 and uses voltage reference switching technique is used generate 129 level AC voltage. The design, simulation, and performance are analyzed and presented.

II. PROPOSED TOPOLOGY

A. Schematic Diagram of Proposed Topology

In conventional MLI topology, the number of levels depends on number of dc sources. In the proposed topology, high level voltage output can be obtained keeping number of dc sources required low. The schematic diagram of the proposed 129 level ASCHBMLI is shown in the Fig 1. The proposed topology consists of fourteen switches, five dc sources. The switches can be MOSFET or IGBT power semiconductor devices.

The proposed topology consists of two parts, a h bridge circuit and a level switching circuit. The H-bridge circuit functions as a polarity changing circuit. It changes polarity for every half cycle. In the Fig 1, the switches S7, S8, S9, S10 make up h-bridge circuit. To get positive polarity, S7, S9 are switched on together while S8, S10 are turned off. To get negative polarity, S7, S9 are switched off and S8, S10 are on. The switches, S1, S2, S3, S4, S5, S6 make up level generating circuit. This circuit generates multiple dc output voltage levels based on switching sequences. The switching sequence is generated by a switching control unit which uses voltage reference switching technique to generate switching pulses,

There are 129 different operating modes to generate 129 different output voltage levels for the proposed 129 level ASCHBMLI topology.

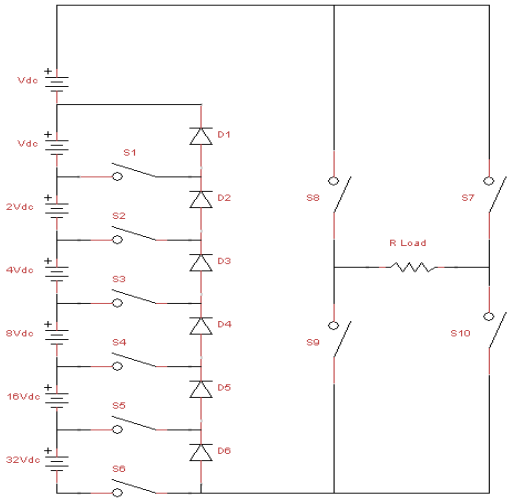


Fig 2. Proposed single phase 129 level ASCHBMLI topology

B. Comparative Analysis Of Proposed Inverter With Other Topologies

The comparative analysis of different topologies with the proposed topology is given in the table 1. The different parameters compared are number of switches, dc sources, capacitors, diodes. Where, n is the number of levels

TABLE 1: Comparison of different topologies.

Inverter Topologies	NPC	FC	CHB	Proposed Topology
Number of levels	n	n	n	n
Number of DC sources	1	1	(n-1)/2	$\log_2(n-1)$
Number of switches	2(n-1)	2(n-1)	2(n-1)	$\log_2(n-1)+3$
Number of Diodes	(n-2)(n-1)	-	-	$\log_2(n-1)$
Number of Capacitors	n-1	(n-2)(n-1)/2	-	-

From the table 1, it can be proved that proposed topology can generate 129 level output voltage with lesser number of DC sources, capacitors, power diode. The lesser number of components required reduces the switching losses of the system, reduces the system size, and makes the system cheaper.

C. Control Strategy

The switching sequence and the obtained voltage levels of the proposed topology is shown in the table 2 and table 3. The switches S1, S2, S3, S4, S5, S6 are controlled to supply different voltage levels and switching sequence for them is given in the table 2 and H-bridge switches S7, S8, S9, S10 are controlled to reverse polarity and its switching sequence is given in table 3. The switching sequence has 64 positive levels, 64 negative levels with only one '0' level in the output.

The switching control unit provides gate signals to the switches to control the switching states of the circuit. The control strategy is done by a voltage reference technique. In this technique, switching control unit will change the switching angles by comparing a reference signal, the switching pulses are generated by comparing absolute sine wave with multiple DC offset voltages. The comparator unit compares the absolute sine signal with DC offset values to generate binary values 0 or 1. The comparator outputs are 0, when reference signal is lesser than DC offset and 1, when reference signal is greater than DC offset. If the comparator outputs is 1 at that time, switching angle is achieved.

TABLE 2: Switching States for the proposed topology.

Switching States												
Output Voltages (Vo)	Conducting Switches						Conducting Diodes					
	S1	S2	S3	S4	S5	S6	D1	D2	D3	D4	D5	D6
+/- 64Vdc	1	1	1	1	1	1	0	0	0	0	0	0
+/- 63Vdc	0	1	1	1	1	1	1	0	0	0	0	0
+/- 62Vdc	1	0	1	1	1	1	0	1	0	0	0	0
+/- 61Vdc	0	0	1	1	1	1	1	1	0	0	0	0
+/- 60Vdc	1	1	0	1	1	1	0	0	1	0	0	0
+/- 59Vdc	0	1	0	1	1	1	1	0	1	0	0	0
+/- 58Vdc	1	0	0	1	1	1	0	1	1	0	0	0
+/- 57Vdc	0	0	0	1	1	1	1	1	1	0	0	0
+/- 56Vdc	1	1	1	0	1	1	0	0	0	1	0	0
+/- 55Vdc	0	1	1	0	1	1	1	0	0	1	0	0
+/- 54Vdc	1	0	1	0	1	1	0	1	0	1	0	0
+/- 53Vdc	0	0	1	0	1	1	1	1	0	1	0	0
+/- 52Vdc	1	1	0	0	1	1	0	0	1	1	0	0
+/- 51Vdc	0	1	0	0	1	1	1	0	1	1	0	0
+/- 50Vdc	1	0	0	0	1	1	0	1	1	1	0	0
+/- 49Vdc	0	0	0	0	1	1	1	1	1	1	0	0
+/- 48Vdc	1	1	1	1	0	1	0	0	0	0	1	0
+/- 47Vdc	0	1	1	1	0	1	1	0	0	0	1	0
+/- 46Vdc	1	0	1	1	0	1	0	1	0	0	1	0
+/- 45Vdc	0	0	1	1	0	1	1	1	0	0	1	0
+/- 44Vdc	1	1	0	1	0	1	0	0	1	0	1	0
+/- 43Vdc	0	1	0	1	0	1	1	0	1	0	1	0
+/- 42Vdc	1	0	0	1	0	1	0	1	1	0	1	0
+/- 41Vdc	0	0	0	1	0	1	1	1	1	0	1	0
+/- 40Vdc	1	1	1	0	0	1	0	0	0	1	1	0
+/- 39Vdc	0	1	1	0	0	1	1	0	0	1	1	0
+/- 38Vdc	1	0	1	0	0	1	0	1	0	1	1	0
+/- 37Vdc	0	0	1	0	0	1	1	1	0	1	1	0
+/- 36Vdc	1	1	0	0	0	1	0	0	1	1	1	0
+/- 35Vdc	0	1	0	0	0	1	1	0	1	1	1	0
+/- 34Vdc	1	0	0	0	0	1	0	1	1	1	1	0
+/- 33Vdc	0	0	0	0	0	1	1	1	1	1	1	0
+/- 32Vdc	1	1	1	1	1	0	0	0	0	0	0	1
+/- 31Vdc	0	1	1	1	1	0	1	0	0	0	0	1
+/- 30Vdc	1	0	1	1	1	0	0	1	0	0	0	1
+/- 29Vdc	0	0	1	1	1	0	1	1	0	0	0	1
+/- 28Vdc	1	1	0	1	1	0	0	0	1	0	0	1
+/- 27Vdc	0	1	0	1	1	0	1	0	1	0	0	1
+/- 26Vdc	1	0	0	1	1	0	0	1	1	0	0	1
+/- 25Vdc	0	0	0	1	1	0	1	1	1	0	0	1
+/- 24Vdc	1	1	1	0	1	0	0	0	0	1	0	1
+/- 23Vdc	0	1	1	0	1	0	1	0	0	1	0	1
+/- 22Vdc	1	0	1	0	1	0	0	1	0	1	0	1
+/- 21Vdc	0	0	1	0	1	0	1	1	0	1	0	1
+/- 20Vdc	1	1	0	0	1	0	0	0	1	1	0	1
+/- 19Vdc	0	1	0	0	1	0	1	0	1	1	0	1
+/- 18Vdc	1	0	0	0	1	0	0	1	1	1	0	1
+/- 17Vdc	0	0	0	0	1	0	1	1	1	1	0	1

+/- 16Vdc	1	1	1	1	0	0	0	0	0	0	1	1
+/- 15Vdc	0	1	1	1	0	0	1	0	0	0	1	1
+/- 14Vdc	1	0	1	1	0	0	0	1	0	0	1	1
+/- 13Vdc	0	0	1	1	0	0	1	1	0	0	1	1
+/- 12Vdc	1	1	0	1	0	0	0	0	1	0	1	1
+/- 11Vdc	0	1	0	1	0	0	1	0	1	0	1	1
+/- 10Vdc	1	0	0	1	0	0	0	1	1	0	1	1
+/- 9Vdc	0	0	0	1	0	0	1	1	1	0	1	1
+/- 8Vdc	1	1	1	0	0	0	0	0	0	1	1	1
+/- 7Vdc	0	1	1	0	0	0	1	0	0	1	1	1
+/- 6Vdc	1	0	1	0	0	0	0	1	0	1	1	1
+/- 5Vdc	0	0	1	0	0	0	1	1	0	1	1	1
+/- 4Vdc	1	1	0	0	0	0	0	0	1	1	1	1
+/- 3Vdc	0	1	0	0	0	0	1	0	1	1	1	1
+/- 2Vdc	1	0	0	0	0	0	0	1	1	1	1	1
+/- 1Vdc	0	0	0	0	0	0	1	1	1	1	1	1
0Vdc	0	0	0	0	0	0	0	0	0	0	0	0

TABLE 3: Switching States for polarity changing h-bridge inverter

Voltage Polarity	Conducting Switches			
	S7	S8	S9	S10
Positive	1	0	1	0
Negative	0	1	0	1

The switching pulses for the operation of proposed 129 level ASCHBMLI is given the Fig 3

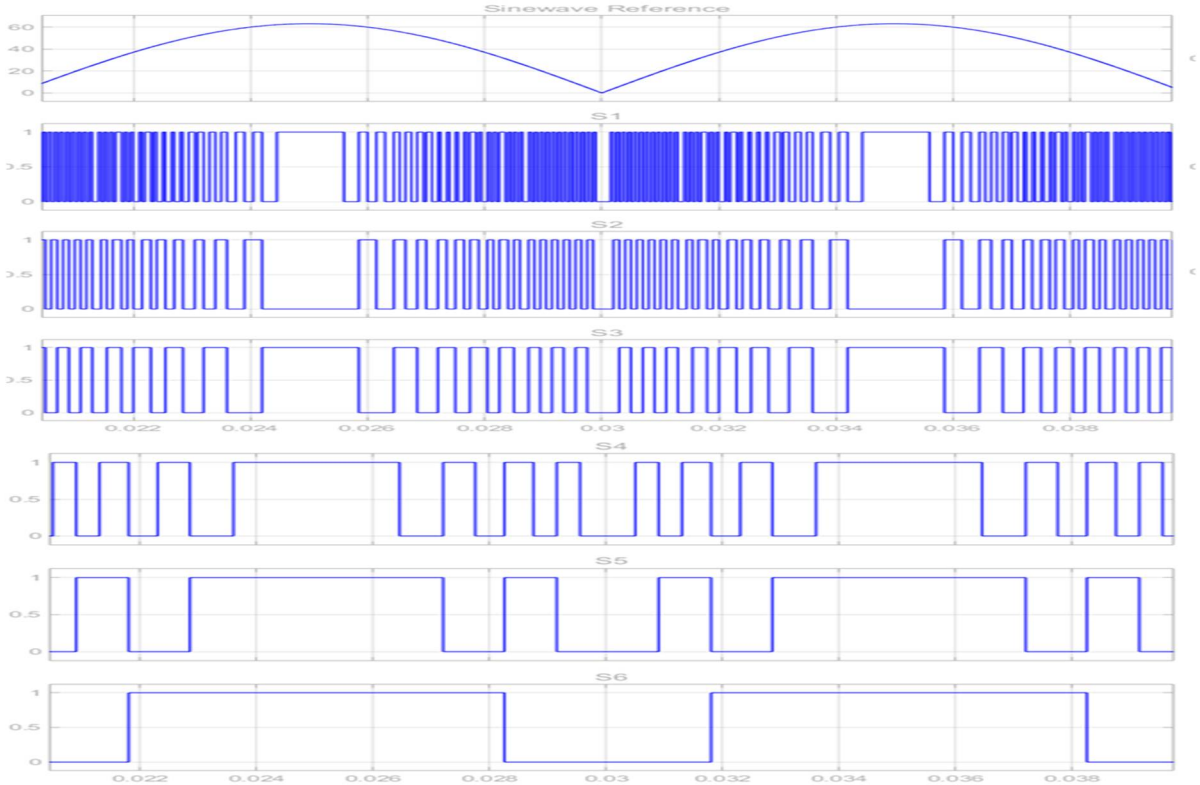
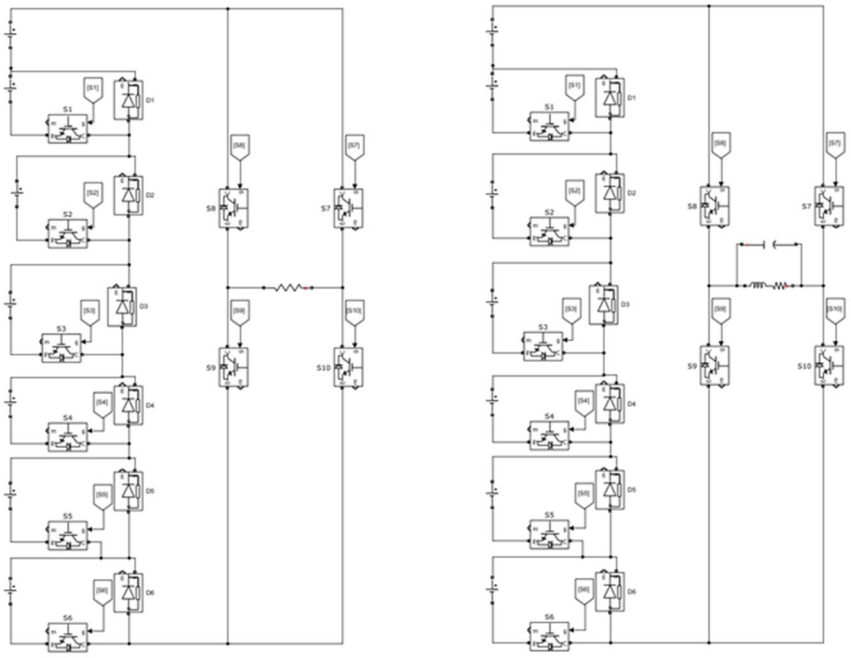


Fig 3. Switching pulse pattern for proposed inverter

III.SIMULATION AND RESULTS

The proposed topology is simulated in MATLAB/SIMULINK software, and performance of the topology in different loading conditions is studied in simulation of topology. Fig 4. shows Simulink model. The output voltage and current waveforms, value of THD and output power is measured. The value of different dc voltage sources are chosen in the ratio of 1:1:2:4:8:16:32 and the value of resistor during resistive load condition is 45Ω and during RL loads, the resistors and inductors are 45Ω and 10mH respectively.

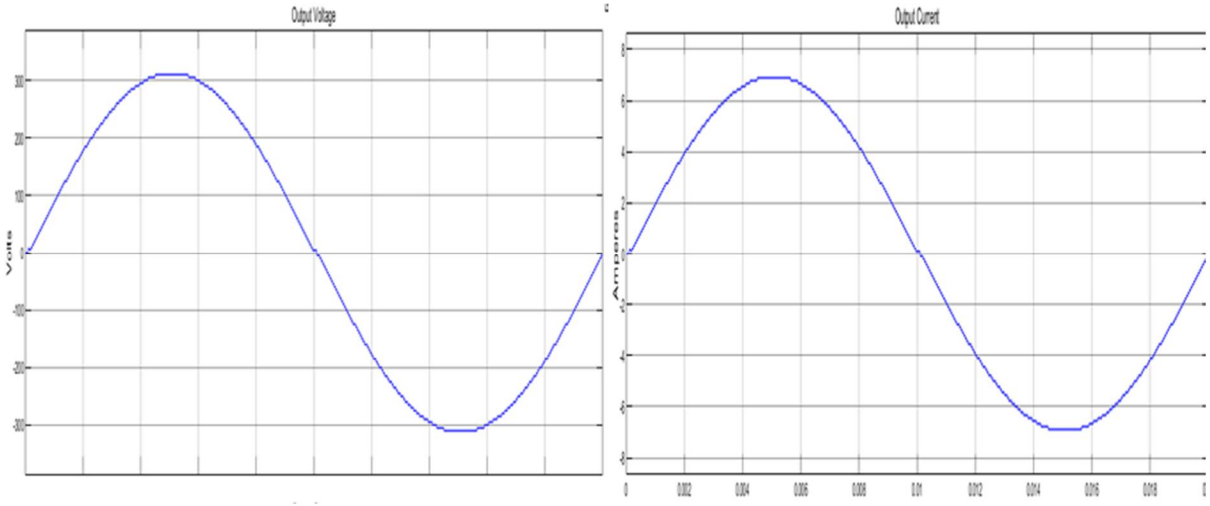


(a) (b)

Fig 4. Simulink model of the 129 level Multilevel inverter for (a) R Load (b) RL Load

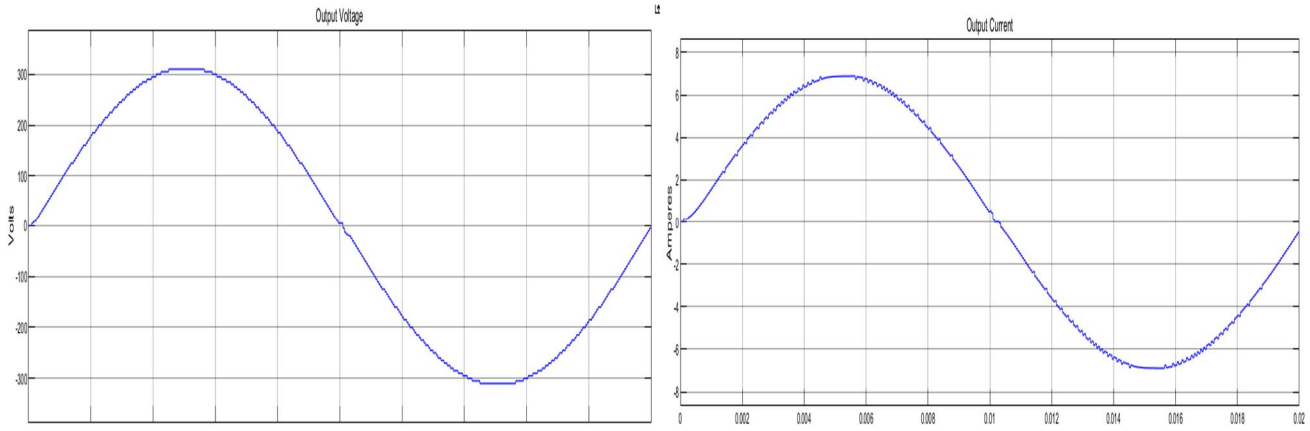
The DC sources in the simulation are of voltage magnitude 5Vdc, 10Vdc, 20Vdc, 40Vdc, 80Vdc, 160Vdc. The inverter generates output voltage of maximum voltage magnitude of 310V and minimum voltage magnitude of -310V. The switches used are IGBT which have fundamental operating switching frequency of 50 Hz. A capacitor of 1.2µF is connected in parallel to RL load to reduce the spikes.

The output waveform of 129 level inverter for R Load and R-L Load is given in the Fig 5 and Fig 6 respectively. The peak positive output current is found to be 6.88 A for R load and R-L load.



(a) (b)

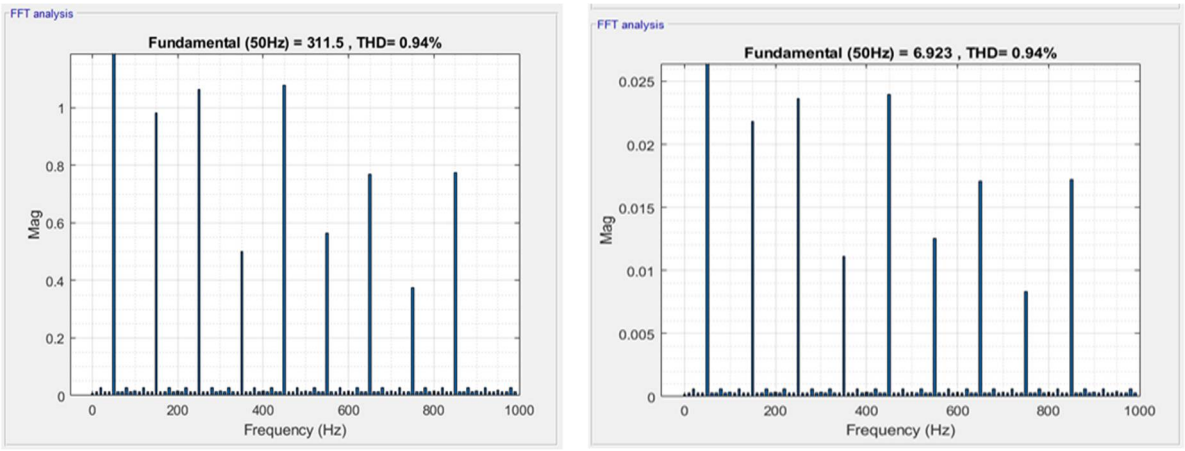
Fig 5. (a) Output voltage waveform (b) Output current waveform for R Load



(a) (b)

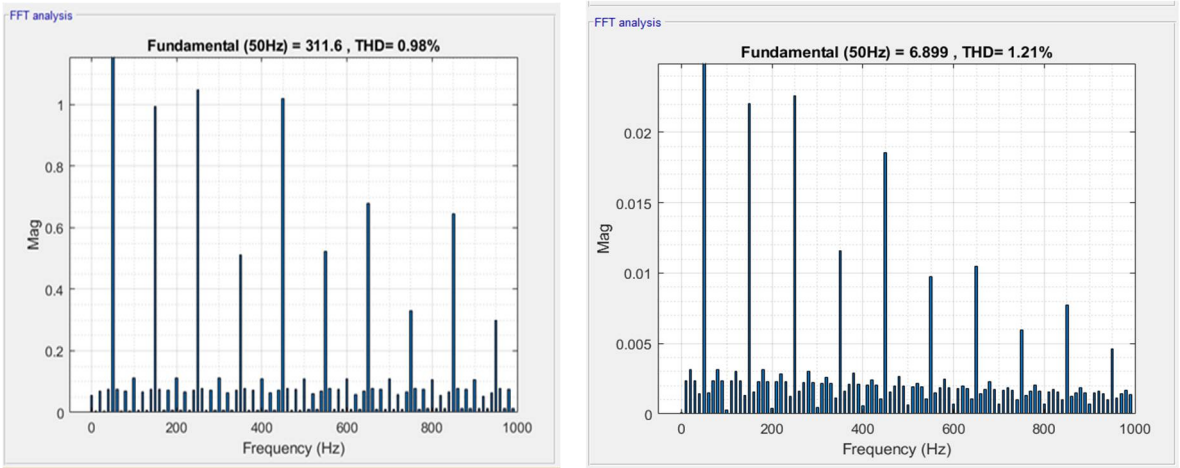
Fig 6. (a) Output voltage waveforms (b) Output current waveforms for R-L Load

The Fast Fourier Transfer Function (FFT) is used to calculate the Total Harmonic Distortion of the proposed converter for different loads. The FFT analysis is done for output voltage waveform and current waveform.



(a) (b)

Fig 7. (a) output voltage THD analysis for R Load (b) output current THD analysis for R Load



(a) (b)

Fig 8. (a) output voltage THD analysis for RL Load (b) output THD analysis for RL Load

IV. CONCLUSION

The simplified and reduced component cascaded H bridge inverter topology is proposed. The topology produces 129 level output voltage using less switches and lower THD value. The proposed topology has THD value of 0.94 % for voltage waveforms for R load and 0.98% for RL Load which is very less and within IEEE standards. For output currents, the FFT analysis gives THD values of 0.94 % and 1.21 % for R and RL loads respectively. The proposed inverter has output power measured to be 1072W. Due to low THD values and good power capacity, the proposed inverter is suitable for medium to high voltage applications.

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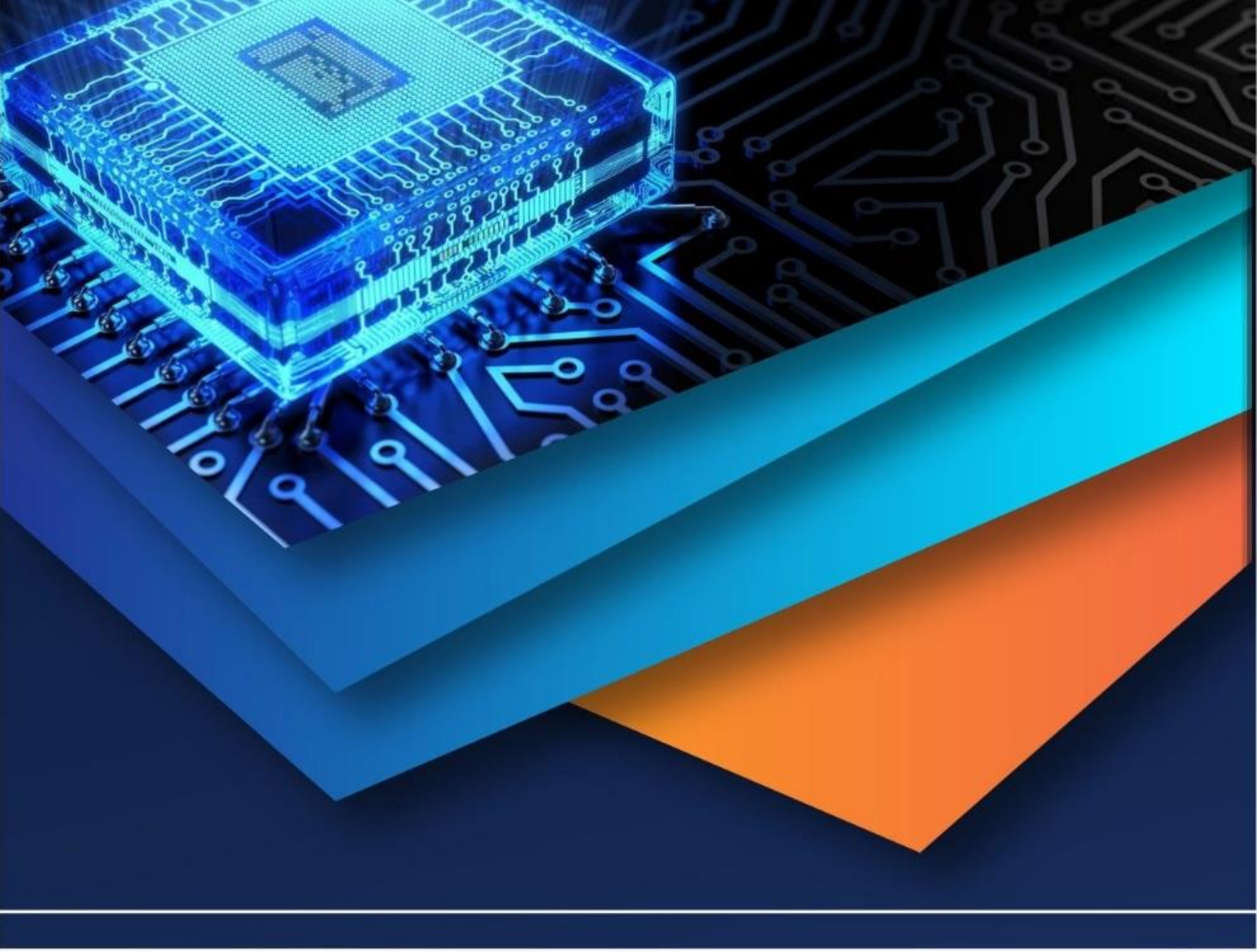

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