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Comparison between Cascaded Multilevel inverter and reduced switch multilevel inverter

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Abstract- This paper proposes a comparison between cascaded seven level inverter and nine level inverter using Phase opposition and disposition Pulse Width Modulation control scheme. The number of switches used in the cascaded seven and nine level inverter is identified and the Total Harmonic Distortion (THD) between them is compared. As the level gets increased the number of switches gets increased so the reduced switch topology is used with Pulse Width Modulation control scheme. The number of switches used in the reduced switch seven level and nine level inverter topology will be less when compared to the cascaded seven level and nine level inverter. The Total Harmonic Distortion (THD) between cascaded multilevel inverter and the reduced switch multilevel inverter is compared. The results are observed by MATLAB/SIMULINK software.

I. INTRODUCTION

There is a huge power requirement in industries and other areas. Multilevel inverter has become popular to fulfil power requirement due to advantage of high power quality waveforms, low electromagnetic compatibility [1]. Inverter is a device that converts electrical power from DC to AC form using electronic circuits. Generally simple inverter gives 2 or 3 level output voltage .Multilevel inverter gives 3 or more output voltage levels. It produces a stepped output voltage with reduced harmonic distortion when compared to a 2 level inverter. Multilevel inverters are basically 3 types [2]

A. Diode clamped inverter
B. Flying capacitor inverter
C. Cascaded inverter

The most commonly efficient inverter is cascaded multilevel inverter (CMLI). It provides higher output voltage and power levels. It is one of the methods used for drive application which meet the requirements such as high power rating with reduced THD and switching losses. The CMLI consists of number of levels as the levels gets increase the number of switches gets increase. In order to overcome this problem, we use the concept of “switch reduction”. In this work, the new topology called reduced switch diode bridge topology is used to reduce the switches and separate dc-source in CMLI. The MOSFETs used as semiconductor switches. MOSFETs are preferred in: High frequency applications (1MHZ), Wide line or load variations, Long duty cycles, and Low-voltage applications (500V). Mainly the MOSFET switches are selected because of its fast switching capability.

Here the bi-directional switch diode bring is used as the reduced switch topology. Bi-directional switch consists of three major categories namely common emitter type, common collector type and diode bridge. The diode bridge is the simplest technique comparing to other two methods. The diode bridge topology comprises a conventional H-bridge inverter, bidirectional switches, and also includes capacitor where the voltage gets divided. The modified H-bridge topology is significantly advantageous over other topologies, i.e., less power switch, power diodes, and less capacitor for inverters of the same number of levels [3]. The comparison between cascaded and reduced switch 9 level MLI and 7 level MLI were done and based on the results obtained the most effective MLI is adopted that gives the reduced THD output, less number of separate DC sources and also reducing the number of switches used as the levels gets increased.

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II. CASCADED SEVEN LEVEL INVERTER

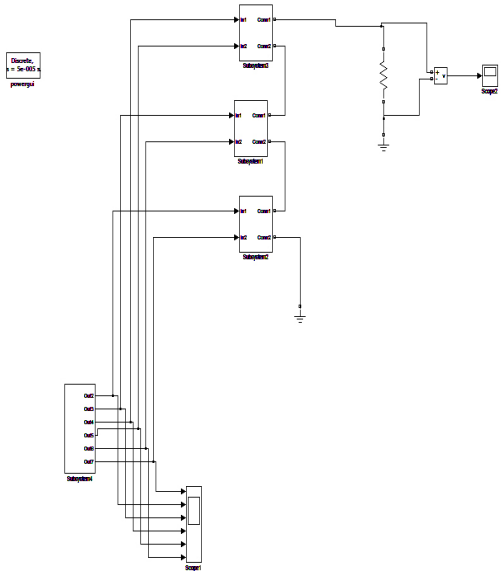

Fig.1. Simulation model of cascaded seven level inverter

The cascaded seven level inverter requires 2(m-1) switches where, m represents the number of levels. Thus for the nine level it is that 2(7-1) = 2*6 = 12 switches are used in the cascaded nine level inverter. The control technique for the CMLI used is the pulse width modulation with POD technique is used where the carrier signal above the zero axis all the carrier wave have same frequency, same amplitude and in phase each other. But the below the zero axis all the carrier wave have same frequency, same amplitude and in phase but all carrier wave have phase shifted 180 degree compare to the above zero axis carrier waveform. The PODPWM method has been given the better results among various methods. The first three subsystems consists of the full bridge circuit which uses MOSFET as the switching device.

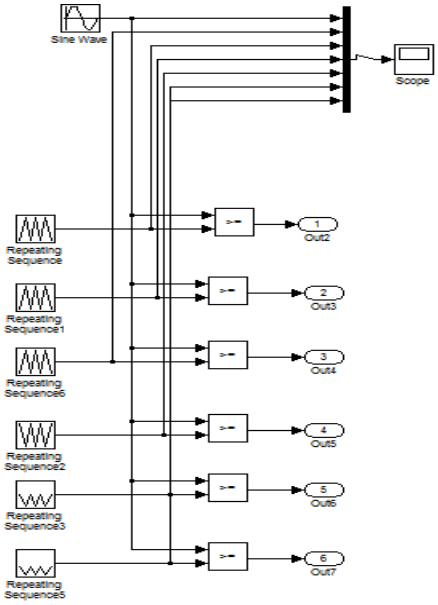

Fig.2. Simulation model of PODPWM technique

The Fig.2. Represents the PODPWM technique. The modulating signal is compared with the four carrier signal above zero axis and four carrier signals below zero axis that generates the gate pulses.

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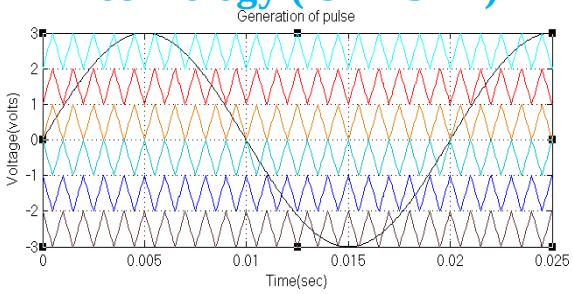

Fig.3. Generation of pulses by PODPWM technique

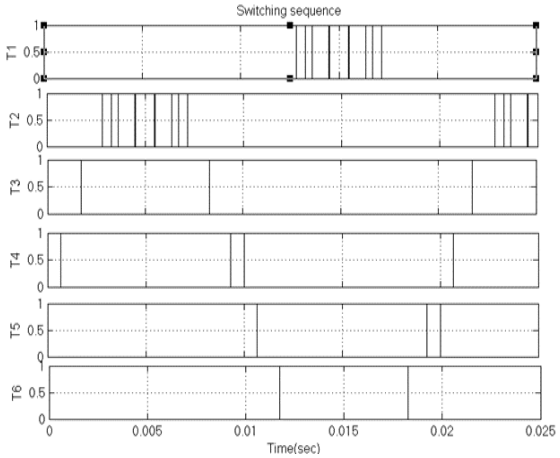

Fig.4. Switching pattern for cascaded seven level inverter

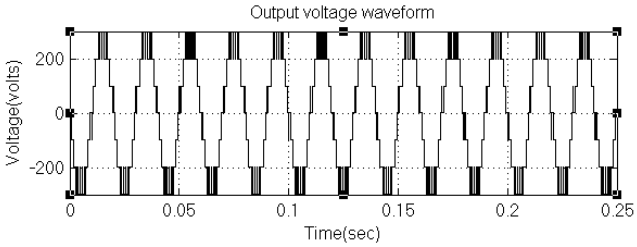

Fig.5. Output voltage of cascaded seven level inverter

The Fig.3.shows the generation of pulses by using the PODPWM technique and the Fig.4.represent the switching sequence of the cascaded seven level inverter. The Fig.5.shows the output voltage which has seven steps in the positive and the negative half cycle.

III. REDUCED SWITCH SEVEN LEVEL INVERTER

The multilevel inverters do have some disadvantages. One particular disadvantage is the greater number of power semiconductor switches needed and also it needs separate DC sources. There are many topologies to reduce the switches in the multilevel inverter. The bi-directional switch topology is used for the reduction of switches. There are three types of bi-directional switch topology such as common collector type, common emitter type and diode bridge topology. This project
uses diode-bridge topology for the reduction of switches, which consists of four diodes are arranged in the bridge topology in which switch is placed at the middle of the diode bridge.

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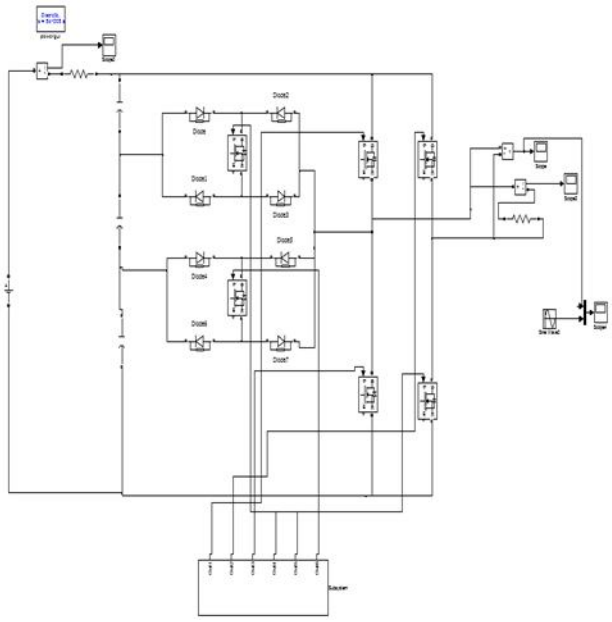

Fig.6. Simulation model of seven level inverter using reduced switch topology.

The Fig.6. represents the reduced switch diode bridge topology for seven level inverter where six switches are used for phase A instead of using 12 switches.

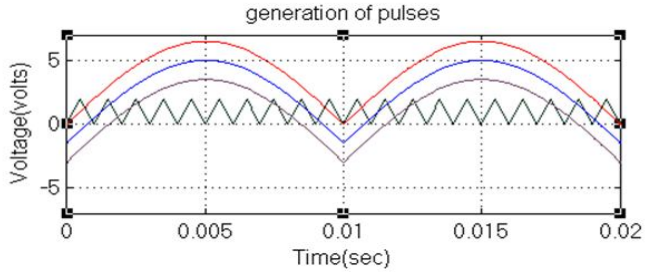

Fig.7. Single carrier sinusoidal pulse width modulation

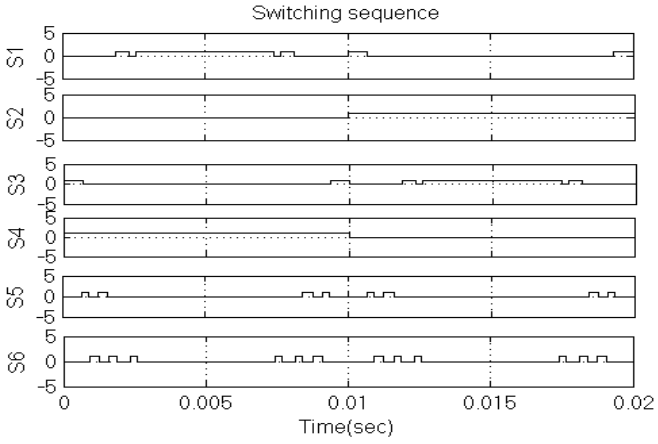

Fig.8. Switching sequence for seven level inverter.

There are three reference signal compared with one carrier signal to produce the pulse. Here ref1 interacts with carrier signal and produce the pulse1, ref2 interacts with the carrier and produces pulse2, ref3 interacts with the carrier and produces pulse3 and ref2 interacts with the carrier and produce the pulse4. The switch S2and S4 operates at the fundamental frequency. By comparing the pulse P1 and P3 that produces the pulse for the switch S1, switch S2 operates at fundamental frequency is triggered. The pulse1 and 3 is compared for next positive cycle to produce the pulse for switch S3, then S4 operates at fundamental frequency is triggered. The pulse for the switch S5 is produced by comparing the NOT gated pulse P1 and the pulse P2 both are AND gated and produces the

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pulse for the switch S5. The NOT gated pulse P3 and the pulse P4 is AND gated and produces the pulse for the switch S6. The number of switches require in the cascaded H bridge seven level inverter is 12 switches for each phase so totally 36 switches requires for three phase seven level inverter in cascaded form. But the reduced switch topology requires 6 switches per phase so totally 18 switches requires for three phase seven level inverter. Hence the component gets decreased in using the reduced switch topology.

TABLE I

Table.1. Switching table for reduced switch seven level inverter

Voltages	S1	S2	S3	S4	S5	S6
0V	0	1	0	1	0	0
+100V	0	0	0	1	0	1
+200V	0	0	0	1	1	0
+300V	1	0	0	1	0	0
0V	1	0	1	0	0	0
-100V	0	0	1	0	0	1
-200V	0	0	1	0	1	0
-300V	0	1	1	0	0	0

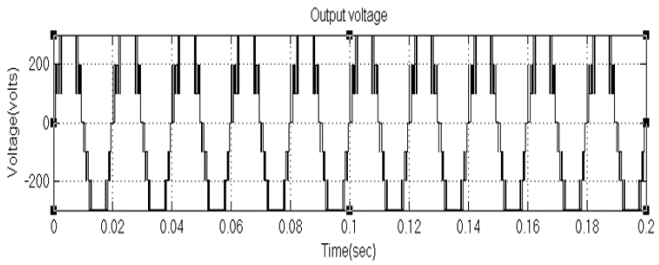

Fig.9. Output voltage waveform of reduced switch seven level inverter

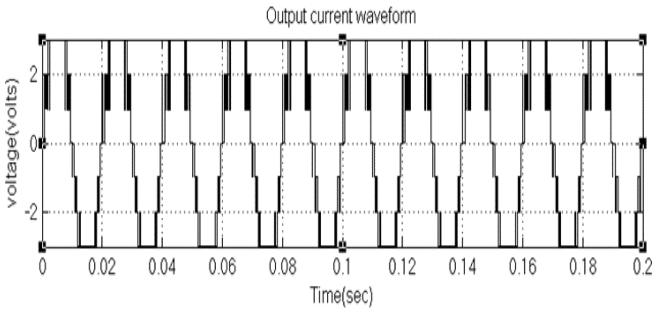

Fig.10. Output current waveform of reduced switch seven level inverter

The Fig.9. represents output voltage waveform and Fig.10. represents output current waveform of reduced switch seven level inverter.

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IV. CASCADED NINE LEVEL INVERTER

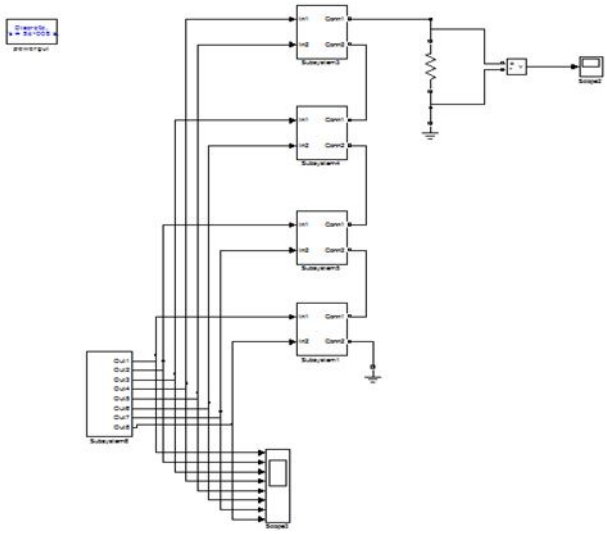

Fig.11. Simulation model of cascaded nine level inverter

The cascaded nine level inverter requires 2(m-1) switches where, m represents the number of levels. Thus for the nine level it is that 2(9-1) = 2*8 =16 switches are used in the cascaded nine level inverter. The control technique for the CMLI used is the pulse width modulation with POD technique is used where the carrier signal above the zero axis all the carrier wave have same frequency, same amplitude and in phase each other. But the below the zero axis all the carrier wave have same frequency, same amplitude and in phase but all carrier wave have phase shifted 180 degree compare to the above zero axis carrier waveform. The PODPWM method has been given the better results among various methods. Where the subsystem 1,5,4,3 consists of the full bridge circuit which uses the MOSFETs as the switches.

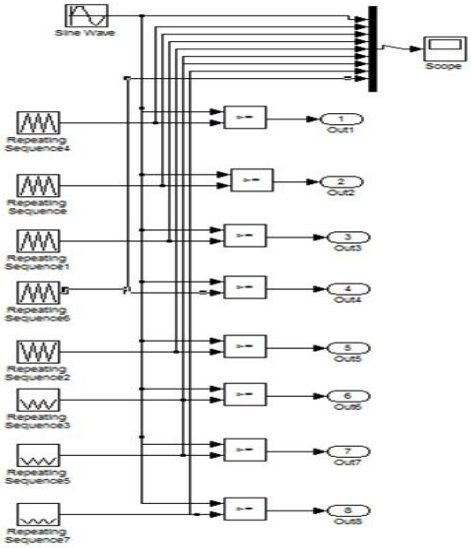

Fig.12. Simulation model of PODPWM technique

The Fig.12. represent the PODPWM technique. In which one reference signal is compared with the four carrier signal above zero axis and four carrier signals below zero axis that generates the gate pulses.

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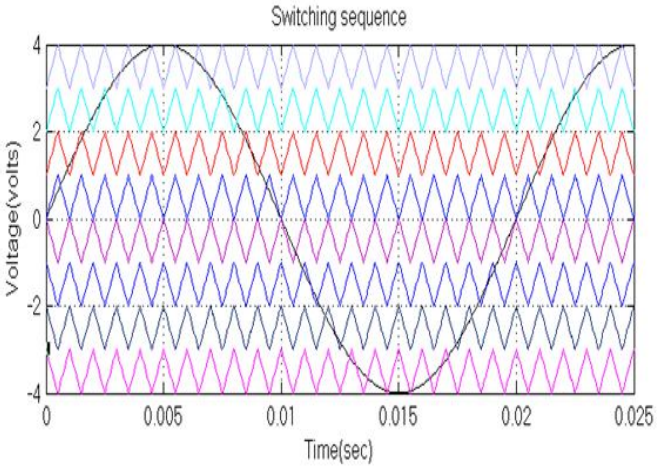

Fig.13. Generation of pulses by PODPWM technique

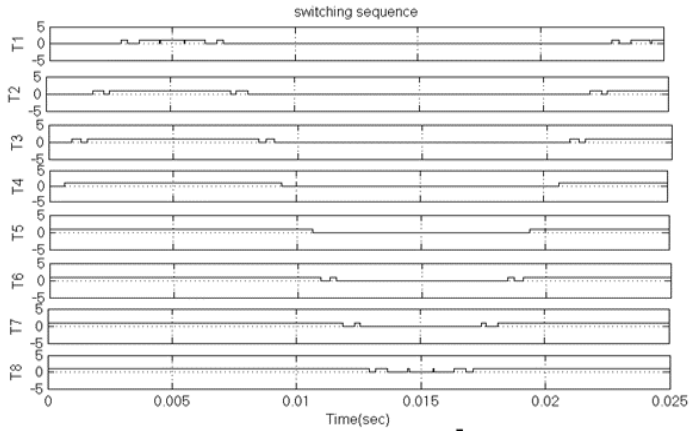

Fig.14. Switching pattern for cascaded nine level inverter

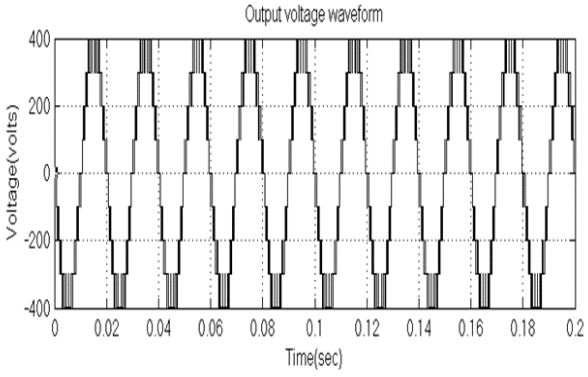

Fig.15. Output voltage of cascaded nine level inverter

The Fig.13.shows the generation of pulses by using the PODPWM technique and the Fig.14.represent the switching sequence of the cascaded nine level inverter. The Fig.15.shows the output voltage which have nine steps in the positive and the negative half cycle.

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V. REDUCED SWITCH NINE LEVEL INVERTER

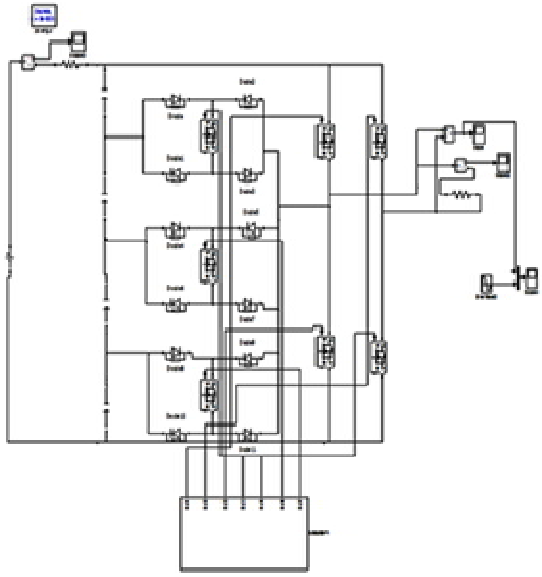

Fig.16. Simulation model of nine level inverter using reduced switch topology

The Fig.16. represents the reduced switch diode bridge topology for nine level inverter where seven switches are used for phase A instead of using 16 switches.

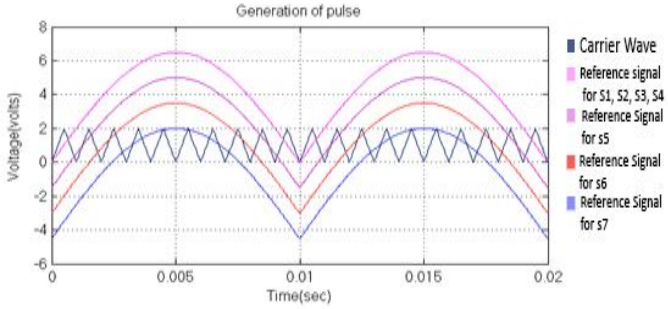

Fig.17. Single carrier sinusoidal pulse width modulation

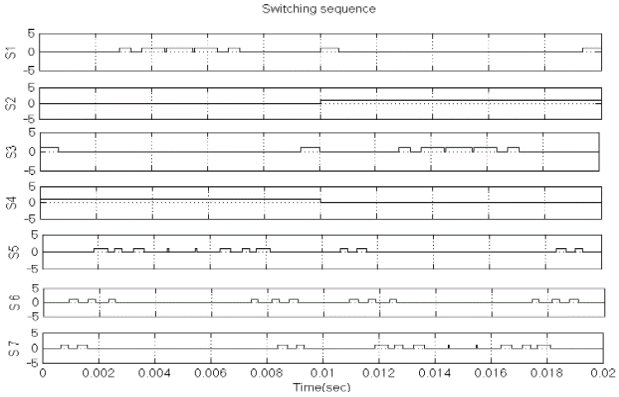

Fig.18. Switching sequence for nine level inverter.

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Voltages	S1	S2	S3	S4	S5	S6	S7
0V	0	0	1	1	0	0	0
V/4	0	0	0	1	0	0	1
2V/4	0	0	0	1	0	1	0
3V/4	0	0	0	1	1	0	0
4V/4	1	0	0	1	0	0	0
0V	1	1	0	0	0	0	0
-V/4	0	1	0	0	1	0	0
-2V/4	0	1	0	0	0	1	0
-3V/4	0	1	0	0	0	0	1
-4V/4	0	1	1	0	0	0	0

TABLE II

Table.2. Switching table for reduced switch nine level inverter

There are four reference signal compared with one carrier signal to produce the pulse. Here ref1 interacts with carrier signal and produce the pulse1, ref2 interacts with the carrier and produces pulse2, ref3 interacts with the carrier and produces pulse3, ref2 interacts with the carrier and produce the pulse4, and the ref4 interacts with carrier and produces pulse5. The switch S2and S4 operates at the fundamental frequency. By comparing the pulse1 and 3 produces the pulse to the switch S1, switch S2 operates at fundamental frequency is triggered. The pulse1 and 3 is compared for next positive cycle to produce the pulse for switch S3, then S4 operates at fundamental frequency is triggered. The product of pulse 3 and NOT gated pulse5 is compared with the product of pulse4 and NOT gated pulse1 to produce the pulse for the switch S5 and S7 and the switch S6 is triggered by comparing the pulse2 and NOT gated pulse3. The number of switches require in the cascaded H bridge nine level inverter is 16 switches for each phase so totally 48 switches requires for three phase nine level inverter in cascaded form. But the reduced switch topology requires 7 switches per phase so totally 21 switches and three separate dc sources are required for the three phase nine level inverter using reduced switch topology. Hence the components gets decreased in using the reduced switch topology.

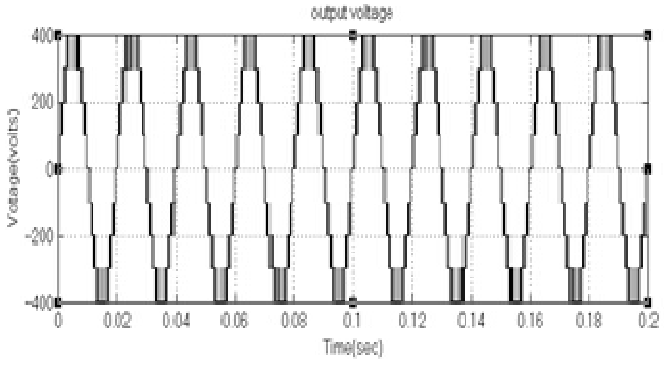


Fig.19. Output voltage waveform of reduced switch nine level inverter

The Fig.19. represents the output voltage waveform of reduced switch nine level inverter, where it uses the less number of switches and separate DC sources when compared to the cascaded nine level inverter.

TABLE III

Table.3. Comparison between Cascaded Multilevel inverter and reduced switch multilevel inverter

S.NO.	CASCADED SEVEN LEVEL INVERTER TOPOLOGY	REDUCED SWITCH SEVEN LEVEL INVERTER TOPOLOGY	CASCADED NINE LEVEL INVERTER TOPOLOGY	REDUCED SWITCH NINE LEVEL INVERTER TOPOLOGY
No. of switches used per phase	12 switches are used per phase	6 switches are used per phase	16 switches are used per phase	7 switches are used per phase
THD	19.70%	16.46%	13.79%	11.12%

From the above comaparison table we can easily identify that the reduced switch nine level inverter uses less number of switches compared to other multilevel inverter and also produces lowest THD in the output voltage. Thus the reduced switch nine level inverter is more efficient to uses in many applications.

VI. CONCULSION

In this work the cascaded seven and nine level inverter configuration are simulated using SIMULINK. The number of switches, separate DC sources and the THD in both the cascaded seven level and nine level inverter is compared. As the levels get increased the switches and the separate DC sources also increases. In order to reduce the number of switches, DC sources and the THD the reduced switch topology is used. The reduced switch seven level and nine level inverter configuration was implemented using SIMULINK. By comparing the cascaded seven level and the nine level with the reduced switch seven level and the nine level inverter, the reduced switch topology using multilevel inverter requires less number of switches and the separate DC sources and the THD value gets reduced as the levels gets increased. From the results the reduced switch nine level inverter is more efficient when comparing with the other such that it requires seven switches, one separate DC source and the THD is 11.12% which is less when compared with other configuration using multilevel inverter.

REFERENCES

[1] V. Chandana, S. Suriya (Department of Electrical and Electronics, M.tech (P.E), JNTU University, Dept of EEE Assistant professor, SMEC), “A Comparison of Symmetrical and Asymmetrical Three-Phase Cascaded Multilevel Inverter Using Flexible Control Technique for DTC Induction Motor Drives” , ISSN : 2248-9622, Vol. 3, Issue 5, Sep-Oct 2013, pp.1800-1806.

[2] Nayna Bhargava, Sanjeev Gupta, S. P. Phulambrikar, “Analysis of Asymmetrical Cascaded 7 Level and 9 Level Multilevel Inverter Design for Asynchronous Motor”, International Journal of Engineering Research & Technology (IJERT) Vol. 3 Issue 8, August – 2014 ISSN: 2278-018.

[3] K.L.Dheeraj, M.Diwakar, M.DurgaRaj, M.Eswar, K.Naga Venkatesh Dept. of EEE, KLUniversity, Vaddeswaram, Guntur, A.P. India, “THD Analysis of Cascaded Mli for Various PWM Techniques”, International Journal of Engineering Trends and Technology (IJETT) – Volume 11 Number 3 - May 2014.

[4] J. Rodriguez, Departament de Electronica, Univ. Tecnica Federico Santa Maria, Valparaiso, Chile Jih-Sheng Lai ; Fang Zheng Peng, “Multilevel inverters: a survey of topologies, controls, and applications”, Industrial Electronics, IEEE Transactions on Volume:49 , Issue: 4.

[5] Pontt, J.; Rodriguez, J.; Huerta, R. "Digital signal processing course innovations for power electronics practice", Frontiers in Education, 2003. FIE 2003 33rd Annual, On page(s): F1B - 6-11 Vol.2 Volume: 2, 5-8 Nov. 2003.

[6] Boroyevich, D.; Burgos, R.P. "PEBB-oriented generalized representation of switching power converters", Power Engineering Society General Meeting, 2003, IEEE, On page(s): 1344 - 1349 Vol. 3 Volume: 3, 13-17 July 2003.

[7] Sirisukprasert, S.; Huang, A.Q.; Lai, J.-S. "Modeling, analysis and control of cascaded-multilevel converter-based STATCOM", Power Engineering Society General Meeting, 2003, IEEE, Volume: 4, 13-17 July 2003.

[8] Vassallo, J.; Clare, J.C.; Wheeler, P.W. "A power-equalized harmonic-elimination scheme for utility-connected cascaded H-bridge multilevel converters", Industrial Electronics Society, 2003. IECON '03. The 29th Annual Conference of the IEEE, On page(s): 1185 - 1190 Vol.2 Volume: 2, 2-6 Nov. 2003.

[9] Kempski, A.; Smolenski, R.; Kot, E.; Fedyczak, Z. "Active and passive series compensation of common mode voltage in adjustable speed drive system", Industry Applications Conference, 2004. 39th IAS Annual Meeting. Conference Record of the 2004 IEEE, On page(s): 2665 - 2671 vol.4 Volume: 4, 3-7 Oct.

2004.

[10] B.P.Mcgrath and D.G Holmes "Multi carrier PWM strategies for multilevel inverter" IEEE Transaction on Industrial Electronics, Volume 49, Issue 4, Aug 2002, pp 858-867.

[11] Agilities and M. Calais, "Application Specific Harmonic Performance Evaluation of Multicarrier PWM Techniques", in Conf. Rec. 1998 IEEE Power Electronics Specialists Conference, pp. 172-178.

[12] Rashid, M.H, 2004. "Power Electronics: Circuits, devices and application", Third Edition, Prentice Hall

[13] D.Mohan and Sreejith B.Kurub "Performance Analysis of Multi Level Shunt Active Filter based on SDM" in CiiT International Journal of Digital Signal Processing pp 42 –46.

[14] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari and G. Sciutto, "A New Multilevel PWM Method: A Theoretical Analysis",IEEE Transactions on Power Electronics, Vol. 7, NO. 3, July 1992, pp.497-505.

[15] J.Rodríguez, J.S.Lai, and F. Z.Peng,"Multilevel Inverters: A SurveyofTopologies,Controls,and Applications",IEEETransactions on Industrial Electronics, Vol. 49,No. 4, August 2002,pp.724-739.

[16] C. Govindaraju1 and K.Baskaran, "Performance Improvement of Multiphase Multilevel Inverter Using Hybrid Carrier Based Space Vector Modulation", International Journal on Electrical Engineering and Informatics - Volume 2, Number 2, 2010,pp 137-149.

[17] M. N. A. Kadir S. Mekhilef, and H. W. Ping "Voltage vector control of a hybrid three-stage eighteen-level inverter by vectordecomposition" IET Trans. Power Electron.,vol.3,no. 4, pp.601- 611, 2010.

[18] Kang, D. W., Lee, Y. H., Suh, B. S., Choi, C. H., and Hyun, D. S. "An improved carrierwave-based SVPWM method using phase voltage redundancies for generalized cascaded multilevel inverter topology,". In Proc. IEEE APEC, 2000, pp. 542–5 4.

[19] E. Babaei, S. H. Hosseini, G. B. Gharehpetian, M. T. Haque, and M. Sabahi, "Reduction of dc voltage sources and switches in asymmetrical multilevel converters using a novel topology," Elsevier J. Electr. Power Syst. Res., vol. 77, no. 8, pp. 1073–1085, Jun. 2007.

[20] Zhong Du; Tolbert, L.M.; Chiasson, J.N.; Ozpineci, B.;, "A cascade multilevel inverter using a single DC source," ," in Proc. IEEE APEC'06, 2006, pp. 426 – 430.

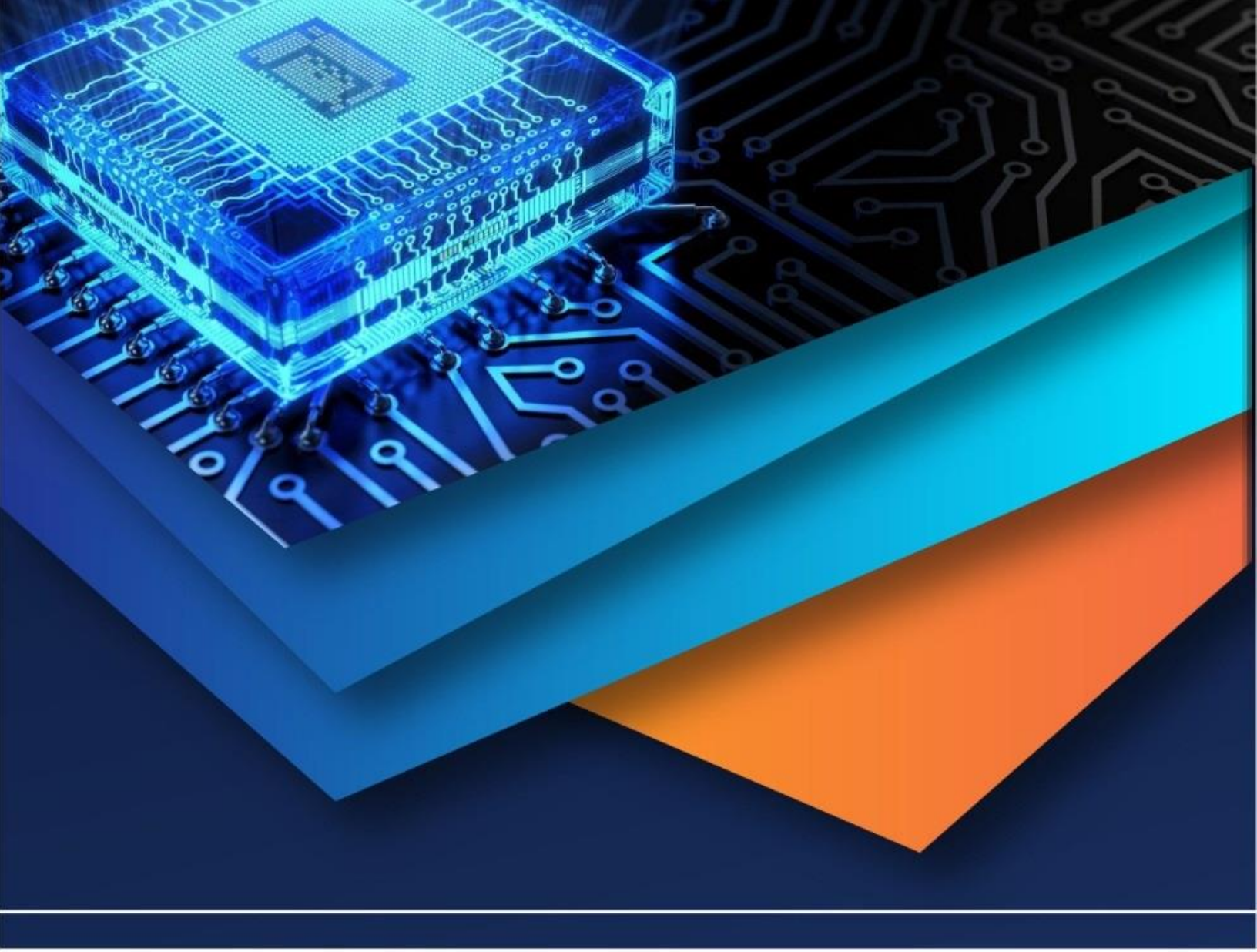
[21] S. J. Park, F. S. Kang, M. H. Lee, C. U. Kim, "A new single-phase fivelevel PWM inverter employing a deadbeat control scheme," IEEE Trans.Power Electron.,vol. 18, no. 18, pp. 831-843, May. 2003.

[22] L. M. Tolbert, F. Z. Peng, "Multilevel converters as a utility interfacefor renewable energy systems," in Proc. IEEE Power Eng. Soc. Summer Meeting 2000 ,vol. 2 , pp. 1271-1274.

[23] A.Nabae, I. Takahashi, and H. Akagi, "A new neutral-point clamped PWM inverter," IEEE Trans. Ind. Applicat., vol. IA-17, no. 5, pp. 518–523, Sep./Oct 1981 .

[24] Kang, D. W., Lee, Y. H., Suh, B. S., Choi, C. H., and Hyun, D. S. "An improved carrierwave-based SVPWM method using phase voltage redundancies for generalized cascaded multilevel inverter topology,". In Proc. IEEE APEC, 2000, pp. 542–5 48.

[25] Rokan Ali Ahmed, S. Mekhilef, Hew Wooi Ping Department of Electrical, "New multilevel inverter topology with reduced number of switches", Proceedings of the 14th International Middle East Power Systems Conference (MEPCON'10), Cairo University, Egypt, December 19-21, 2010, Paper ID 236.



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IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

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