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Development of Programmable Test Pattern Generator for VLSI Testing

Neha Sharma[1], Dr. Vishal Ramola[2]
Faculty of Technology Uttarakhand Technical University Dehradun-248007, INDIA

Abstract—This paper depicts a low-control (LP) programmable generator equipped for creating pseudorandom test designs with fancied toggling levels and improved fault coverage slope contrasted with the best-to built in self test (BIST)- based pseudorandom test design generators. It is involved a direct limited state machine (A linear feedback shift register or a ring generator) driving a phase shifter, and it accompanies various components permitting this device to deliver binary sequences with preselected toggling (PRESTO) action. We acquaint a strategy with naturally select a few controls of the generator offering simple and exact tuning. The same method is in this way utilized to deterministically direct the generator toward test groupings with enhanced fault coverage . Besides, this paper proposes a LP test pressure strategy that permits modeling the test power envelope in a completely unsurprising, precise, and adaptable style by adjusting the PRESTO-based logic BIST (LBIST) foundation. The proposed half and half plan productively consolidates test pressure with LBIST, where both methods can work synergistically to convey amazing tests.

Keywords— BIST (Built In Self Test), LFSR (Linear Feedback Shift Register), PRPG (Pseudo Random Pattern Generator), PRESTO (Preselected Toggling)Generator.

I. INTRODUCTION

Although over the next years, the primary objective of manufacturing test will remain essentially the same to ensure authentic and very high quality semiconductor products conditions and consequently also check solutions may undergo a significant evolution. The semiconductor technology, and its design characteristics, and the design process are one of the key factors that will affect this evolution. With new types of deficiencies that one will have to consider to provide the required test quality for the next technology nodes such as 3-D, it is appropriate to pose the question of what matching design-for- test (DFT) methods will need to be deployed. Test compression, introduced a decade ago, has quickly become the main stream DFT methodology. However, it is unclear whether test compression will be capable of coping with the rapid rate of technological changes over the next decade. Interestingly, logic built-in self-test (LBIST), originally developed for board, system, and in-
field test, is now gaining acceptance for production check as it provides terribly sturdy DFT and is employed progressively usually with check compression. This hybrid approach seems to be the next logical biological process step in DFT. It has potential for improved test quality; it ought to augment the abilities to run at-speed power aware tests, and it can scale back the worth of manufacturing check whereas protective all LBIST and scan compression advantages.

This project describes that a low-power (LP) programmable generator is enough capable for producing pseudorandom check patterns with desired toggling levels and increased fault
coverage gradient compared with the best-to- date integral self-test (BIST)- based mostly pseudorandom check pattern generators. It is contained a direct limited state machine (a straight feedback shift register or a ring generator) driving a suitable stage shifter, and it accompanies various elements permitting this gadget to deliver binary groupings with preselected flipping (PRESTO) action. We introduce a method to automatically select several controls of the generator offering easy and precise tuning. The same technique is subsequently employed to deterministically guide the generator toward test sequences with improved fault-coverage- to pattern-count ratios. The test design generator produces test vectors that are connected to the tried circuit amid pseudo-random testing of combinational circuits. The way of the generator subsequently straightforwardly impacts the shortcoming scope accomplished. Straight criticism shift registers (LFSRs) are for the most part utilized as test example generators, and the creating polynomial is primitive to guarantee the greatest period. We have demonstrated that it is not imperative to use primitive polynomials, and also that their utilizing is even undesirable as a part of generally cases. This is archived by measurable charts. The need of the correct
decision of a producing polynomial and a LFSR seed is appeared here, by planning a blended mode BIST for the ISCAS benchmarks As the many-sided quality of VLSI circuits always increments, there is a need of an implicit individual test (BIST) to be utilized. Worked in individual test empowers the chip to test itself and to assess the circuit reaction. Along these lines, the extremely perplexing and costly outer ATE (Automatic Test Equipment) might be totally overlooked, or its many-sided quality

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essentially lessened. Besides, BIST empowers a simple access to inner structures of the tried circuit, which are amazingly difficult to reach from outside. There have been proposed numerous BIST hardware plan techniques. In the majority of the best in class strategies some sort of a pseudorandom design generator (PRPG) is utilized to create vectors to test the circuit. As the complexity of VLSI circuits perpetually will increase, there is a requirement of a built-in self-test (BIST) to be used. Built-in self-test enables the chip to take a look at itself and to judge the circuit response. There have been proposed several BIST instrumentality style ways. In most of the state-of- the-art ways some kind of a pseudorandom pattern generator (PRPG) is employed o supply vectors to check the circuit. These vectors are applied to the circuit either as they are, or the vectors are changed by some further electronic equipment in order to get higher useful coverage.

II. BIST ARCHITECTURE

The most effective way to ensure the correctness of functionality of a certain device is to test it. For Application Specific Integrated Circuits (ASICs), testing becomes a significant topic itself. Modern ASIC manufacture technology allows integration of billions of gates into a single chip, and requires an efficient, automated way to test it. Testing is also becoming a key cost factor in ASIC production. It is reported that testing cost can be over one third of the product cost [13].

The typical way to test a digital circuit is to apply certain stimuli (called test vectors or test patterns) to the input of the circuit, and analyse the responses extracted from the output of the circuit. Keeping in mind the end goal to peruse and compose the interior condition of the circuit, the memory components in the circuit are arranged into sweep chains so their substance can be gotten to. It is a generally received technique today to apply test vectors created via Automatic Test Pattern Generation (ATPG) programming utilizing an outer Automatic Test Equipment (ATE). However, this method uses costly equipment which is not available after the manufacturing process. For applications requiring high reliability and security, continuous testing is necessary through the entire life-cycle of the product.

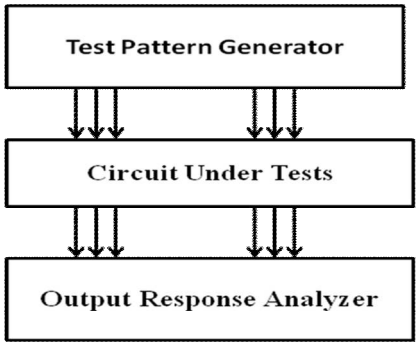

Fig 1 basic architecture of BIST

1) *Circuit Under Test (CUT):* It is the part of the circuit tried in BIST mode. It can be consecutive, combinational or a memory. Their Primary Input (PI) and Primary yield (PO) delimit it.
2) *Test pattern generator (TPG):* It creates the test designs for the CUT. It is a committed circuit or a microchip. The examples might be created in pseudorandom or deterministically.
3) *Output Response Analysis (TRA):* It investigations the quality arrangement on PO and contrasts it and the normal yield.

A. *Pseudo random pattern generator*

These utilization a formula to produce numbers which carry on extremely like real random numbers and are generally utilized for simulation of random procedures and measurable techniques. As a rule a decent pseudo-random number generator appears to fill in as you would expect a certifiable irregular generator to work.

In a perfect world, the created arbitrary numbers ought to be uncorrelated and fulfil any factual test for randomness. A generator can be either "really random" or "pseudo random". The previous shows genuine arbitrariness and the estimation of next number is erratic. The later just seems, by all accounts, to be irregular. The succession is really taking into account particular scientific calculations and in this manner the example is tedious and unsurprising. Be that as it may, if the cycle time frame is extensive, the succession gives off an impression of being non-tedious and arbitrary. In spite of the fact that it is conceivable to actualize a genuine arbitrary number generator in equipment, it is moderate and generally costly. Security conventions and encryption calculations are fundamentally taking into account random number generators. A LFSR (straight input shift register) is the most widely recognized

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circuit structure used to deliver pseudorandom vectors. In spite of the fact that its examples are deterministically create and thusly repeatable, the LFSR yield arrangement has a portion of the properties of random groupings.

III. LINEAR FEEDBACK SHIFT REGISTER

Linear Feedback Shift Register is a circuit comprising of flip-flops associated in arrangement with each other. The yield of one flip-flop is associated with the contribution of the following flip failure etc. The criticism polynomial which is otherwise called the trademark polynomial is used to determine the feedback taps which in turn determines the length of the random pattern generation. Linear-feedback shift register (LFSR) is a shift register whose input bit is a linear function of its previous state. The most commonly used linear function of single bits is exclusive-or (XOR).

A. Theory of operation

Feedback around an LFSR's shift register comes from a selection of points (taps) in the register chain and constitutes XORing these taps to provide tap(s) back into the register. Register bits that do not need an input tap, operate as a standard shift register. It is this criticism that causes the register to circle through dreary successions of pseudo-random worth. The decision of taps decides what number of qualities there are in a given grouping before the arrangement 0rehashes. The executed LFSR utilize a one-to-numerous structure, instead of a numerous to-one structure, since this

structure dependably has the most brief clock-to- clock delay way. Pseudo random number sequence generator is generated in VHDL according to the following circuit in Figure 1 based on the concept of shift register rather than a many-to- one structure, since this structure always has the shortest clock-to- clock delay path. Pseudo random number sequence generator is generated in VHDL according to the following circuit in Figure 2 based on the concept of shift register

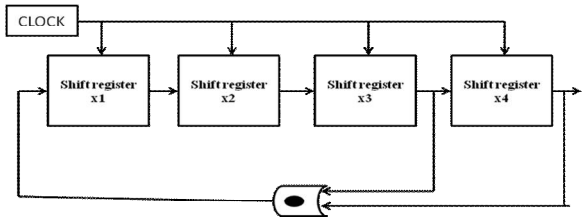

Fig 2 LINEAR FEEDBACK SHIFT REGISTER

The bits in the LFSR state which impact the information are called taps. A most extreme length LFSR produces a grouping (i.e. it pushes through all conceivable 2n- 1 state inside the movement register aside from the state where all bits are zero),

unless it contains all zeros, in which case it will never show signs of change. The grouping of numbers created by this technique is arbitrary. The period of the sequence is (2n - 1), where n is the number of shift registers used in the design.

B. Types of LFSR

There are two conventional forms of LFSR designs:

1) *Standard LFSR:* Figure shows an n-stage standard LFSR. It consists of n flip-flops and a number of XOR gates. Since XOR gates are placed on the external feedback path, the standard LFSR is also referred to as an external-XOR LFSR.

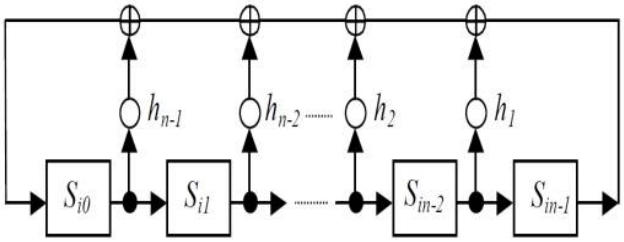

fig 3 n-state LFSR

2) *Modular LFSR:* Similarly, an n-stage modular LFSR with each XOR gat placed between two adjacent flip-flops, as shown in Figure 3, is alluded to as an inward XOR LFSR. This circuit runs quicker than its comparing standard LFSR, in light of the fact

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that every stage presents at most one XOR-entryway delay.

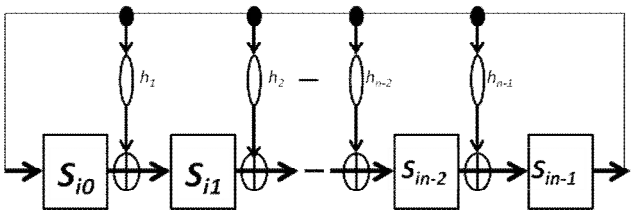

Fig 4 modular LFSR

IV. BASIC ARCHITECTURE OF PRESTO GENERATOR

A digital system is tested and diagnosed during its lifetime on numerous occasions. It is extremely basic to have fast and high blame scope testing. One basic and generally utilized as a part of semiconductor industry for IC chip testing is to guarantee this is to determine test as one of the framework capacities and consequently gets to be individual test. A framework outlined without an incorporated test strategy which covering all levels from the entire system to components is being described as chip-wise and system-foolish. A proper designed Built-In- Self-Test (BIST) can balance the expense of included test equipment while in the meantime guaranteeing the dependability, testability and diminish support cost . The essential considered BIST, in its most fundamental structure, is to diagram a circuit so that the circuit can test itself and figure out if it is good or bad; (blame free or defective, individually). This regularly requires extra hardware whose usefulness must be equipped for producing test designs and in addition giving a system to figure out whether the yield reactions of the circuit under test (CUT) to the test patterns correspond to that of a fault-free circuit . In all the cases test-per- clock and the test per-scan schemes are required

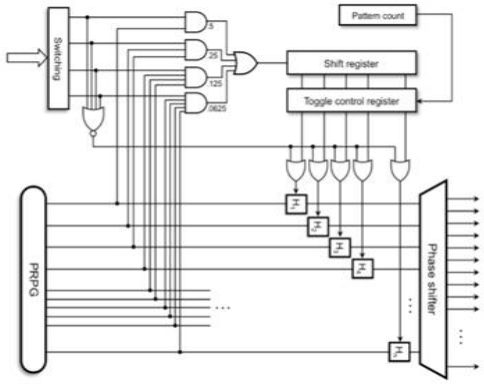

Fig 4 Basic architecture of PRESTO GENERATOR

The generator primarily aims at reducing the switching activity during scan loading due to its preselected toggling (PRESTO) levels.

A. Minimum transitions

In the proposed pattern, each generated vector applied to each and every PRPG output, which can minimize the input transition and decrease test power.

B. Uniqueness of examples

The proposed grouping does not contain any rehashed designs, and the quantity of unmistakable examples in an arrangement can meet the prerequisite of the objective shortcoming scope for the CUT.

C. Uniform distribution of examples

The customary calculations of adjusting the test vectors created by the LFSR utilize additional equipment to get more related test vectors with a low number of moves. Be that as it may, they may decrease the randomness in the patterns, which may result in lower fault coverage and higher test time.

D. Low hardware overhead consumed by extra TPGs[3]

The linear relations are selected with consecutive vectors or within a pattern, which has the benefit of generating a sequence with a

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sequential de-compressor[5]. Hence, the proposed TPG can be easily implemented by hardware. An n-bit PRPG [5] connected with a phase shifter feeding scan chains forms a kernel of the generator producing the actual pseudorandom test patterns. A linear feedback shift register or a ring generator can implement a PRPG.1) Minimum transitions: In the proposed pattern, each generated vector applied to each PRPG output, which can minimize the input transition and reduce test power.

E. Fully operational version of PRESTO GENERATOR WITH MEMORY CONTROLLER

Much higher flexibility in forming low-toggling test patterns can be achieved by deploying a scheme presented in Fig. Essentially, while preserving the operational principles of the basic solution, this approach splits up a shifting period of every test pattern into a sequence of alternating hold and toggle intervals. To move the generator back and forth between these two states, we use a T-type flip-flop that switches whenever there is a 1 on its data input. If it is set to 0, the generator enters the hold period with all latches temporarily disabled regardless of the control register content. This is accomplished by placing AND Gates on the control register outputs to allow freezing of all phase shifter inputs. This property can be crucial in SOC designs where only a single scan chain crosses a given core, and its abnormal toggling may cause locally unacceptable heat dissipation that can only be reduced due to temporary hold periods. If the T flip-flop is set to 1 (the toggle period), then the latches enabled through the control register can pass test data moving from the PRPG to the scan chains.

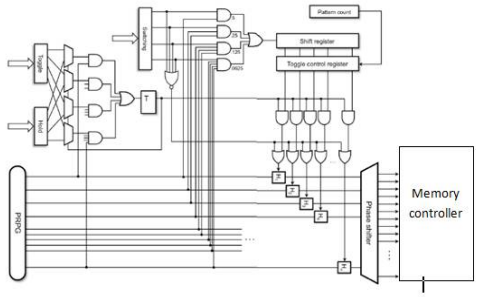

Fig 5 Fully operation architecture of memory controller

Here we are implementing memory controller which is not only a simple RAM memory but also used to store the data coming from phase shifter .memory controller stores the data coming from phase shifter and transfer it to other peripheral device when required . It stores the information when RD=0 and ,WR= 1. At this time it only stores the information .when RD=1, WR=0 this time data can be transferred to any peripheral devices. it also reduces the transition during the transmission to peripheral devices.

V. METHDOLOGY USED

A. Finite State Machine

Here we are using finite state machine for the generation of 64 bit Pseudo random pattern generator. State machine outlines are broadly utilized for successive control rationale, which frames the centre of numerous computerized frameworks. State machines are required in an assortment of

uses covering an expansive scope of execution and unpredictability; low-level controls of microchip to-VLSI- fringe interfaces, transport mediation and timing era in routine chip, custom piece cut chip, data encryption and decryption, and transmission protocols are but a few examples. Typically, the details of control logic are the last to be settled in the design cycle, since they are continuously affected by changing system requirements and feature enhancements. Programmable rationale is an easy-going answer for control rationale plan since it permits simple adjustments to be made without irritating PC board format. Its adaptability gives a getaway valve that licenses plan changes without affecting time-to- business sector.ere we are using finite state machine .
Basically there are two types of state machines –

1) Mealy machine-In the theory of computation, a Coarse machine is a limited state transducer that creates a yield taking into account its present state and information. This implies the state outline will incorporate both an info and yield signal for every move edge. The utilization of a Mealy FSM drives frequently to a lessening of the quantity of states.

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2) moore machine- A Moore machine is a finite state transducer where the outputs are dictated by the current State alone (and don't depend specifically on the information). The state outline for a Moore machine will incorporate a yield signal for every state. Contrast and a Mealy machine, which maps moves in the machine to output . The point of interest of the Moore model is a rearrangement of the conduct

B. Structural Style Of Modeling

In the structural style of modeling, an element is portrayed as an arrangement of interconnected parts. Basic displaying includes associating instantiated parts to characterize the usefulness of a circuit. component instantiations can be of different modules and/or gadget primitives. Utilizing entryway level permit the development of basic combinatorial circuits.

With structural code, on the other hand, you are connecting different parts together to get the final design.

We have use structural style of modelling for coding of different modules like for multiplexer we have designed one multiplexer and call it for 64 times at a time of operation .due to which the hardware utilization is also reduced.

VI. RESULTS AND DISCUSSION

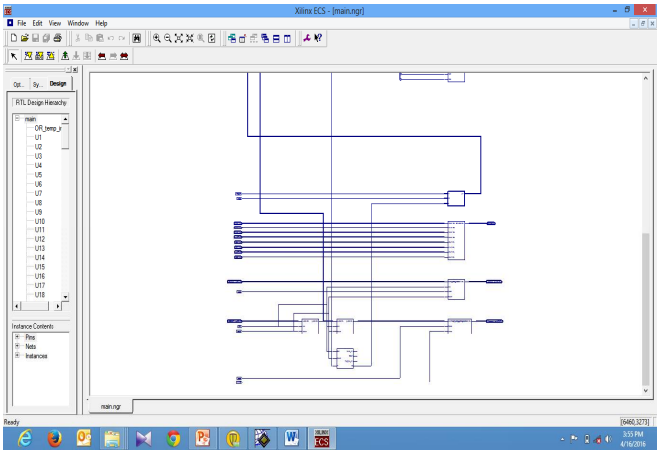

Fig 6 RTL of PRESTO GENERATOR OYTPUT WAVEFORM

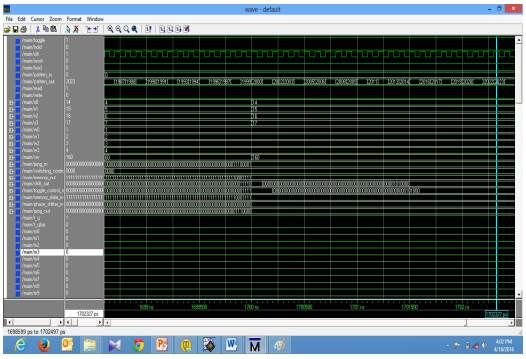

Fig 7 output waveform of PRESTO GENERATOR

This is the output waveform of 64bits PRESTO GENERATOR according to the applied inputs.

VII.CONCLUSION

The proposed approach shows the concept of reducing the transitions in the test pattern generated. The transition is reduced by increasing the correlation between the successive bits. The simulation results shows that how the patterns are generated for the applied seed vector. This paper presents the implementation with regard to verilog language. Synthesizing and implementation (i.e. Translate, Map and Place and Route) of the code is carried out on Xilinx - Project Navigator, ISE 12.3i suite .it also enhances the fault coverage upto 64 bits. Delay during the switching activity is also minimized by using structural style of modelling.

VIII. ACKNOWLEDGMENT

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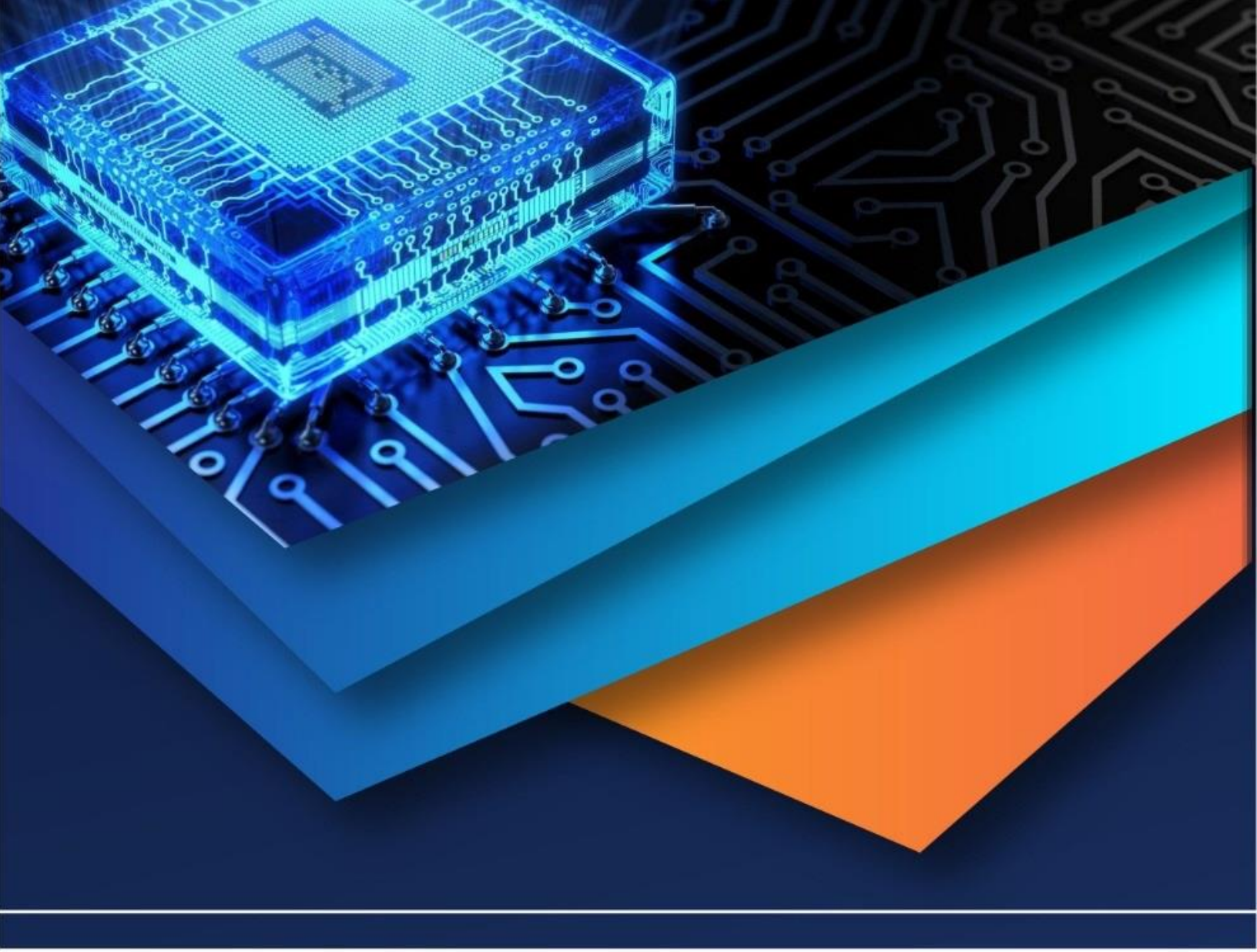
REFERENCES

[1] kenneth d. wagner, cary k. chin, and edward j. mc cluskey, fellow, IEEE Pseudorandom Testing
[2] Nur A. Touba and Edward J. McCluskey CRC Technical Transformed Pseudo-Random Patterns for BIST Report No. 94-10 (CSL TR No. 94-640)
[3] GaneshBabu.J 1, Radhika.P2 TEST PATTERN GENERATION USIN PSEUDO RANDOM International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering Vol. 2, Issue 5, May 2013.
[4] kanisetty reddy prasad (m.tech)1, chithra margaband M.Tech2.
[5] Mitrajit Chatterjee and Dhiraj K. Pradhan, Fellow, IEEE A BIST Pattern Generator Design for Near-Perfect Fault Coverage IEEE TRANSACTIONS ON COMPUTERS, VOL. 52, NO. 12, DECEMBER 2003M. Shell. (2002) IEEEtran homepage on CTAN./
[6] Swarup Bhunia, Student Member, IEEE, Hamid Mahmoodi, Student Member, IEEE, Debjyoti Ghosh, Saibal Mukhopadhyay, Student Member, IEEE, and Kaushik Roy, Fellow, IEEE "PDCA12-70 data sheet," Opto Speed SA, Mezzovico, Switzerland.
[7] Abhijit Jas, Member, IEEE, C. V. Krishna, Member, IEEE, and Nur A. Touba,Member, IEEE Weighted Pseudorandom Hybrid BIST ieee transactions on very large scale integration (vlsi) systems, vol. 12, no. 12, december 2004
[8] Patrick Girard, Christian Landrault, and Serge Pravossoudovitch LIRMM Arnaud Virazel and Hans-Joachim Wunderlich High Defect Coverage with Low-Power Test Sequences in a BIST Environment.
[9] S.Vinod Kumar, 2K. Govinda Rao 1Student,2 Assistant Professor ,Power Optimized Implementation of PRPG with Low Transition Test Compression Technique ijcsiet-- international journal of computer science information and engg ., technologies issn 2277-4408 .
[10] H.-G. Liang, S. Hellebrand, and H.-J. Wunderlich, "Two-dimensional test data compression for scan-based deterministic BIST," in Proc. Int. Test Conf. (ITC), 2001, pp. 894–902.



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