iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 4 **Issue:** VI **Month of publication:** June 2016

DOI:

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

Volume 4 Issue VI, June 2016
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

Implementation of 8-bit Sigma-Delta ADC using 45nm Technology

Yogita Tembhre[#1], Anil Kumar Sahu[*2]
[#] *ETC, SSTC, SSGI (FET) Bhilai, India*

Abstract— Design for oversampling sigma-delta (ΣΔ) ADCs is conferred here. In this paper a contemporary design for 8-bit ΣΔ oversampling ADC is presented, in which first order oversampling ΣΔ modulator and the decimation filter is second order Cascaded Integrated Comb (CIC) filter which is utilized. Transistor level circuit design and output simulation of the sigma-delta ADC with a power supply of 1V is presented here. This architecture is implemented by Tanner EDA tool v15.0 using 45nm BSIM4 CMOS technology.
Keywords— 8-bit Sigma-Delta ADC, BSIM4, CIC filter, Oversampling, Sigma delta modulator.

I. INTRODUCTION

Oversampling ΣΔ ADCs are pervasively termed as oversampling ADCs. ΣΔ ADCs become popular in nano-CMOS technologies as the higher sampling rates allow higher transference bandwidths while reaching medium resolution. Initially ΣΔ ADCs was applied on audio and other sensing applications which require high-resolution, but recently, these modulators are widely utilized in reconfigurable radio and wireless communication systems. A ΣΔ ADC based on two aspects noise shaping and oversampling, which allow higher data conversion accuracy, i.e. optimum trade off between resolution and speed. Also, oversampling diminishes the necessity of the anti-aliasing filter with the modulator [1]. ΣΔ -Modulators are trending in ADCs because of the high accuracy results in standard low-cost CMOS technology. Being an oversampling converter, ΣΔ -ADCs do not have a direct input to output relationship.

Oversampling ADCs may be designed by using either discrete-time (switched-capacitor) loop-filter or a continuous-time loop filter. Both the style has some benefits as well as drawbacks. The discrete-time ΣΔ ADCs is used in industrial designs, whereas the continuous-time ΣΔ ADCs is popular with the academics. CT-ΣΔ ADCs are becoming popular in broadband wireless communication systems because of some desirable features which include anti-aliasing filtering, with relaxed bandwidth requirements of the active elements and lower power consumption. However, there are few challenges in the adoption of CT-ΣΔ ADCs in industries due to the complex design because of a hybrid CT and DT system, and sensitiveness to the T_{RC} (time constant) of RC circuit and also timing jitter [10].

II. PREVIOUS WORK

With the improvements of IC technologies it is difficult to obtain a low power supply and devices with shorter channel length. Preferably, opamps with a large dc gain were avoided by single stage modulator circuits. Despite, practically it is tough to make stable higher order single stage modulators. The first order ΣΔ modulator has many benefits over other higher order ΣΔ modulators as on area, performance, and power consumption [6]. DT ΣΔ modulator importantly shortens the necessity of interference and the operational amplifier gain by using noise shaping technology, well capacitive matching features and oversampling, so it is very pertinent for lower voltage applications [9]. Alternatively ΣΔ modulator can also be designed based on LDI ladder (lossless digital integrator) for high order and stable oversampled oscillator using modulation techniques [5].

III.PROPOSED CIRCUIT

A. First Order Sigma Delta Modulator

In this, primary single stage sigma-delta modulator built by using a comparator, an integrator, a 1-bit DAC in the feedback loop and an op-amp. Normally, the output of modulator is the results of repeated measurement between the analog i/p and the response output of the 1-bit DAC. This comparison is measured at the op-amp at the x inception of the modulator. After that, the output of the op-amp is fed to the integrator, which measures the analog-voltage output and presents a sloping signal to the comparator. Then, the comparator will compare the input which comes from the integrator with the reference voltage and remodel it to a digital signal which is digital one or zero. The response of the comparator is act as the output of the modulator and also provided to the 1-bit DAC

Volume 4 Issue VI, June 2016
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

as a feedback. The main task of the modulator is to encode an analog signal to 1-bit digital bit stream which equal to the actual value.

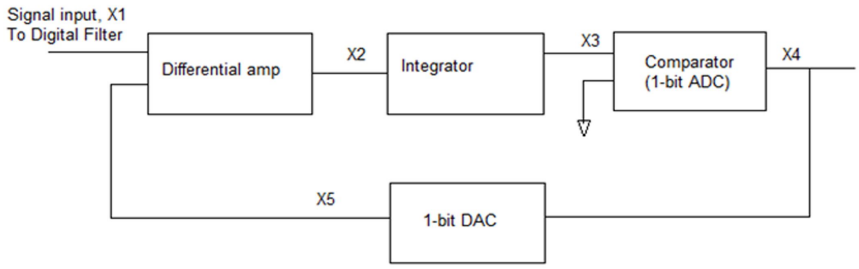


Fig. 1. Basic first order ΣΔ modulator Architecture

1) OP-AMP: The diagram below depicts the two-stage CMOS op-amp transistor level circuit design. The first phase is used as differential input while the second stage is used for additional voltage gain. The first stage of the op-amp considered comprises transistor (PMOS_1, PMOS_2, NMOS_1, NMOS_2, and PMOS_4). Here transistors PMOS_1- PMOS_2 and NMOS_1- NMOS_2 are p-channel differential transistor pair and n-channel current sourcing mirror load respectively, and transistor PMOS_4 is a tail current source transistor. The second phase contains the transistors PMOS_5, NMOS_3 in which PMOS_5 is n-channel common-source amplifier and NMOS_3 is a p-channel current load. The other transistors PMOS_3 and PMOS_6 give biasing to the circuit.

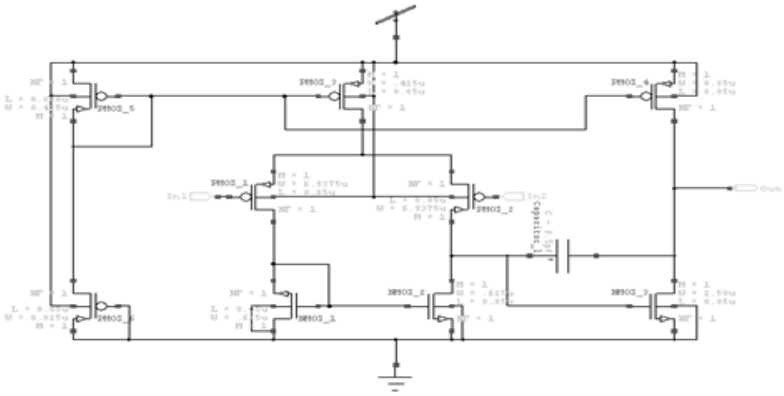


Fig. 2. Schematic of the two stage CMOS OP-AMP

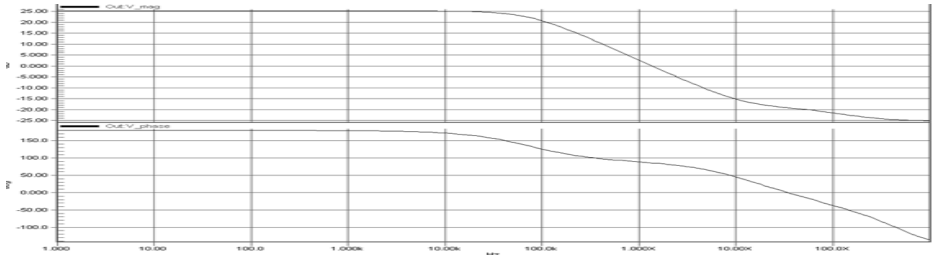


Fig. 3. Frequency response characteristic of the two stage CMOS OPAMP

TABLE I: PARAMETERS OF OPAMP

Parameters	Values
Gain	25dB
Gain bandwidth product	34.4279X
Phase margin	266
Average Power consumed	2.54uW

Volume 4 Issue VI, June 2016
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

2) Switched-Capacitor Integrator: Switched-capacitor integrator is used to design the modulator. A switched-capacitor integrator consists of two capacitors, (a sampling capacitor and a hold capacitor), an op-amp and switches (S1, S2, S3 and S4). The clock signals Φ1 and Φ2 applied to form non-coinciding clock signals. Switches S1 and S3 are ON and switch S2 and S4 initially OFF when clock Φ1 is high and start to charge the sampling capacitor, Cs until equal the input voltage. When clock Φ1 fall, clock Φ2 start to rise and at the same time S1 and S3 are OFF while switches S2 and S4 turn ON which connecting the sampling capacitor, Cs [11].

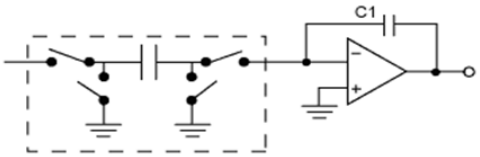


Fig. 4. Circuit diagram of Switched-capacitor Integrator

3) COMPARATOR: To design the comparator, we just used the two-stage op-amp makes some modification on it so that it acts like a comparator. The modification that needs to do is just removed the compensation capacitor 0.5pF from the actual circuit of the two-stage op-amp.

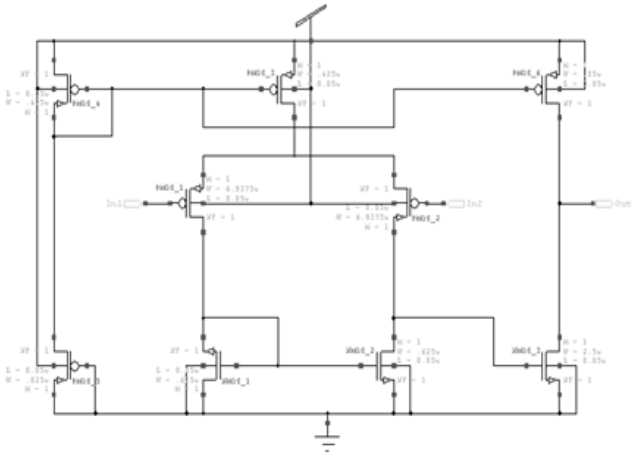


Fig. 5. Schematic of Comparator

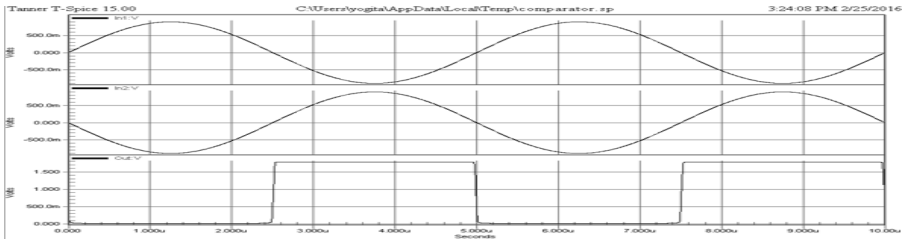


Fig. 6. Waveform of Comparator

After complete designing all the components-part that required in the modulator, all the components-parts are combining all together to make a complete design of the ΣΔ modulator. The non-overlapping input for the switched-capacitor integrator is from the output of the switched-capacitor circuit while the overlapping input of the comparator is from the output of the switched-capacitor integrator.

Volume 4 Issue VI, June 2016
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

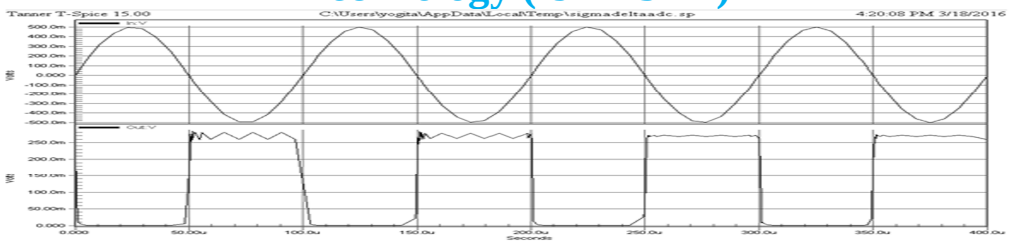


Fig. 7. Input and output waveform of ΣΔ modulator

B. Decimation Filter

The architecture of decimation filter that being used is the Cascaded Integrated Comb (CIC) filter. There are two essential building blocks integrator and differentiator in the first order CIC filter. The integrator considered is an IIR filter having single pole with identity response coefficient, which also acts as the accumulator. The single integrator is unstable due to the single pole at z = 1, due to this there is a high chance of register overflow and data may be lost. To avoid this problem, two's complement technique is considered [7]. Since here CIC filter is used, the order of CIC filter is can be determined by looking the sigma-delta modulator used. For the given condition, here first order sigma-delta modulator is used, i.e. L = 1, hence the CIC filter is used in the order of k = L + 1. It is clear that to properly undermine the quantization noise a second order CIC filter is required. Since we deal with high order and sampling rates, the circuit becomes more complex. To minimize the complicatedness a decimation stage is introduced between integrator and differentiator stage. The clock divider divides the oversampling frequency by the oversampling ratio (K) before going into the differentiator while the integrator operates in the oversampling frequency. Since the differentiator operates in low frequency it makes a reduction in power consumption. There are two major stages which are integrator stage and differentiator stage. The implementation of the concept of second order CIC filter in circuit design is as shown in Figure as we want to produce an 8-bit digital response.

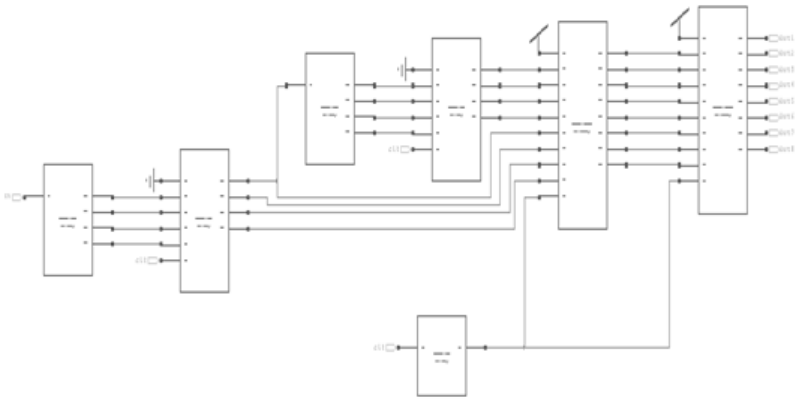


Fig. 8. Circuit diagram of decimation filter

C. Level Shifter

A level shifter circuit is used to provide the level shift in the voltage range from - 0.5 V - + 0.5 V to 0 V - 1 V. It is at the input end of the decimator and forms the interface between the modulator and the decimator. The available modulator operates within a voltage range of ± 0.5 V for the purpose of biasing the operational amplifier and setting the reference voltage at 0 V. The decimator is a digital circuit and designed to work in the 0 to 1 V range. Since the response of the modulator is in the ±0.5V, it becomes significant for having a circuit at the input stage of the decimator which can provide the necessary shift in the voltage level. The transistor level circuit for the level shifter which is considered is a simple buffer circuit.

Volume 4 Issue VI, June 2016
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

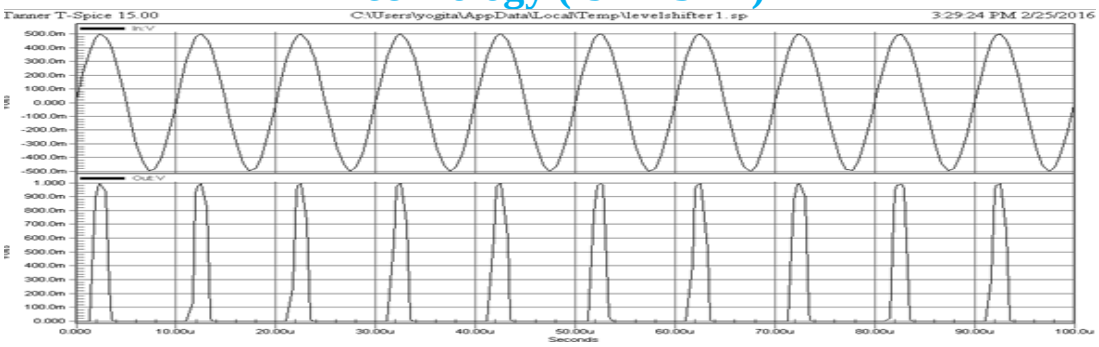


Fig. 9. Input and Output waveform of level shifter

IV. SIMULATION AND RESULT OF SIGMA DELTA ADC

The ΣΔ ADC is created using a Tanner EDA tool v15.0 using a 45nm BSIM4 CMOS process, the supply voltage is 1V. All the main parameters of the described 8-bit ΣΔ ADC are summed up in the Table II given below. Oversampling ΣΔ ADC is designed by using ΣΔ modulator, level shifter and decimation filter. Fig. 14 depicts the 8-bit oversampling ΣΔ ADC.

TABLE II: PARAMETERS OF ADC

PARAMETERS	VALUE
Technology	45nm
Order of Modulator	1
Order of decimation filter	2
Supply voltage	1V
Resolution	8 bit
Average power consumed	6.7mW

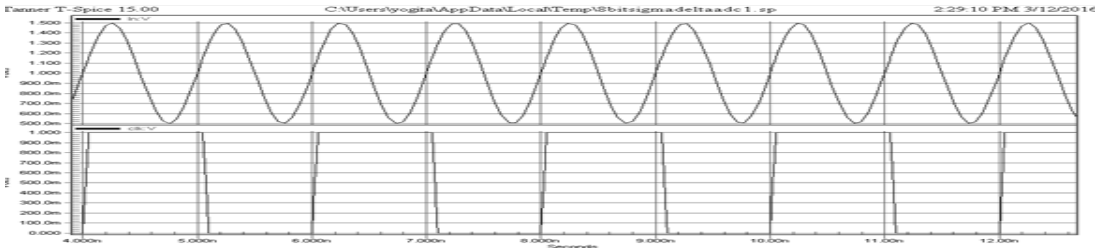


Fig. 10. Input waveform of ΣΔ ADC

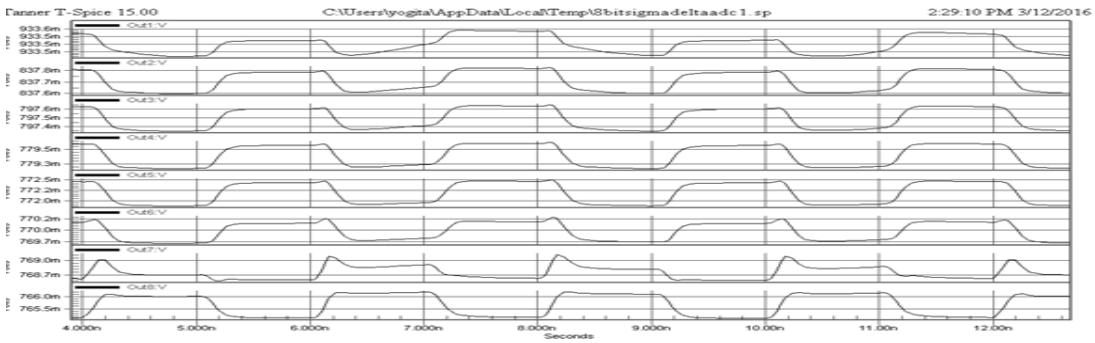


Fig. 11. Output waveform of ΣΔ ADC

TABLE III
COMPARISON OF PRESENT WORK WITH PREVIOUS WORK

TECHNOLOGY (CMOS)	SUPPLY VOLTAGE	RESOL-UTION	ORDER OF MODUL-ATOR	POWER CONSUMPTION	REFERENCES
0.35um double-poly treble metal	5/3	16	2	300mW	[1]
0.18um one-poly six metal	1.8	12	0-3MASH	24mW	[2]
0.35um	3.3	10	1	12.2mW	[4]
0.18um double poly five metal	1.8	14	5	150mW	[6]
0.045um BSIM4	1	8	1	6.7mW	Present work

V. CONCLUSION

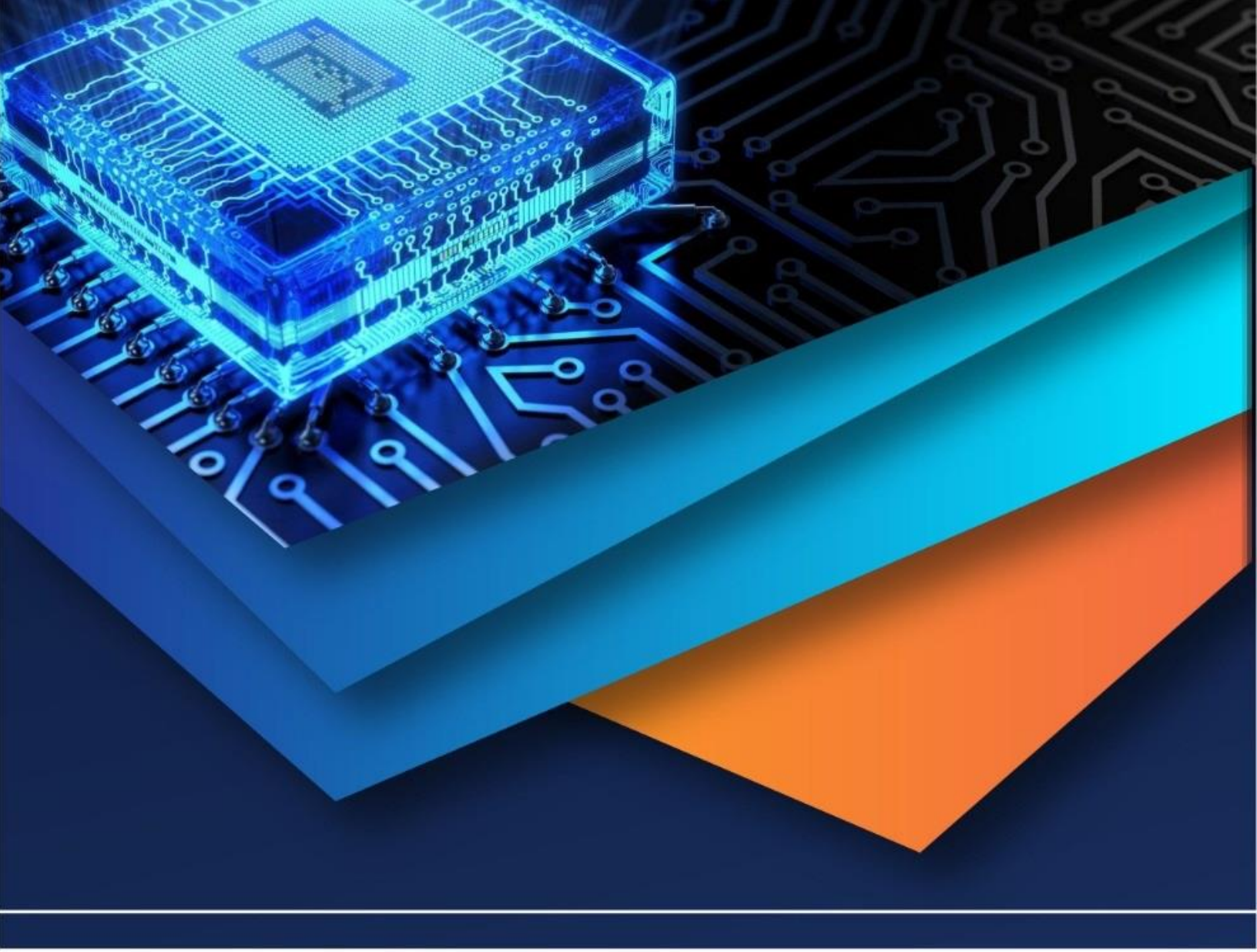
This paper has presented a technique of designing first order sigma delta ADC. A design procedure for first order ΣΔ modulator and second stage CIC filter for decimation filter was presented. This ΣΔ ADC is can be further used in the ADC BIST pattern to detect the faults present in any given problem. The present paper gives the ΣΔ ADC in Tanner EDA tool v15.0 using 45nm BSIM4 CMOS technology. The advantages of first stage modulator over other modulators are on performance, power dissipation and also stability.

VI. ACKNOWLEDGMENT

The authors would like to thank the management, SSTC SSGI institute for providing Tanner EDA Tool v15.0.

REFERENCES

[1] Li Liang, Ruzhang Li, Zhou Yu, Jiabin Zhang and Jun'an Zhang, "A 16-bit cascaded sigma-delta pipeline A/D converter" Journal of Semiconductors , May 2009, pp. 550101-550106.
[2] A. Gharbiya and David A. Johns, "A 12-bit 3.125 MHz bandwidth 0-3 MASH delta-sigma modulator" IEEE Journal of Solid-State Circuits, July 2009, pp. 2010-2018.
[3] L. Liu, Li Dongmei, Chen Liangdong, Ye Yafei and Z. Wang, "A 1-V 15-bit audio-ADC in 0.18 m CMOS" IEEE Transactions on Circuits and Systems, May 2012, pp. 915-925.
[4] L. Hernández Corporales, Prefasi Enrique, Pun Ernesto and Patón Susana "A 1.2-MHz 10-bit Continuous-Time Sigma-Delta ADC Using a Time Encoding Quantizer" IEEE Transactions on Circuits and Systems, January 2009, pp. 16-20.
[5] Dallet Dominique, Chiheb Rebai, and Marchegay Philippe "Signal generation using single-bit sigma-delta techniques" IEEE Transactions on Instrumentation and Measurement, August 2004, pp. 1240-1244.
[6] R. Jiang, and S. Fiez Terri "A 14-bit delta-sigma ADC with 8× OSR and 4-MHz conversion bandwidth in a 0.18-µm CMOS process" IEEE Journal of Solid-State Circuits, January 2004, pp. 63-74.
[7] M. Arifuddin Sohel, K. Chenna Kesava Reddy and Syed Abdul Sattar. "Design of low power Sigma Delta ADC" International Journal of VLSI design & Communication Systems, August 2012, pp. 67-80.
[8] Yamei Li and He. Lili "First-order continuous-time sigma-delta modulator" IEEE International symposium on Quality Electronic Design, March 2007, pp. 229-232..
[9] R. Laajimi, "First order sigma-delta modulator with low-power consumption implemented in ams 0.35 µm cmos technology" International Journal of Research in Engineering and Technology, April 2013, pp. 700-705.
[10] V. Acharya, "MWSCAS 2012 Tutorial Proposal Delta-Sigma Analog-to-Digital Converters-From System Architecture to Transistor-level Design".
[11] Nowshad Amin, Goh Chit Guan, and Ahmad Ibrahim, "An efficient first order sigma delta modulator design." IEEE In Electrical and Computer Engineering, 2008, pp. 000029-000032..
[12] Anil Kumar Sahu, Vivek Kumar Chandra and G. R. Sinha, "System Level Behavioral Modeling of CORDIC Based ORA of Built-in-Self-Test for Sigma-Delta Analog-to-Digital Converter" International Journal of Signal and Image Processing, 2016, pp. 37-44.



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY